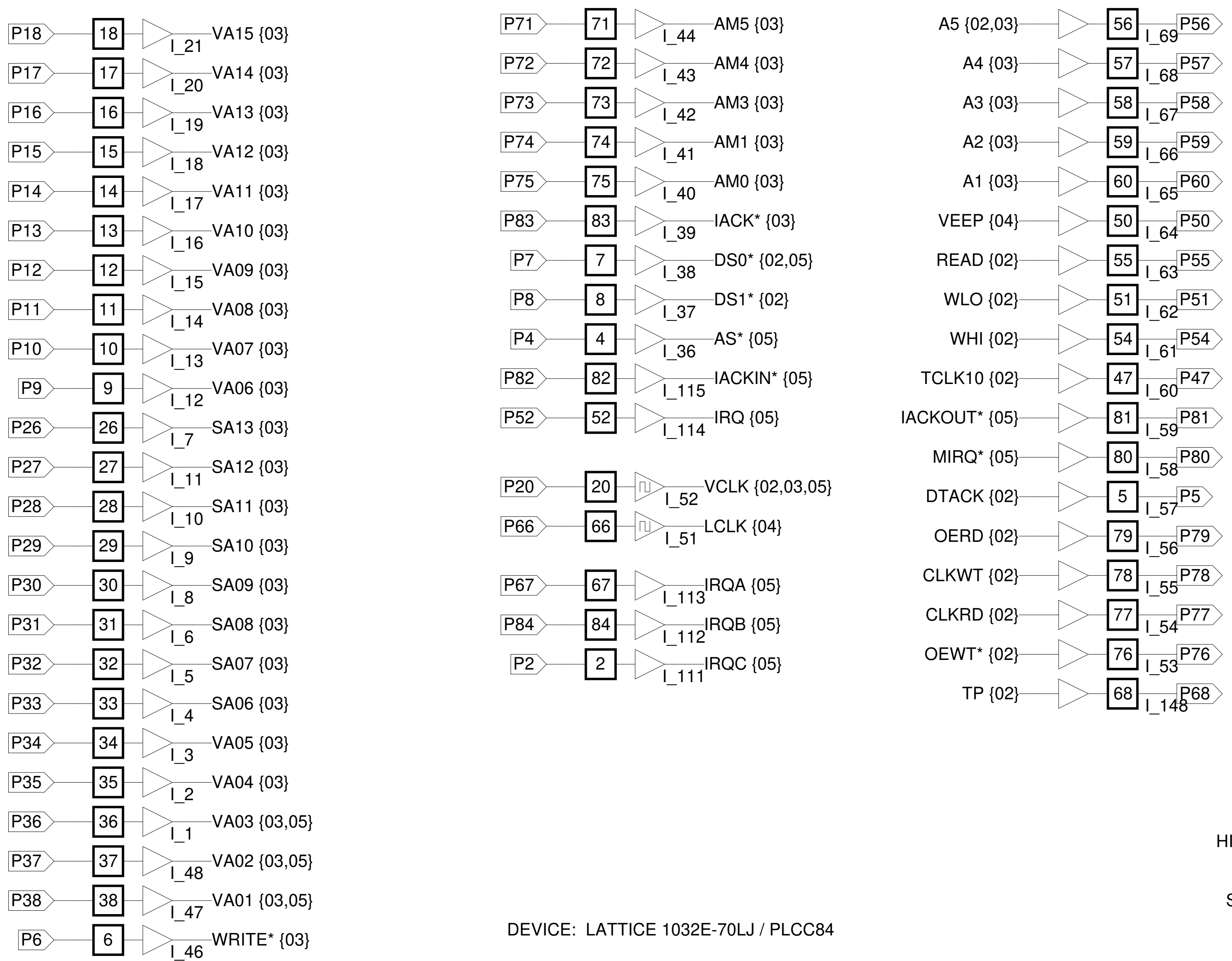


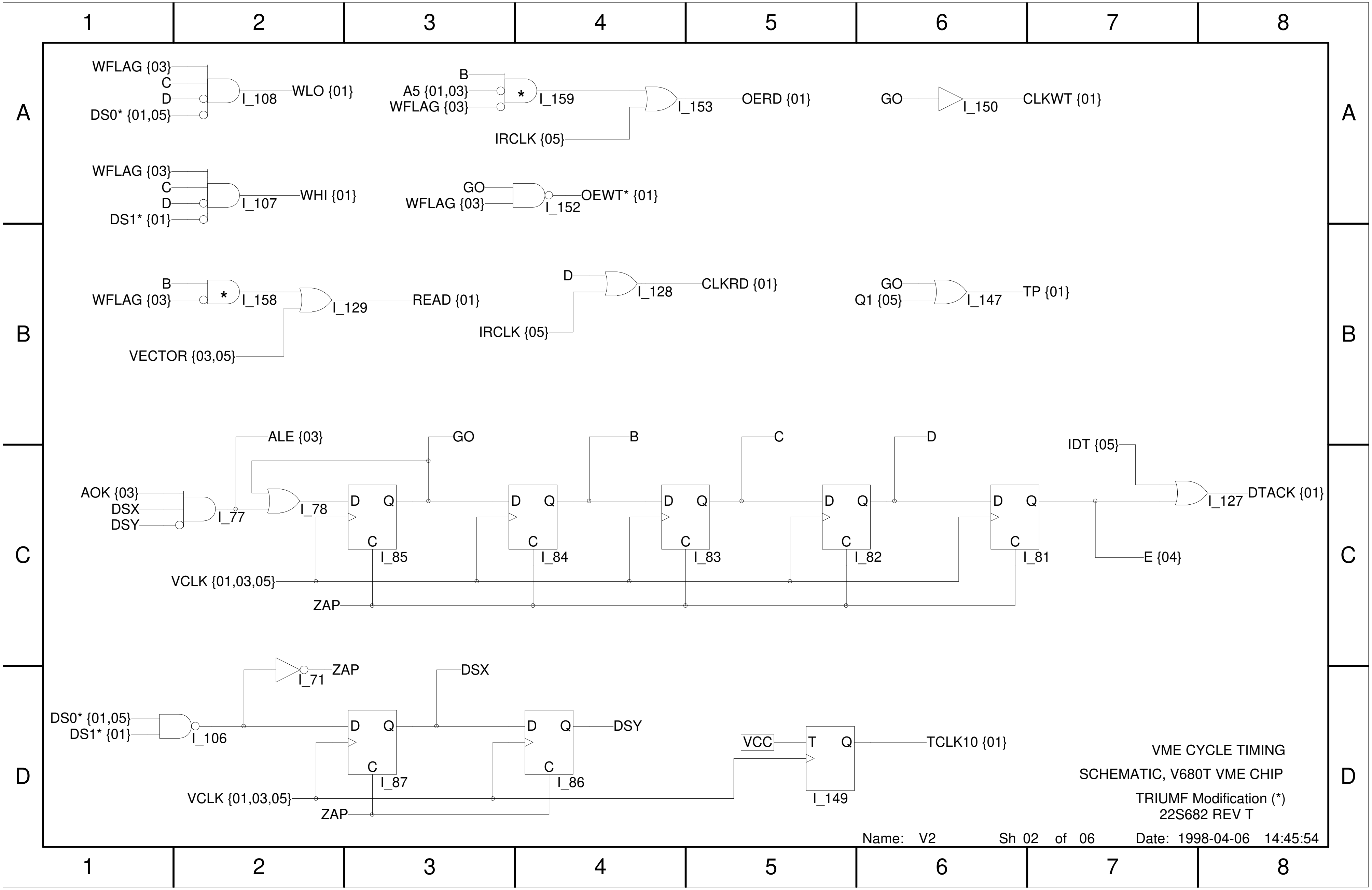
DEVICE: LATTICE 1032E-70LJ / PLCC84

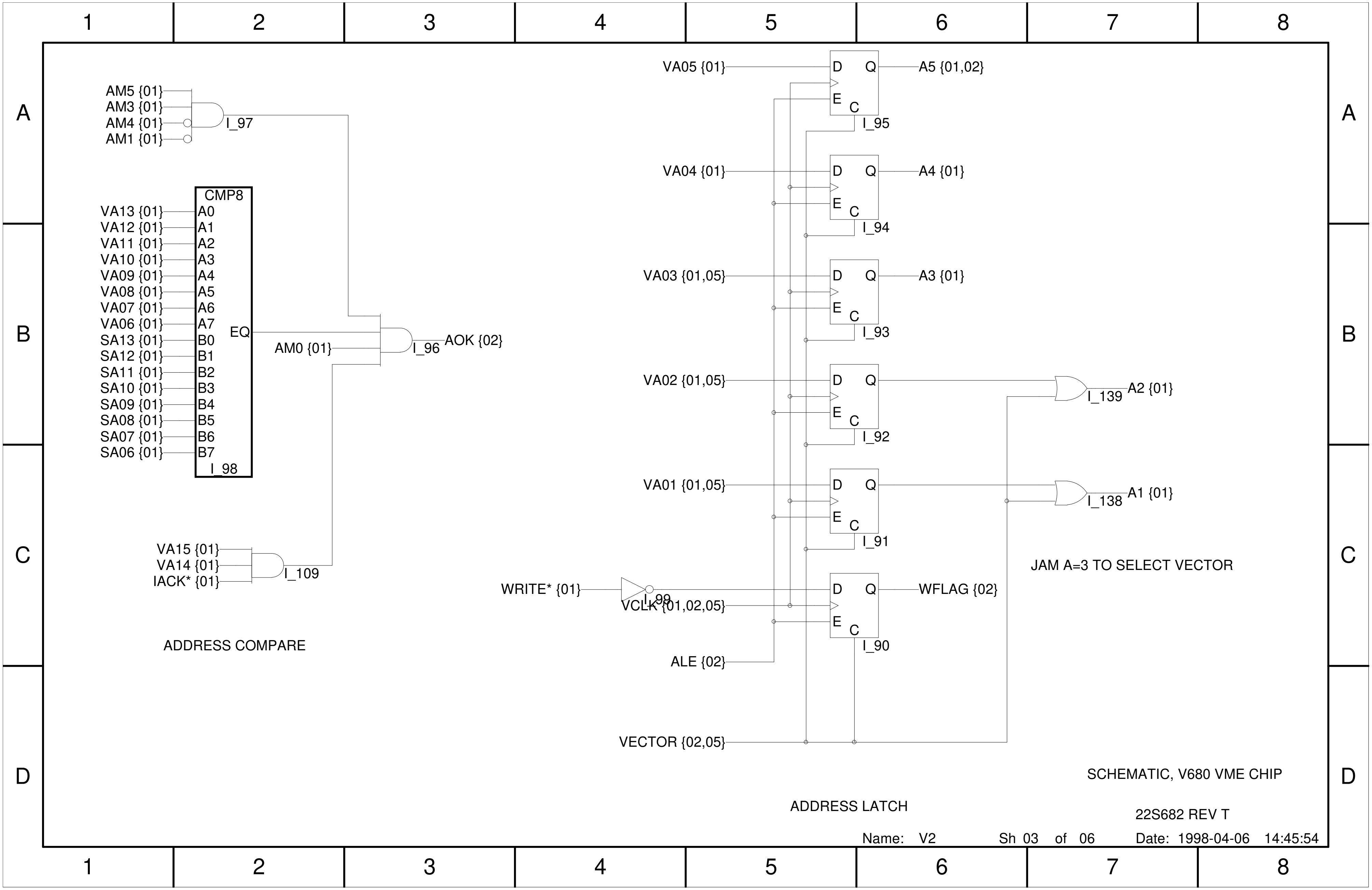
HIGHLAND TECHNOLOGY, INC

SCHEMATIC, V680 VME CHIP

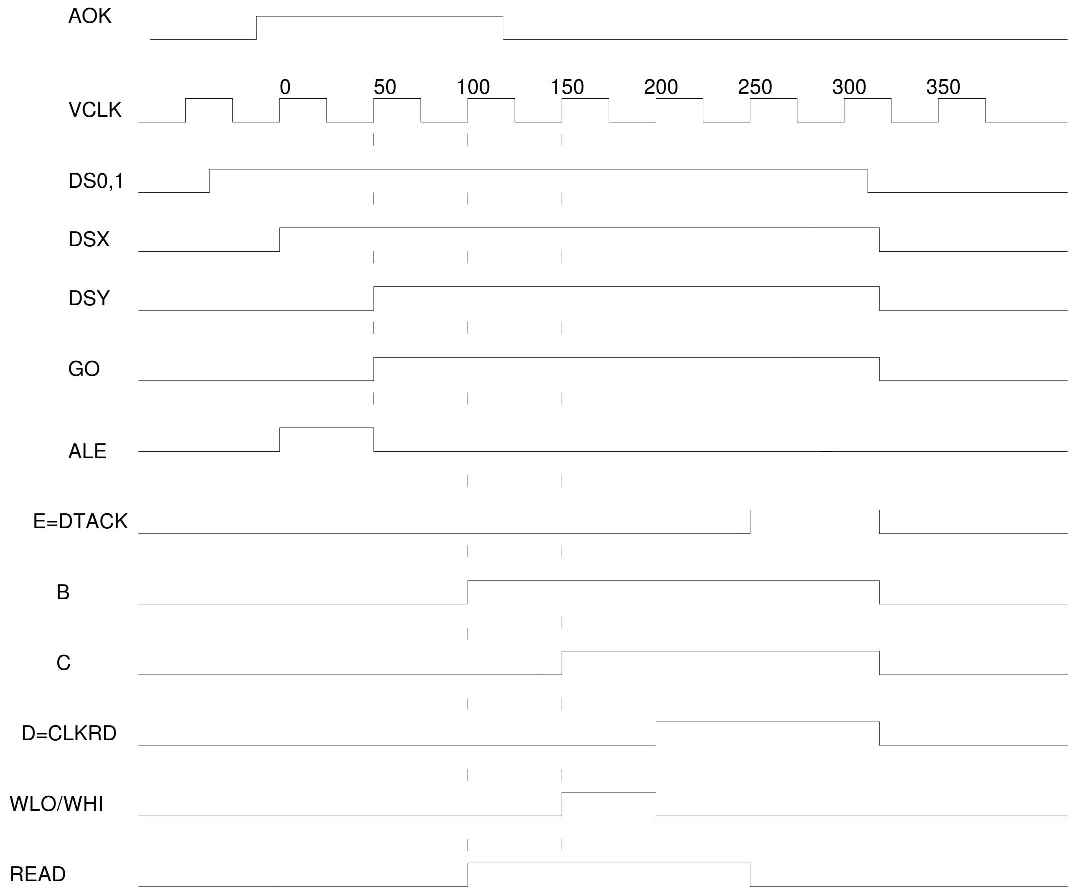
22S682 REV T

Name: V2 Sh 01 of 06 Date: 1998-04-06 14:45:54

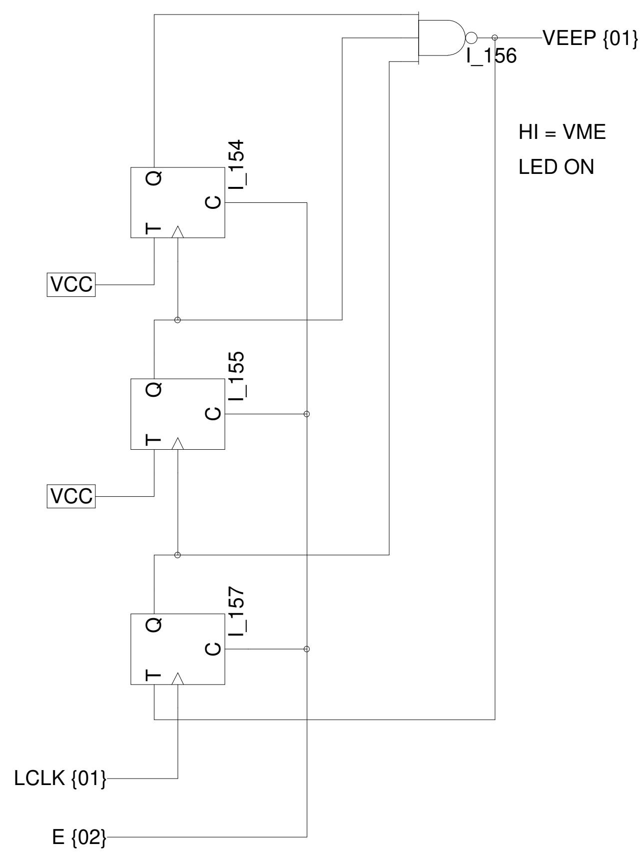

WFLAG {03}
C
D
DS0* {01,05}
I_108
WLO {01}
B
A5 {01,03}
WFLAG {03}
*
I_159
I_153
OERD {01}
IRCLK {05}
GO
I_150
CLKWT {01}
WFLAG {03}
C
D
DS1* {01}
I_107
WHI {01}
GO
WFLAG {03}
I_152
OEWT* {01}
B
WFLAG {03}
*
I_158
I_129
READ {01}
VECTOR {03,05}
D
I_128
CLKRD {01}
IRCLK {05}
GO
Q1 {05}
I_147
TP {01}
ALE {03}
GO
B
C
D
IDT {05}
AOK {03}
DSX
DSY
I_77
I_78
I_85
I_84
I_83
I_82
I_81
I_127
DTACK {01}
E {04}
VCLK {01,03,05}
ZAP
I_71
ZAP
DSX
DS0* {01,05}
DS1* {01}
I_106
I_87
I_86
DSY
VCC
T
Q
TCLK10 {01}
I_149
VCLK {01,03,05}
ZAP
VME CYCLE TIMING
SCHEMATIC, V680T VME CHIP
TRIUMF Modification (*)
22S682 REV T
Name: V2
Sh 02 of 06
Date: 1998-04-06 14:45:54



AM5 {01}
AM3 {01}
AM4 {01}
AM1 {01}
I_97
CMP8
VA13 {01} A0
VA12 {01} A1
VA11 {01} A2
VA10 {01} A3
VA09 {01} A4
VA08 {01} A5
VA07 {01} A6
VA06 {01} A7
SA13 {01} B0
SA12 {01} B1
SA11 {01} B2
SA10 {01} B3
SA09 {01} B4
SA08 {01} B5
SA07 {01} B6
SA06 {01} B7
EQ
I_98
AM0 {01}
I_96
AOK {02}
VA15 {01}
VA14 {01}
IACK* {01}
I_109
ADDRESS COMPARE
VA05 {01}
A5 {01,02}
I_95
VA04 {01}
A4 {01}
I_94
VA03 {01,05}
A3 {01}
I_93
VA02 {01,05}
I_92
A2 {01}
I_139
VA01 {01,05}
I_91
A1 {01}
I_138
JAM A=3 TO SELECT VECTOR
WRITE* {01}
I_99
VCLK {01,02,05}
WFLAG {02}
I_90
ALE {02}
VECTOR {02,05}
D Q E C
ADDRESS LATCH
SCHEMATIC, V680 VME CHIP
22S682 REV T
Name: V2
Sh 03 of 06
Date: 1998-04-06 14:45:54



VME CYCLE TIMING



SCHEMATIC, V680 VME CHIP

22S682 REV T

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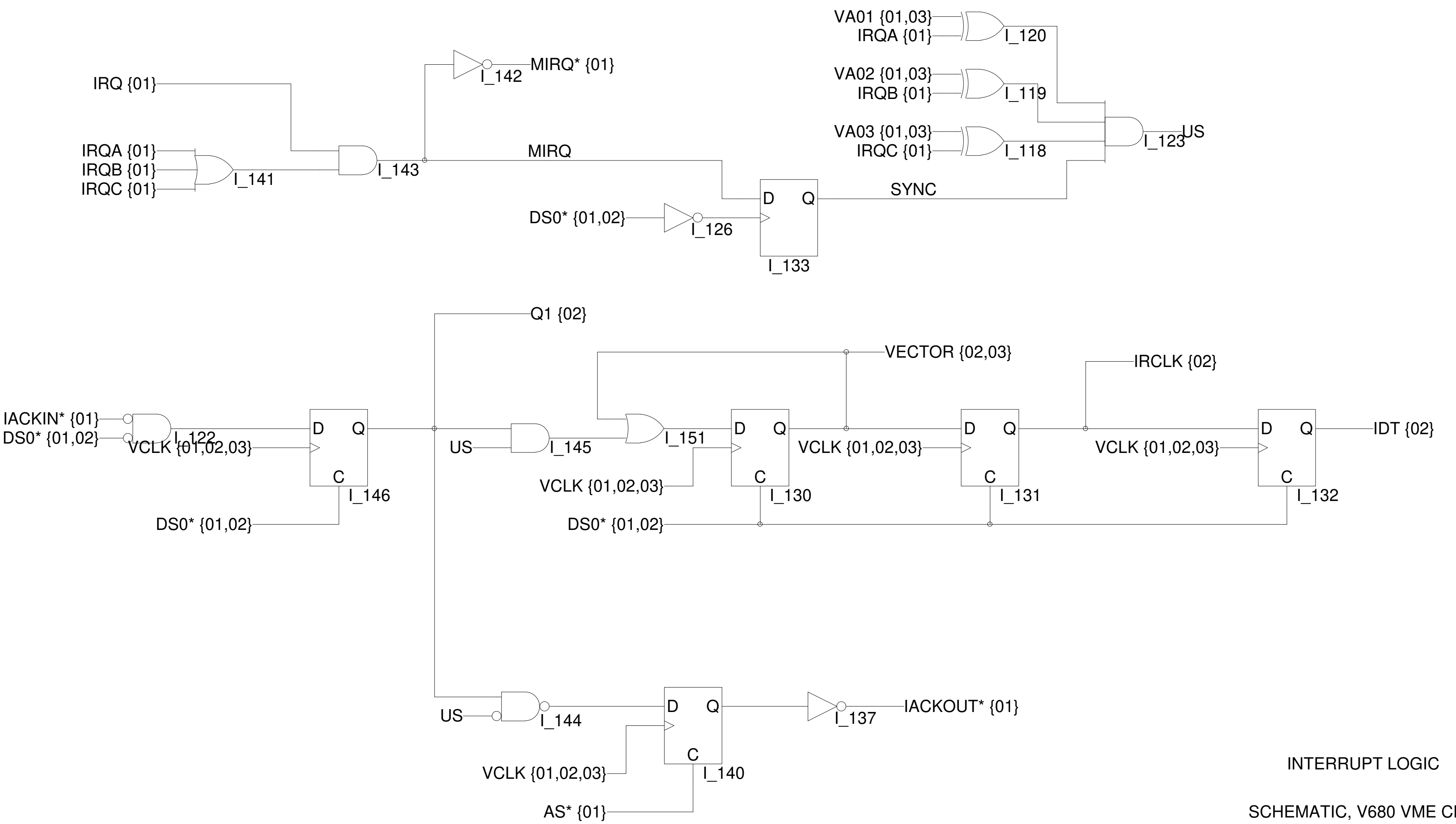
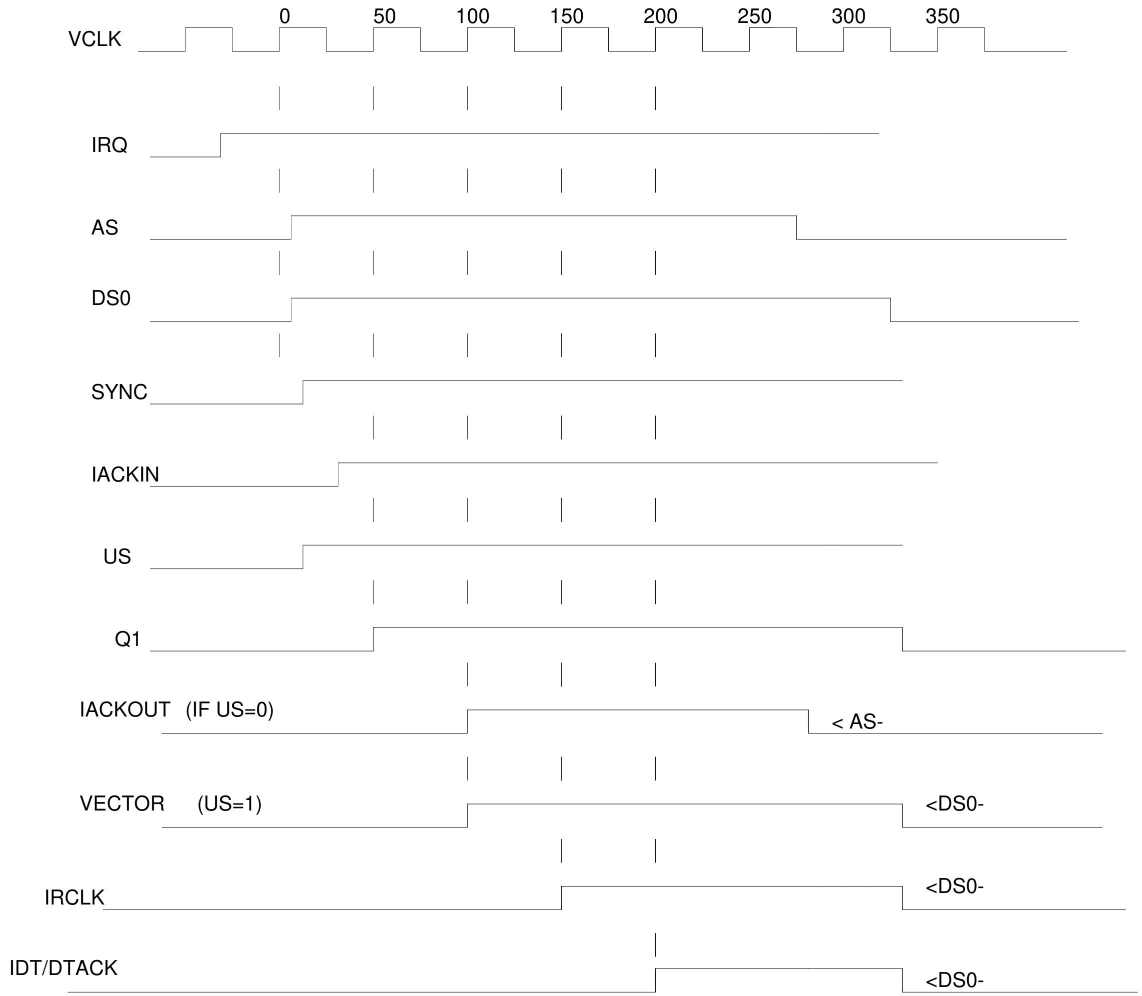


INTERRUPT LOGIC

SCHEMATIC, V680 VME CHIP

22S682 REV T

Name: V2 Sh 05 of 06 Date: 1998-04-06 14:45:54



INTERRUPT TIMING

SCHEMATIC, V680 VME CHIP

22S682 REV T

Name: V2 Sh 06 of 06 Date: 1998-04-06 14:45:54