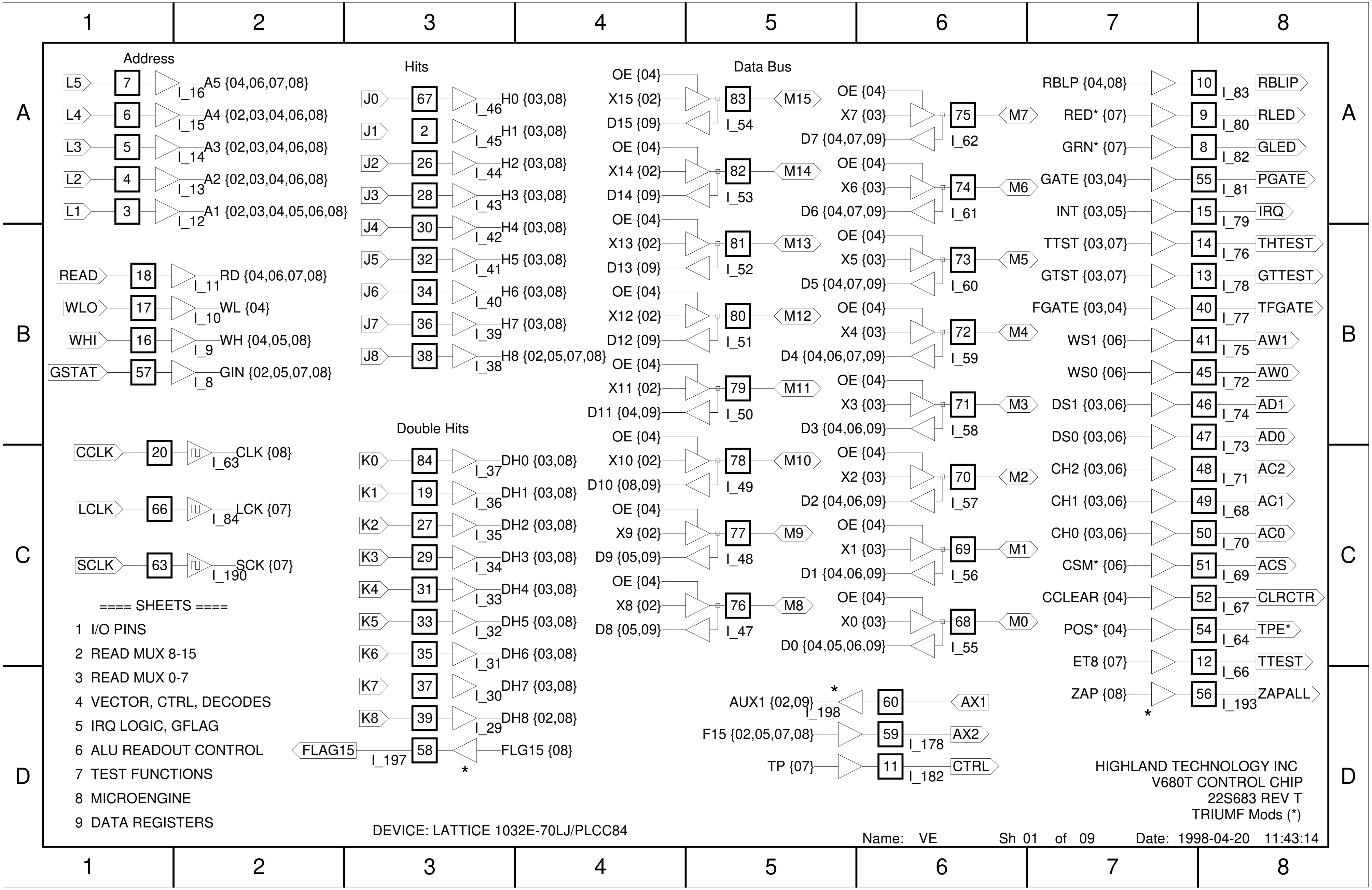
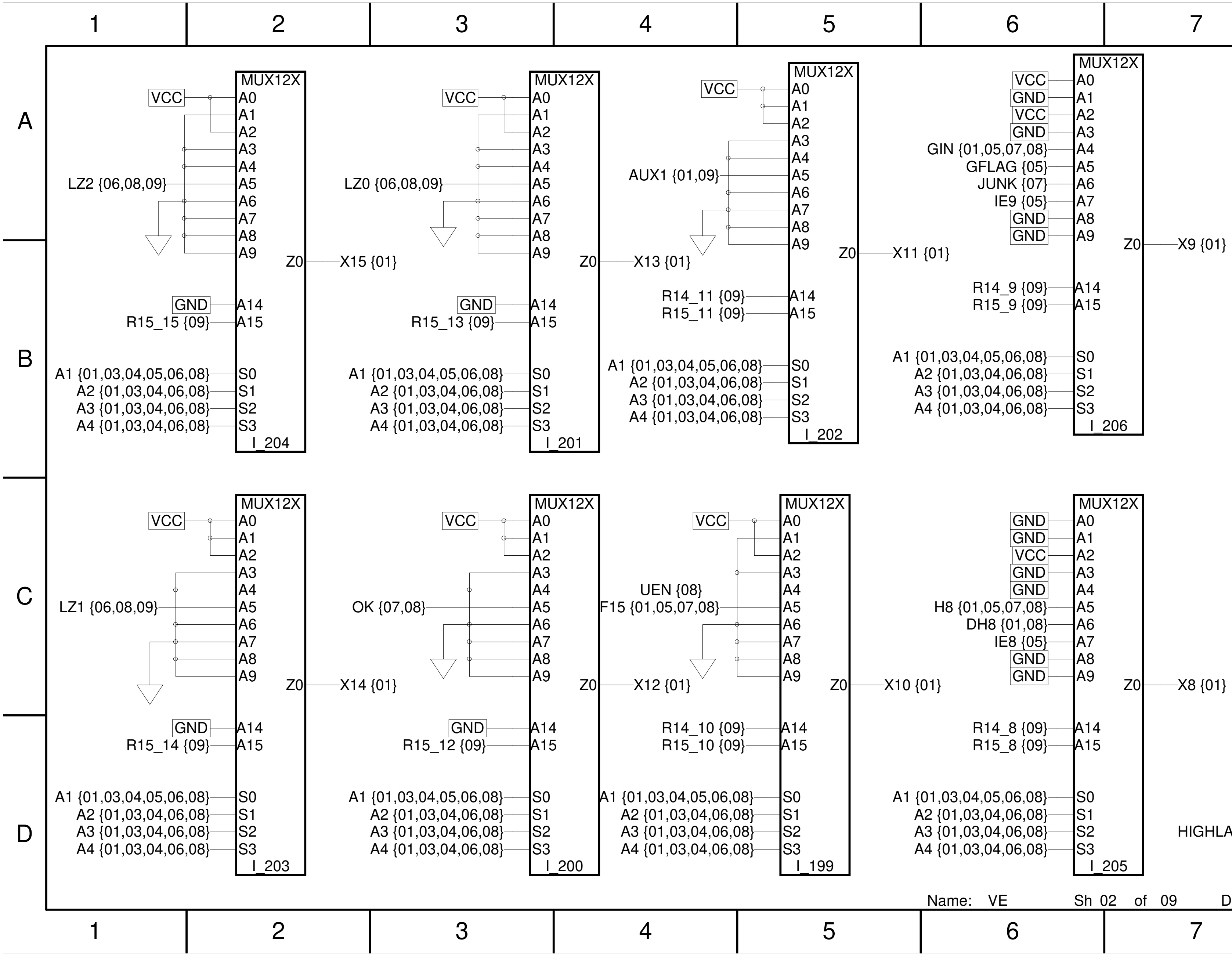

Address
L5 7 I_16 A5 {04,06,07,08}
L4 6 I_15 A4 {02,03,04,06,08}
L3 5 I_14 A3 {02,03,04,06,08}
L2 4 I_13 A2 {02,03,04,06,08}
L1 3 I_12 A1 {02,03,04,05,06,08}
READ 18 I_11 RD {04,06,07,08}
WLO 17 I_10 WL {04}
WHI 16 I_9 WH {04,05,08}
GSTAT 57 I_8 GIN {02,05,07,08}
CCLK 20 I_63 CLK {08}
LCLK 66 I_84 LCK {07}
SCLK 63 I_190 SCK {07}
==== SHEETS ====
1 I/O PINS
2 READ MUX 8-15
3 READ MUX 0-7
4 VECTOR, CTRL, DECODES
5 IRQ LOGIC, GFLAG
6 ALU READOUT CONTROL
7 TEST FUNCTIONS
8 MICROENGINE
9 DATA REGISTERS
Hits
J0 67 I_46 H0 {03,08}
J1 2 I_45 H1 {03,08}
J2 26 I_44 H2 {03,08}
J3 28 I_43 H3 {03,08}
J4 30 I_42 H4 {03,08}
J5 32 I_41 H5 {03,08}
J6 34 I_40 H6 {03,08}
J7 36 I_39 H7 {03,08}
J8 38 I_38 H8 {02,05,07,08}
Double Hits
K0 84 I_37 DH0 {03,08}
K1 19 I_36 DH1 {03,08}
K2 27 I_35 DH2 {03,08}
K3 29 I_34 DH3 {03,08}
K4 31 I_33 DH4 {03,08}
K5 33 I_32 DH5 {03,08}
K6 35 I_31 DH6 {03,08}
K7 37 I_30 DH7 {03,08}
K8 39 I_29 DH8 {02,08}
FLAG15 I_197 58 * FLG15 {08}
Data Bus
OE {04} X15 {02} D15 {09} 83 I_54 M15
OE {04} X14 {02} D14 {09} 82 I_53 M14
OE {04} X13 {02} D13 {09} 81 I_52 M13
OE {04} X12 {02} D12 {09} 80 I_51 M12
OE {04} X11 {02} D11 {04,09} 79 I_50 M11
OE {04} X10 {02} D10 {08,09} 78 I_49 M10
OE {04} X9 {02} D9 {05,09} 77 I_48 M9
OE {04} X8 {02} D8 {05,09} 76 I_47 M8
OE {04} X7 {03} D7 {04,07,09} 75 I_62 M7
OE {04} X6 {03} D6 {04,07,09} 74 I_61 M6
OE {04} X5 {03} D5 {04,07,09} 73 I_60 M5
OE {04} X4 {03} D4 {04,06,07,09} 72 I_59 M4
OE {04} X3 {03} D3 {04,06,09} 71 I_58 M3
OE {04} X2 {03} D2 {04,06,09} 70 I_57 M2
OE {04} X1 {03} D1 {04,06,09} 69 I_56 M1
OE {04} X0 {03} D0 {04,05,06,09} 68 I_55 M0
AUX1 {02,09} * I_198 60 AX1
F15 {02,05,07,08} 59 I_178 AX2
TP {07} 11 I_182 CTRL
RBLP {04,08} 10 I_83 RBLIP
RED* {07} 9 I_80 RLED
GRN* {07} 8 I_82 GLED
GATE {03,04} 55 I_81 PGATE
INT {03,05} 15 I_79 IRQ
TTST {03,07} 14 I_76 THTEST
GTST {03,07} 13 I_78 GTTEST
FGATE {03,04} 40 I_77 TFGATE
WS1 {06} 41 I_75 AW1
WS0 {06} 45 I_72 AW0
DS1 {03,06} 46 I_74 AD1
DS0 {03,06} 47 I_73 AD0
CH2 {03,06} 48 I_71 AC2
CH1 {03,06} 49 I_68 AC1
CH0 {03,06} 50 I_70 AC0
CSM* {06} 51 I_69 ACS
CCLEAR {04} 52 I_67 CLRCTR
POS* {04} 54 I_64 TPE*
ET8 {07} 12 I_66 TTEST
ZAP {08} * 56 I_193 ZAPALL
DEVICE: LATTICE 1032E-70LJ/PLCC84
HIGHLAND TECHNOLOGY INC
V680T CONTROL CHIP
22S683 REV T
TRIUMF Mods (*)
Name: VE
Sh 01 of 09
Date: 1998-04-20 11:43:14



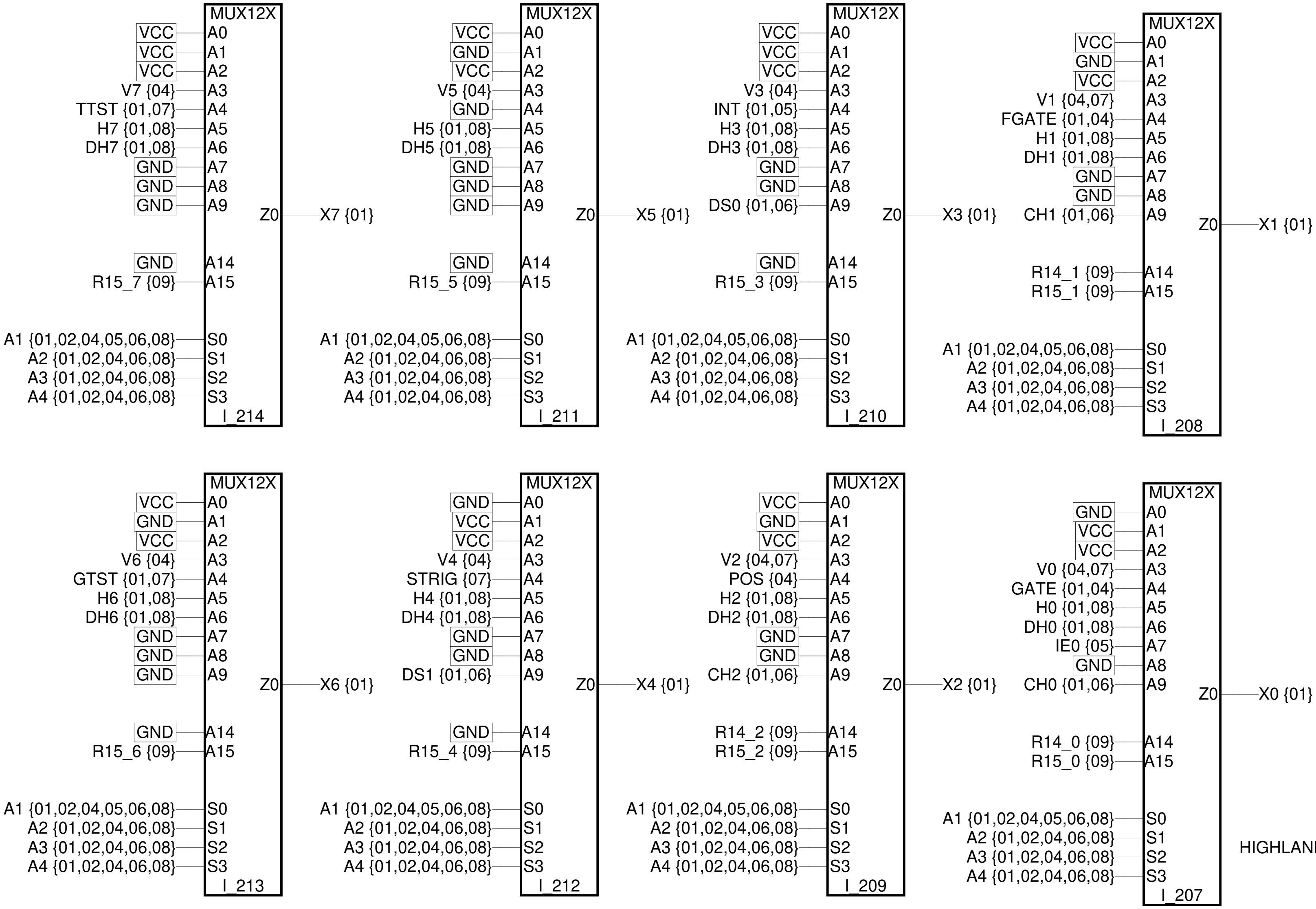

| Register | Function |
|---|---|
| 0 | VXI Mfr |
| 1 | VXI type |
| 2 | VXI sts |
| 3 | Vector |
| 4 | Control |
| 5 | Hit |
| 6 | Double Hit |
| 7 | Int Enable |
| 8 | Resets |
| 9 | Rd Select |
| 10 | T0 MS time |
| 11 | T1 Mid time |
| 12 | T2 LS time |
| 13 | |
| 14 | U1 Mid time |
| 15 | U2 LS time |

READ DATA

MULTIPLEXERS

HIGHLAND TECHNOLOGY INC
V680T CONTROL CHIP
22S683 REV T
TRIUMF version

Name: VE Sh 02 of 09 Date: 1998-04-20 11:43:14




VXI type 0x5899

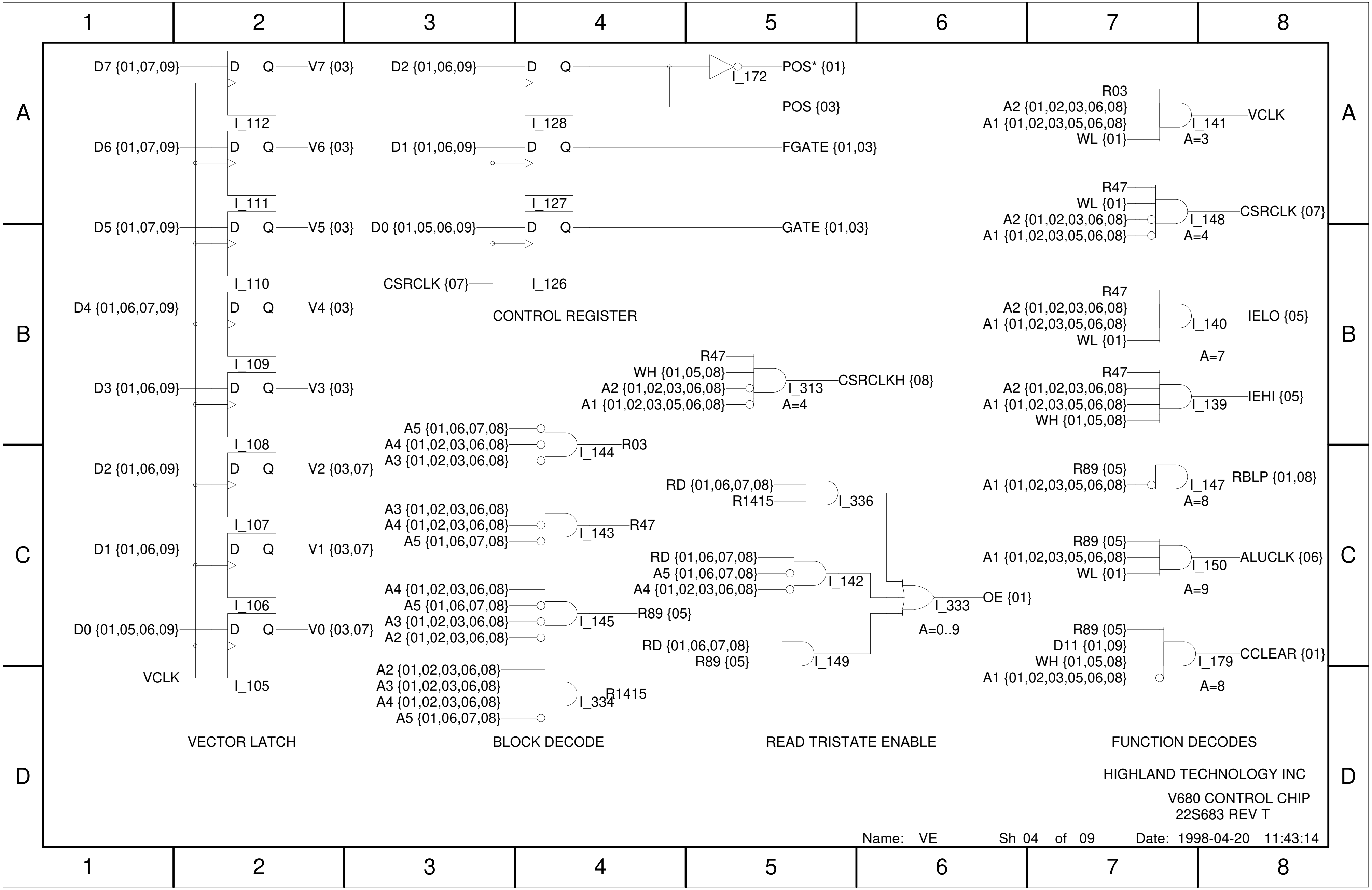
(TRIUMF)

READ DATA

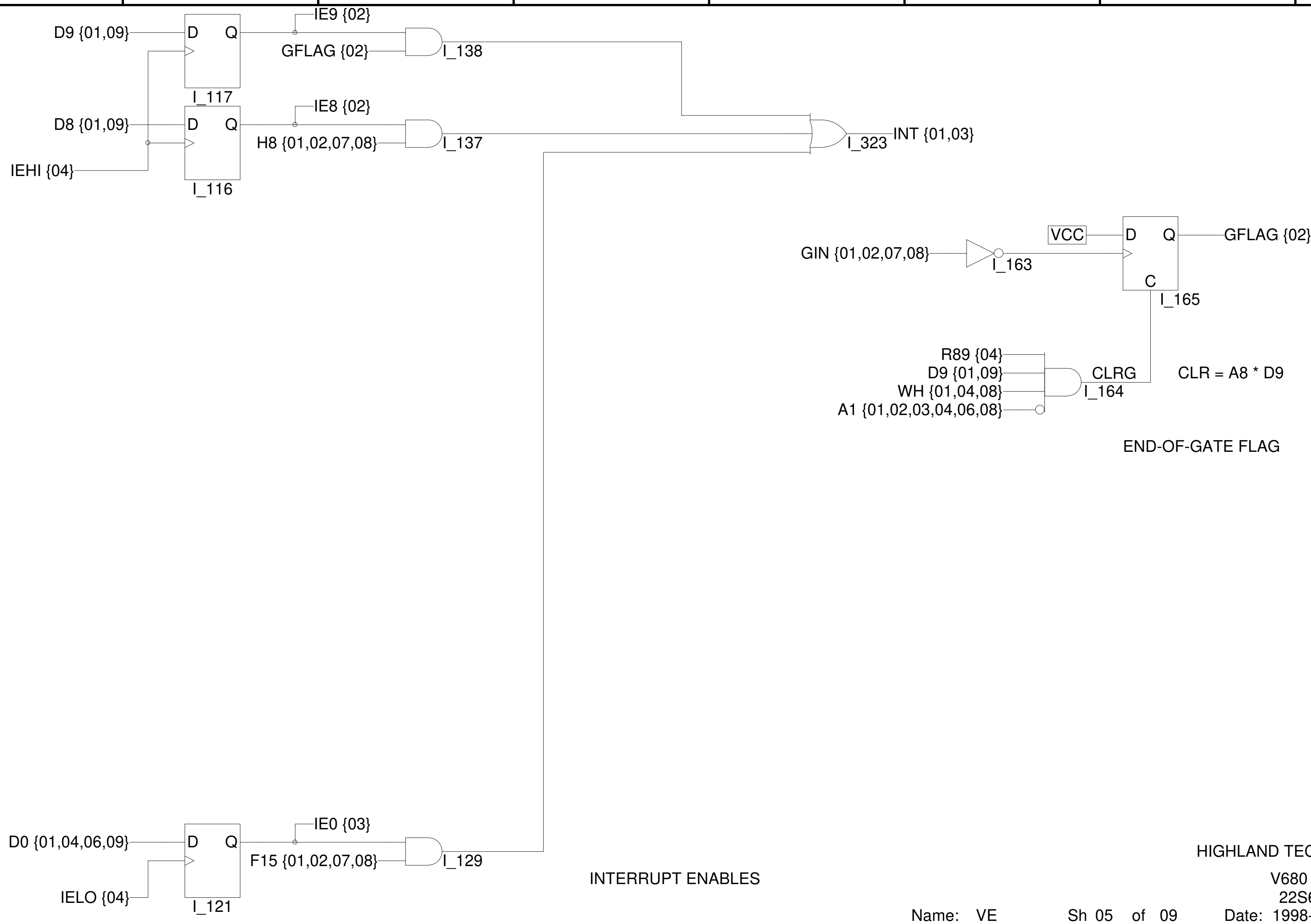
MULTIPLEXERS

HIGHLAND TECHNOLOGY INC
V680T CONTROL CHIP
22S683 REV T
TRIUMF Version

Name: VE Sh 03 of 09 Date: 1998-04-20 11:43:14



D7 {01,07,09}
D Q
V7 {03}
I_112
D6 {01,07,09}
V6 {03}
I_111
D5 {01,07,09}
V5 {03}
I_110
D4 {01,06,07,09}
V4 {03}
I_109
D3 {01,06,09}
V3 {03}
I_108
D2 {01,06,09}
V2 {03,07}
I_107
D1 {01,06,09}
V1 {03,07}
I_106
D0 {01,05,06,09}
V0 {03,07}
VCLK
I_105
VECTOR LATCH
D2 {01,06,09}
I_128
I_172
POS* {01}
POS {03}
D1 {01,06,09}
I_127
FGATE {01,03}
D0 {01,05,06,09}
I_126
GATE {01,03}
CSRCLK {07}
CONTROL REGISTER
R47
WH {01,05,08}
A2 {01,02,03,06,08}
A1 {01,02,03,05,06,08}
I_313
A=4
CSRCLKH {08}
A5 {01,06,07,08}
A4 {01,02,03,06,08}
A3 {01,02,03,06,08}
I_144
R03
A3 {01,02,03,06,08}
A4 {01,02,03,06,08}
A5 {01,06,07,08}
I_143
R47
A4 {01,02,03,06,08}
A5 {01,06,07,08}
A3 {01,02,03,06,08}
A2 {01,02,03,06,08}
I_145
R89 {05}
A2 {01,02,03,06,08}
A3 {01,02,03,06,08}
A4 {01,02,03,06,08}
A5 {01,06,07,08}
I_334
R1415
BLOCK DECODE
RD {01,06,07,08}
R1415
I_336
RD {01,06,07,08}
A5 {01,06,07,08}
A4 {01,02,03,06,08}
I_142
RD {01,06,07,08}
R89 {05}
I_149
I_333
A=0..9
OE {01}
READ TRISTATE ENABLE
R03
A2 {01,02,03,06,08}
A1 {01,02,03,05,06,08}
WL {01}
I_141
A=3
VCLK
R47
WL {01}
A2 {01,02,03,06,08}
A1 {01,02,03,05,06,08}
I_148
A=4
CSRCLK {07}
R47
A2 {01,02,03,06,08}
A1 {01,02,03,05,06,08}
WL {01}
I_140
A=7
IELO {05}
R47
A2 {01,02,03,06,08}
A1 {01,02,03,05,06,08}
WH {01,05,08}
I_139
IEHI {05}
R89 {05}
A1 {01,02,03,05,06,08}
I_147
A=8
RBLP {01,08}
R89 {05}
A1 {01,02,03,05,06,08}
WL {01}
I_150
A=9
ALUCLK {06}
R89 {05}
D11 {01,09}
WH {01,05,08}
A1 {01,02,03,05,06,08}
I_179
A=8
CCLEAR {01}
FUNCTION DECODES
HIGHLAND TECHNOLOGY INC
V680 CONTROL CHIP
22S683 REV T
Name: VE
Sh 04 of 09
Date: 1998-04-20 11:43:14

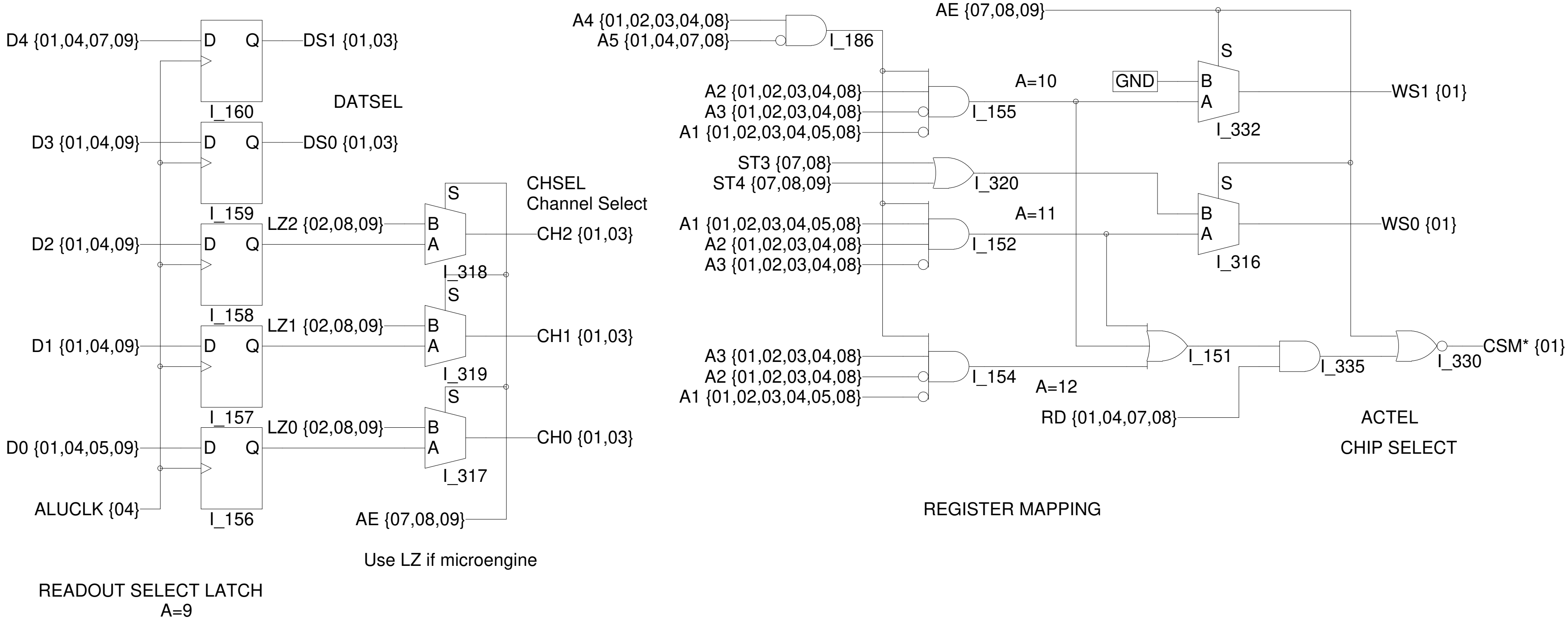



HIGHLAND TECHNOLOGY INC

V680 CONTROL CHIP

22S683 REV T

Name: VE    Sh 05 of 09    Date: 1998-04-20 11:43:14




ACTEL REGISTER MAPPING

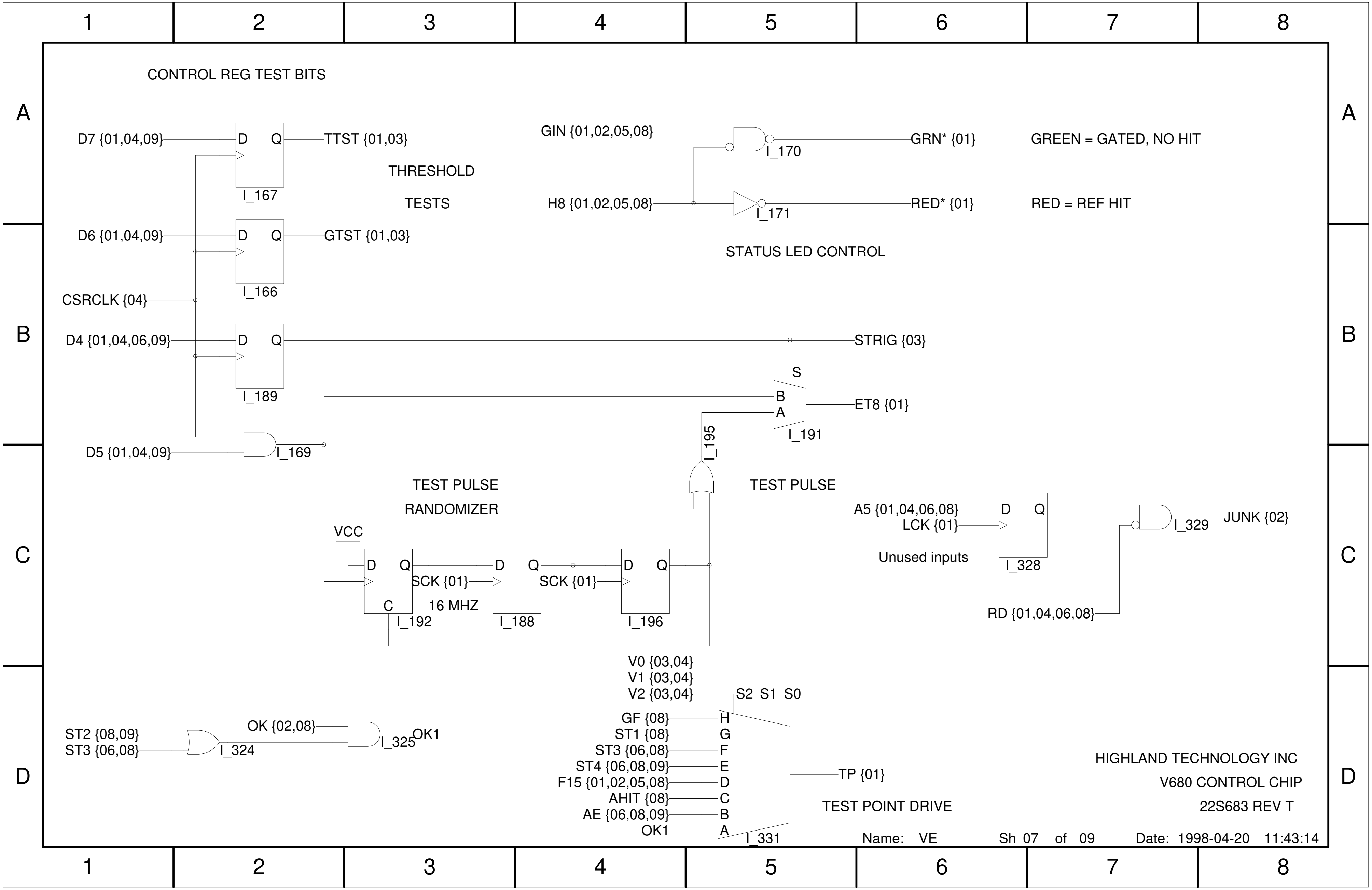
| DATSEL | FUNCTION |
|---|---|
| 0 | Relative TIme |
| 1 | Timestamp |
| 2 | Timestamp, CH8 |
| 3 | Master Counter |

| VMEREG | A5 | A4 | A3 | A2 | A1 | WS1 | WS0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| 10 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | MS TIME |
| 11 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | MID TIME |
| 12 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | LS TIME |

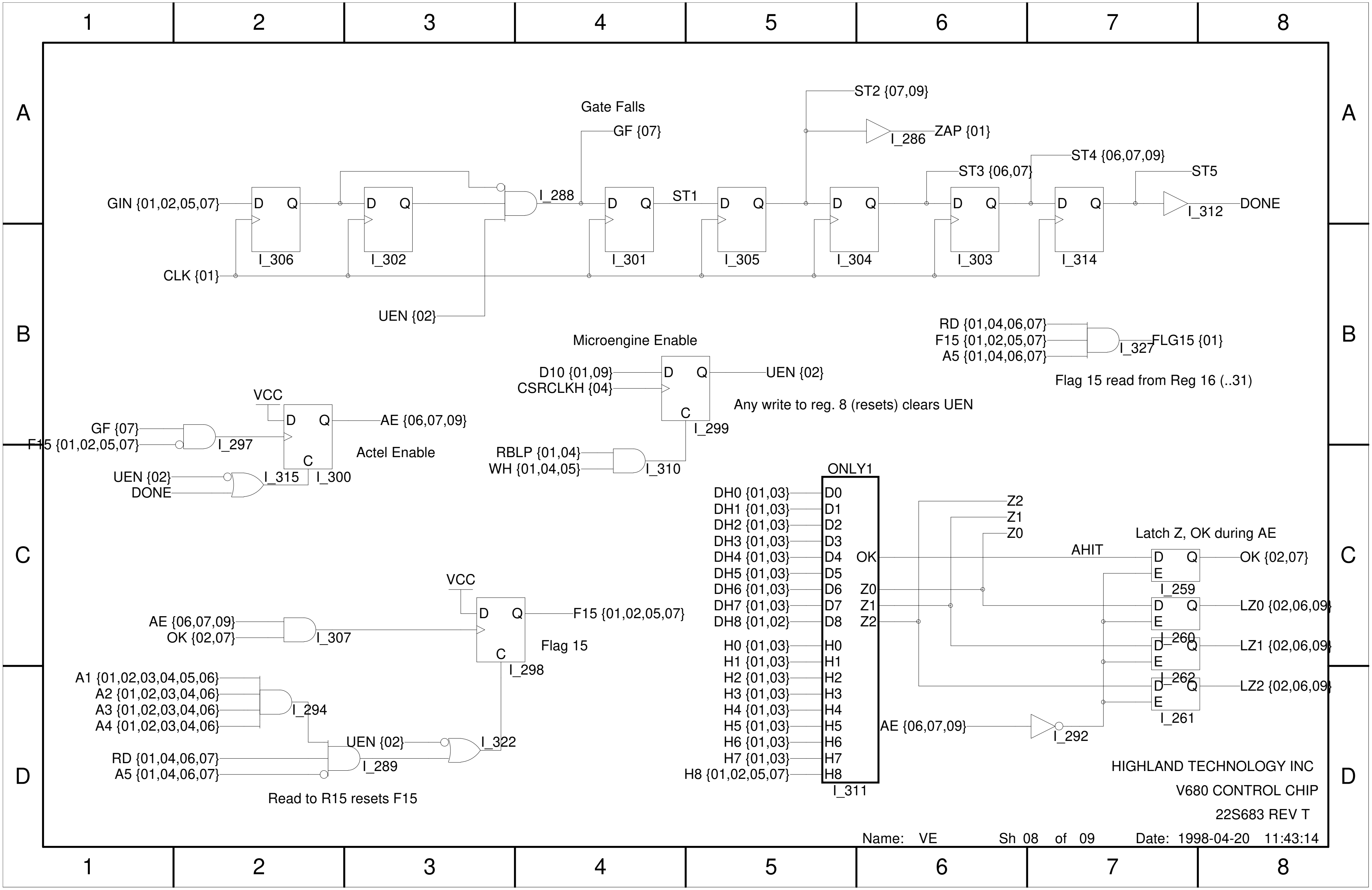
ALU CHIP CONTROL

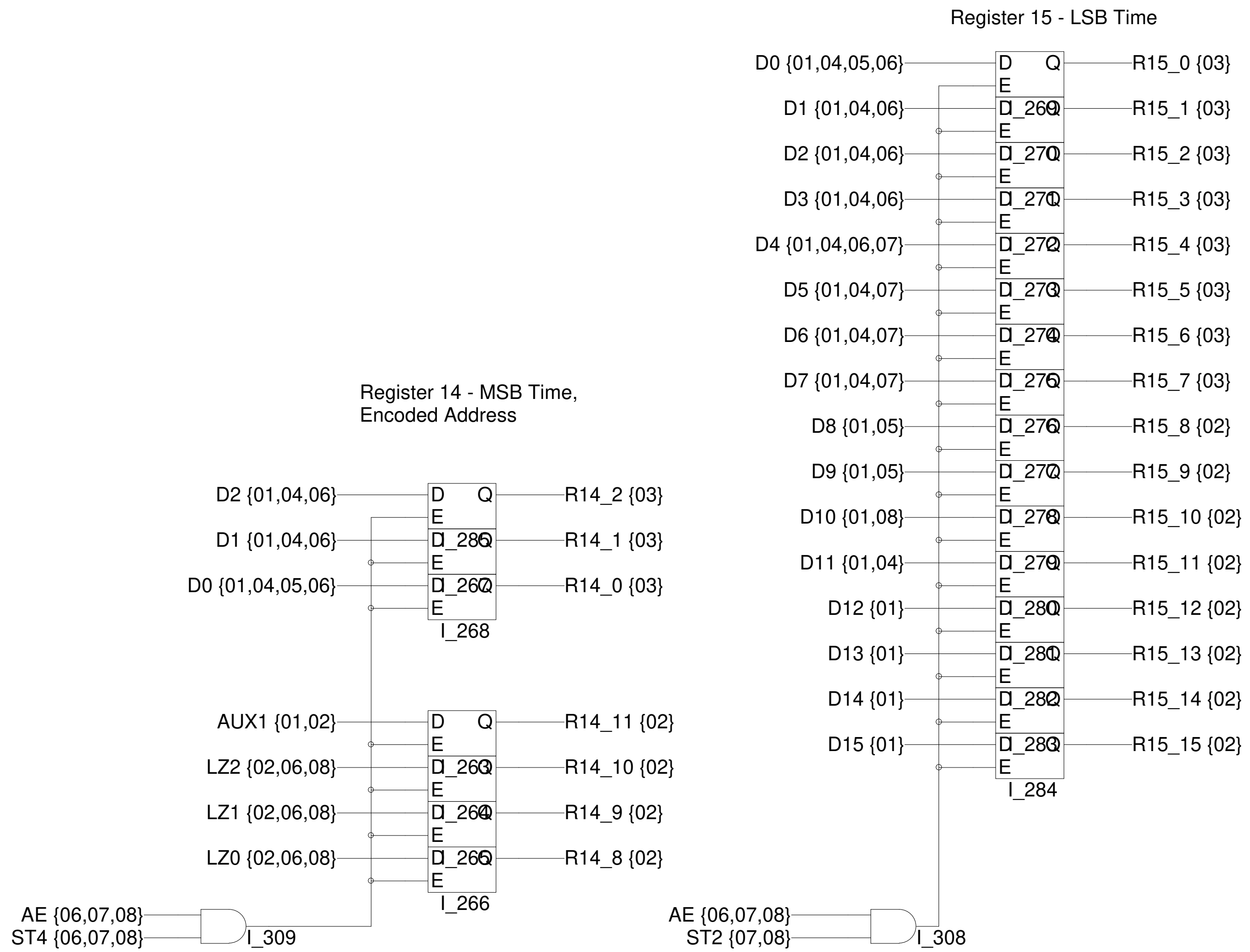
HIGHLAND TECHNOLOGY INC
V680 CONTROL CHIP
22S683 REV T

Name: VE Sh 06 of 09 Date: 1998-04-20 11:43:14



CONTROL REG TEST BITS
D7 {01,04,09}
D
Q
TTST {01,03}
I_167
THRESHOLD
TESTS
D6 {01,04,09}
GTST {01,03}
I_166
CSRCLK {04}
D4 {01,04,06,09}
STRIG {03}
I_189
S
B
A
ET8 {01}
I_191
D5 {01,04,09}
I_169
I_195
GIN {01,02,05,08}
GRN* {01}
I_170
GREEN = GATED, NO HIT
H8 {01,02,05,08}
RED* {01}
I_171
RED = REF HIT
STATUS LED CONTROL
TEST PULSE
RANDOMIZER
TEST PULSE
VCC
SCK {01}
SCK {01}
C
16 MHZ
I_192
I_188
I_196
A5 {01,04,06,08}
LCK {01}
Unused inputs
I_328
JUNK {02}
I_329
RD {01,04,06,08}
V0 {03,04}
V1 {03,04}
V2 {03,04}
S2
S1
S0
GF {08}
ST1 {08}
ST3 {06,08}
ST4 {06,08,09}
F15 {01,02,05,08}
AHIT {08}
AE {06,08,09}
OK1
H
G
F
E
D
C
B
A
TP {01}
TEST POINT DRIVE
I_331
ST2 {08,09}
ST3 {06,08}
I_324
OK {02,08}
I_325
OK1
HIGHLAND TECHNOLOGY INC
V680 CONTROL CHIP
22S683 REV T
Name: VE
Sh 07 of 09
Date: 1998-04-20 11:43:14


Gate Falls
GF {07}
GIN {01,02,05,07}
CLK {01}
UEN {02}
I_306
I_302
I_288
I_301
ST1
I_305
I_304
I_303
I_314
ST2 {07,09}
ZAP {01}
I_286
ST3 {06,07}
ST4 {06,07,09}
ST5
I_312
DONE
RD {01,04,06,07}
F15 {01,02,05,07}
A5 {01,04,06,07}
I_327
FLG15 {01}
Flag 15 read from Reg 16 (..31)
Microengine Enable
D10 {01,09}
CSRCLKH {04}
UEN {02}
I_299
Any write to reg. 8 (resets) clears UEN
RBLP {01,04}
WH {01,04,05}
I_310
VCC
GF {07}
F15 {01,02,05,07}
I_297
AE {06,07,09}
Actel Enable
UEN {02}
DONE
I_315
I_300
ONLY1
DH0 {01,03}
DH1 {01,03}
DH2 {01,03}
DH3 {01,03}
DH4 {01,03}
DH5 {01,03}
DH6 {01,03}
DH7 {01,03}
DH8 {01,02}
H0 {01,03}
H1 {01,03}
H2 {01,03}
H3 {01,03}
H4 {01,03}
H5 {01,03}
H6 {01,03}
H7 {01,03}
H8 {01,02,05,07}
I_311
Z2
Z1
Z0
AHIT
Latch Z, OK during AE
OK {02,07}
I_259
LZ0 {02,06,09}
I_260
LZ1 {02,06,09}
I_262
LZ2 {02,06,09}
I_261
AE {06,07,09}
I_292
VCC
AE {06,07,09}
OK {02,07}
I_307
F15 {01,02,05,07}
Flag 15
I_298
A1 {01,02,03,04,05,06}
A2 {01,02,03,04,06}
A3 {01,02,03,04,06}
A4 {01,02,03,04,06}
I_294
UEN {02}
I_322
RD {01,04,06,07}
A5 {01,04,06,07}
I_289
Read to R15 resets F15
HIGHLAND TECHNOLOGY INC
V680 CONTROL CHIP
22S683 REV T
Name: VE
Sh 08 of 09
Date: 1998-04-20 11:43:14




HIGHLAND TECHNOLOGY INC

V680 CONTROL CHIP

22S683 REV T

Name: VE Sh 09 of 09 Date: 1998-04-20 11:43:14