Berkeley Nucleonics Corporation
Model B980 - 8 Channel VME TDC
Contact factory for complete documentation

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1. GENERAL

The B980 is an eight-channel time measurement module packaged as a single-width, 6U, 16-bit VME module.

2. SPECIFICATIONS

FUNCTION	8-channel time-interval measurement module. Time-of-trigger of eight input channels are measured relative to time-of-trigger of reference channel input. In timestamp mode, all 9 inputs independently report trigger time stamps.
CONFORMANCE	Conforms with ANSI/IEEE 1014-1987 VMEbus spec; Meets VXIC VXI spec rev 1.4 for 'B'-size VXI module
PACKAGING	single-wide 6U Eurocard
DEVICE TYPE	16-bit VME register-based slave: A16:D16:D08(EO); implements 32 16-bit registers at or above C000h in the VME short addressing space.
INPUTS	Nine channels; 0..7 are standard inputs, ch. 8 is reference One GATE input One CLOCK input/output Two special-purpose TTL-level AUX inputs/outputs
LEVELS	Time inputs 0..8, switch selectable as a group for TTL, ECL, NIM, or user-set thresholds; GATE input is switchable for TTL/ECL/NIM/User. All inputs are switchable for polarity (+-) and termination (50 ohms to GND or Hi-Z) AUX1, AUX2, CLOCK : TTL/HCMOS compatible
RESOLUTION	48.828125 picoseconds/LSB; equivalent to 20.48 GHz clock.
RANGE	48 bits; +- 6871 seconds bipolar or +13,743 s unipolar
JITTER	< 70 ps + timebase jitter, RMS. Internal timebase jitter is less than 1E-9 * measured time.
LINEARITY	Integral, < 1 LSB ; differential, < 1%
TIMEBASE	Internal ovenized crystal oscillator. TC below 2E-9/degC, aging below 1 PPM/year; lockable to external 10 MHz TTL reference or to another B980 or V850 module.
CONNECTORS	LEMO, SMA, or SMB

3. FUNCTIONAL MODEL

The B980 time interval counter module functions as follows:
There are nine input channels, numbered 0 through 8, with channel 8 being considered the 'reference channel' for relative-time measurements. Each channel includes an input discriminator, a 'hit' flip-flop, and a 48-bit time latch.

A single 'master' 48-bit counter drives the inputs of all nine channel time latches. When any channel recognizes a valid trigger event, its hit flip-flop is set and the value in the master counter is copied into the channel latch register and saved as the timestamp of the channel trigger event. The state of the nine hit

flip-flops may be read in the HIT register to indicate which, if any, channels have valid timestamps frozen in their latches.

The master counter consists of a 38-bit, 20 MHz physical counter; time interpolation circuits extend the counter to its full 48-bit dynamic range, with the counter LSB having a weight of 48.828125 picoseconds, corresponding to an equivalent count rate of 20.48 GHz. The full range of the counter is about 13,743 seconds.

The module may be used in either of two timing modes: standard mode and timestamp mode. In standard mode, the event time associated with a hit on channel 8 is considered to be the module reference time, and the time of all hits on channels 0..7 are reported relative to this reference time. The value reported for channels 0..7 is the difference between the channel timestamp and the reference timestamp, in the range of +- 6871 seconds, with a positive difference indicating that the channel trigger happened after the channel 8 reference event. If the channel 0..7 hits are known to happen after the channel 8 trigger, the time difference may be interpreted as a positive value from 0 to 13,742 seconds.
In timestamp mode, the actual timestamp of each channel is reported as the channel's time-of-hit, with all nine channels behaving identically. Here, time is relative to the last time that the master counter was cleared. When each channel is triggered, its hit flag may be observed as an indication that the channel has fresh data; the data may then be read and the channel cleared and rearmed in preparation for a new event.

A positive-only mode is selectable; in this mode, triggers on channels 0..7 are ignored until after a hit is sensed on channel 8. The minimum measurable 'positive only' time is typically 4 nanoseconds.

A double-hit register is provided to indicate when a second active trigger edge is sensed on any input channel while the gate is still true. The time of the first hit is always reported. double-hit resolution is typically 3 nanoseconds. The master counter and time interpolators are driven by an on-board precision 40 MHz ovenized crystal oscillator. This oscillator may be phase-locked to an external 10 MHz system reference clock, to another B980, or to a V850-series digital delay generator, permitting accurate interval or time-stamp measurement across any number of modules and channels. Because of the inherent time uncertainty associated with clearing the master counter in any given module, absolute timestamps between modules may differ considerably; for accurate multi-module time measurements, standard (eg, channel-8-relative) timing mode should be used, with a common external trigger applied to channel 8 of all modules to synchronize their time references to sub-nanosecond precision.
Timestamp mode can be used for accurate period measurements of up to nine independent signals, or may be used to perform up to four independent bipolar start-stop measurements using paired channels.

4. ELECTRICAL INPUTS

The B980 has 12 front-panel input connectors, optionally SMB, SMA, or LEMO coaxial types. Inputs are...

8 / REF	reference (channel 8) input
	0..7 eight channel inputs
GATE	hit enable gate
CLK	clock in/out
AUX1	auxiliary TTL input/output
AUX2	auxiliary TTL input/output

4.1 CHANNEL INPUTS

The REF and 0..7 channel connectors connect to the nine input channel discriminators.
A switch is provided to set the thresholds of channels 0..8 as a group to TTL, ECL, or NIM levels (+1.25, -1.25, and -0.4 volts respectively). The GATE input may be individually selected for TTL/ECL/NIM levels.

Each input is individually switch selectable to be a high impedance or 50-ohm-to-ground termination, and each has a selector switch for positive- or negative-edge input. When the GATE input is switched to the '+' position, a positive GATE input enables hits.

4.2 CLOCK INPUT/OUTPUT

CLK is a TTL-compatible signal. When the module is in internal clock mode, this is a 10 MHz output. When the module is in external clock mode, this is an input, and the internal crystal oscillator will phaselock to a 10 MHz TTL signal applied to this connector. A switch is provided to select clock mode. When the module is used in internal clock mode, the CLK connector is an output. The signal is a 10 MHz square wave at HCMOS levels, source-terminated at 50 ohms. It may be run through a 50 ohm coaxial cable directly to a terminated or unterminated oscilloscope or frequency counter input to verify the presence and frequency of the internal clock. The clock output of one B980 may also be used to drive up to four additional B980 units which are operating in external clock mode, such that the four 'slave' units will phase-lock to the single 'master' clock. Total cable length from the master unit to the should not exceed two feet; if cables need to be longer or drive more loads, a buffer amplifier (such as the model V860) will be required.

If an external 10 MHz clock is used to drive one or more B980 units, the signal may be daisy-chained through up to four B980s, with the signal source and/or.

5. VME REGISTER MAP AND PROGRAMMING

The following is a summary of the VME-accessible registers implemented by the B980-series modules. The module follows VXI conventions, having 32 16-bit registers located in the high 4K of the short VME address space. A dipswitch on the module sets the base address, beginning at C000 hex.
All registers are 16 bits wide. REG # below is the ordinal register numberin decimal; OFFSET is the VMEbus address offset from the module baseaddress, shown in hex. The R/W column indicates whether the register is readable and/or writeable from the VMEbus.

REG NAME	REG#	OFFSET	R/W	FUNCTION
VXI MFR	0	00	R	VXI manufacturer ID : always 65262, FEEE hex
VXITYPE	1	02	R	module type, always 22680, 5989 hex
VXI STS	2	04	R	VXI status register, always FFFF hex
VECTOR	3	06	RW	VME interrupt vector register
CONTROL	4	08	RW	module CONTROL register
HIT	5	0A	R	channel HIT flags register
DBLHIT	6	0C	R	channel double hit flags register
IRQMASK	7	0E	RW	interrupt enable mask register
RESETS	8	10	W	channel/module reset bits
SELECT	9	12	RW	data readout select register
T0	10	14	R	MS 16 bits of time
T1	11	16	R	mid 16 bits of time
T2	12	18	R	LS 16 bits of time

Registers 13-31 are reserved for future use.
Registers are described in detail below. Within each register, bits are numbered 0 (LSB) through 15 (MSB).

5.1 VXI MFR REGISTER : VXI MANUFACTURER'S ID

This register displays the VXI-registered manufacturer's ID code. It always reads as FEEE hex.

5.2 VXITYPE REGISTER : MODULE TYPE

This register displays the module type. It normally reads as 22680 decimal, 5898 hex; special-function modules may display different codes.

5.3 VXI STS REGISTER : VXI STATUS REGISTER

This register always reads all 1's (FFFF hex).

5.4 VECTOR REGISTER

This user-loaded register determines the VMEbus vector asserted during Interrupt cycles. Only the low 8 bits are active. The appropriate value must be loaded before enabling interrupts.

5.5 CONTROL REGISTER

Bits in this register establish module operating modes.

BIT	NAME	FUNCTION
0	GATE	gate/enable bit for inputs 0..8
1	FGATE	forces GATE state true.
2	POS	forces positive time measurement mode
3	IRQFLG	true if interrupt is requested
4	SYNC	if set, the ET8 test is synchronous to local clock
5	ET8	triggers the self-test chain; write-only.
6	GTEST	tests the gate threshold detector
7	TTEST	test threshold detectors 0..8
9	GSTAT	state of the GATE input

Channel hits are enabled if the GATE bit is set and the external GATE input is true. If FGATE is set, the external gate input is ignored and inputs are always enabled.
If the POS bit is set, channels 0..7 can be triggered only AFTER the reference channel, channel 8, is triggered. This insures that measured relative times are always positive. Channels 0..7 are enabled about 3 nanoseconds after channel 8 is triggered.

Bits 4, 5, 6, and 7 are used for module testing. If the module gate is enabled and all channel inputs are in the inactive state, writing a '1' to the ET8 bit will 'fire' all nine channel inputs in sequence, with a channel-to-channel separation of about 1 nanosecond. This trigger is asynchronous to the internal clock so may be used to measure and adjust channel jitter. If the SYNC bit is set, the ET8 trigger is synchronous to the internal clock; this can be useful for certain signal probing applications.
If the channel threshold and gate threshold dipswitches are both set to their NIM positions, all thresholds will be programmed to -0.4 volts. then, if the GTEST bit is set, the gate threshold will change to +0.4 volts; similarly, TTEST will change the channel thresholds to +0.4 volts. These bits may be used to test the gate and channel input discriminator circuits.

Bit 9 indicates the immediate state of the GATE input; a '1' indicates that timing channels are enabled to accept hits. FGATE can force this bit high. Note that GSTAT indicates the logical gate state, not the electrical state; that is, if the gate polarity is selected as negative, hits are enabled when the electrical gate input is negative.

5.6 HIT REGISTER

BIT	NAME	FUNCTION
0..8	HIT n	status of HIT flipflops for channels 0..8; a '1' indicates that the associated channel has been triggered at least once.
9	GATEF LAG	this bit is asserted at the fall of the GATE state, whether GATE was asserted by an external GATE input or by the FGATE control register bit. It is cleared by the GATE FLAG RESET bit in the RESETS register.

5.7 DOUBLEHIT REGISTER

BIT	NAME	FUNCTION
0..8	DHITn	status of DOUBLEHIT flip-flops for channels 0..8; a '1' indicates that the associated channel has been triggered two or more times while the GATE state was true.

5.8 IRQ MASK REGISTER

Bits 0..8 of this register are channel interrupt-enable bits. A VME interrupt request will be generated if

(HITn .and. MASKn) <> 0

that is, if any channel has a hit (indicated by a '1' in the HIT register) and the corresponding mask bit is set, an IRQ will be requested.
Bit 9 enables interrupts at the end of the GATE state, namely when the GATE FLAG bit is true.
Bit 10 enables optional microengine interrupts.

5.9 RESET REGISTER

Bits 0..8 of this register, when written as 1's, clear channels 0..8 respectively. Writing a '1' to any bit clears the HIT flip-flop for that channel and prepares the channel to accept a new event trigger.
Writing a '1' to bit 9 clears the GATE FLAG.
Writing a '1' to bit 10 clears the optional microengine.
Writing a '1' to bit 11 clears the master 48-bit timestamp counter. If the module is used in standard mode, the counter need not ever be cleared. In timestamp mode, users may wish to clear the master counter just prior to expected trigger events such as to keep returned 48-bit timestamp values small, or to avoid dealing with possible 10,995 second time stamp rollovers.
The RESET bits do not latch, and always read back as 0's.

5.10 SELECT REGISTER

The five low bits of this register select the data to be presented in the three time readout registers.
Bit select patterns are...

4	3	2	1	0		
DS1	DS0	CH2	CH1	CH0	Hex	Data selected for readout
0	0	0	0	0	00	Relative time, channel 0
0	0	0	0	1	01	Relative time, channel 1
0	0	0	1	0	02	Relative time, channel 2
0	0	0	1	1	03	Relative time, channel 3
0	0	1	0	0	04	Relative time, channel 4
0	0	1	0	1	05	Relative time, channel 5
0	0	1	1	0	06	Relative time, channel 6
0	0	1	1	1	07	Relative time, channel 7
0	1	0	0	0	08	Timestamp, channel 0
0	1	0	0	1	09	Timestamp, channel 1
0	1	0	1	0	0A	Timestamp, channel 2
0	1	0	1	1	0B	Timestamp, channel 3
0	1	1	0	0	0C	Timestamp, channel 4
0	1	1	0	1	0D	Timestamp, channel 5
0	1	1	1	0	0E	Timestamp, channel 6
0	1	1	1	1	0F	Timestamp, channel 7
1	0	0	0	0	10	Timestamp, channel 8
1	1	0	0	0	18	Counter

5.11 TIME READOUT REGISTERS : T0, T1, T2

The T0, T1, and T2 registers contain time data for the item named in the SELECT register. The three 16-bit registers contain a 48-bit time value, with T0 being the most significant 16 bits and T2 being the least significant. For relative times (select codes 0..7h), this data represents the time DIFFERENCE between the channel's hit time and the hit time of channel 8, the reference time channel. The data is valid only if the selected channel AND channel 8 both have their 'hit' flags set.

For select codes 08..10h, the data represents the timestamp value for channels 0..8. This data is valid only if the channel has a hit.

Select code 18h selects the timestamp counter. The 10 LSBs will always read as zeroes, and the remaining bits will count in real time.

5.12 READING TIME REGISTERS

The SELECT register is used to select which channel is readout in the Tn registers, and whether the data is an absolute time stamp (available for all nine channels) or a relative time (channels 0..7 only).

If a single channel 0..7 has its 'hit' flag set in the STATUS register, its timestamp value may be read in the T0:T1:T2 registers by writing the proper channel timestamp SELECT code. If the reference (channel 8) hit is also asserted, then the channel's relative time value may also be read in T0:T1:T2, after asserting the appropriate SELECT code.

To read a time value for channels 0..7, first check the STATUS register to see if the channel has its HIT flag set. If it is desired to read relative values, verify that the channel 8 HIT flag is set as well. Next, write the proper code into the SELECT register, then read the three 'T' registers. After data is read, the channel may be cleared and rearmed by writing the appropriate RESET register bits.

The 3-word (48 bit) 'TN' value represents the either the value in the 48-bit master timestamp counter effective the instant that the channel was triggered or, if relative time is selected for readout, the 3-word value is the time of channel 0..7 trigger relative to the time of the channel 8 trigger. The net value of a timestamp or relative time is...

T = ((T0 * 65536) + T1) * 65536 + T2

where the 'TN' words are considered to be unsigned 16-bit integers, and the net LSB value is 48.828125 picoseconds. Note that the counter overflows every 2^48 counts, about every 13,743 seconds. For time in seconds, just multiply the computed 'T' value by 48.828125E-12. When measuring relative times, counter overflow may be ignored.

If the channel triggers may occur before or after the reference, the relative time data in the Tn registers must be interpreted as a 48-bit, 2's complement signed integer. Use the formula above, but then, if the MSB of the result is set (e.g., if T exceeds +140,737,488,355,327) then subtract 281,474,976,710,656 from the computed value). Again, the result is in units of 48.8 ps, but here the corrected 'T' represents a time from -6871 to +6871 seconds relative to the reference hit.

To maintain full accuracy within application programs, the 3-word time values should be handled as 64-bit integers or as double-precision floating-point values.

If it is certain that a relative time interval will not exceed 209 milliseconds (+-104 ms in bipolar cases) then the MS time register value (namely the T0 register) can be ignored, and the T1:T2 register pair can be processed as a signed or unsigned 32-bit value.

The reprate of time measurements is limited only by VME bus access speed.

The following PowerBasic code fragment reads channel 5 relative time and converts the data into double-precision floating-point time values TU# (unsigned time) and TS# (signed), both in seconds.

The program assumes that the VME registers are directly accessed as elements of the V() array, as unsigned integers. All program variables are unsigned 16-bit integers except '&&' types which are 64-bit

signed integers and '#' types which are double precision floaters.

```
T0 = BASE + 10                          ' DEFINE TIME REGISTERS RELATIVE
T1 = BASE + 11                          ' TO MODULE BASE ADDRESS. NOTE THAT
T2 = BASE + 12                          ' THESE ARE *WORD* ADDRESSES!
RD = BASE + 9                           ' DEFINE READOUT SELECT REG, TOO.


V(RD) = 5                               ' SELECT CHANNEL 5, RELATIVE TIME


T0D = V(T0)                             ' READ MS TIME,
T1D = V(T1)                             ' MID TIME,
T2D = V(T2)                             ' AND LS TIME AS UNSIGNED 16'S


T&& = T0D                               ' MAKE A COMPOSITE TIME VARIABLE
SHIFT LEFT T&&, 16                      ' 'T&&' IN B980 LSB'S
T&& = T&& + T1D                         '
SHIFT LEFT T&&, 16                      ' (DATA IS 48 BITS, SO WE MUST
T&& = T&& + T2D                         ' DO QUAD-WORD 64-BIT MATH)


TU# = 4.8828125E-11 * T&&               ' FLOAT THAT, IN SECONDS
' AS 'UNSIGNED TIME'


S&& = T&&                               ' COPY 48-BIT STUFF AND


IF (S&& AND &H400000000000)THEN         ' SIGN EXTEND TO SIGNED
S&& = (S&& OR &HFFFF400000000000)       ' 64-BIT INTEGER!
END IF


TS# = 4.8828125E-11 * S&&               ' FLOAT THAT, IN SECONDS
                                        ' (LSB IS WORTH 48.8 PICOSECONDS)
```

5.13 INTERRUPTS

The B980 uses the RORA (reset on register access) VME interrupt mechanism. Internal to the module, all bits of the INTERRUPT ENABLE register are logically ANDed with corresponding bits of the HIT register. If any bit pair and's to 1 (e.g., any pair of bits is 1:1) then the IRQ state is true. If interrupts are enabled by the IRQ dipswitch, the IRQ state asserts and holds one of the seven available VME interrupt request lines until the IRQ state is cleared by the user's interrupt service routine. Note this is a static (rather than a edge-triggered) interrupt system.

The GATE FLAG may be enabled to generate interrupts by setting bit 9 of the interrupt enable register. In this case, an interrupt will be requested at the end of the channel-enable gate.
To enable interrupts,

1. Set the IRQ dipswitch to the desired interrupt level, 1 to 7. Selecting level 0 will disable interrupts. Level 7 is often an NMI to the host processor and should not be used here.
2. Write the desired IRQ vector number into the VECTOR register.

3. Assert the desired bits in the INTERRUPT ENABLES register.

An interrupt service routine must run at a priority level sufficiently high that it cannot be re-interrupted by the module. The ISR must take actions to clear the interrupting condition (typically, it reads out and resets channels having hits) before exiting.

5.14 MICROENGINE

The B980 has a optional custom microengine capability that may be useful in high data rate applications. An internal programmable gate array may be configured to perform simple internal sequencing, data routing, and buffering operations. The microengine can qualify or discard certain events, automatically reset channel hits, and store and buffer 'good event' data. Contact the factory for more information on the capabilities of this option.

For the complete manual please contact the factory.