CBD 8210
CAMAC Branch Driver
User's Manual
Version 1.0

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CREATIVE ELECTRONIC SYSTEMS S.A.

Chapter 1

INTRODUCTION

1.1. Overview

This Module, type CBD 8210, is a double height VME card allowing a CAMAC Branch (EUR 4600) to be driven from VME. This means that up to 7 CAMAC crates, on the same branch highway, can be accessed from VME. The use of PALs and I.C.s in the mechanical SO format makes it a high performance module. The design of this module has been made with the intention of allowing it to work in conjunction with a second module enabling DMA transfers to be made from CAMAC to VME.

The module is an update of the CAMAC Branch Driving VME module developed by the French Research Institute at SACLAY. The characteristics are the following:

a) Programmable 16-bit or 24-bit transfers.
b) Two external interrupts with handshake.
c) Comprehensive LAM handling.
d) Addition of a DMA module at a later date.
e) Complete monitoring of all transfers displayed on the front panel.
f) Multi-crate addressing possible.

1.2. Address Mapping

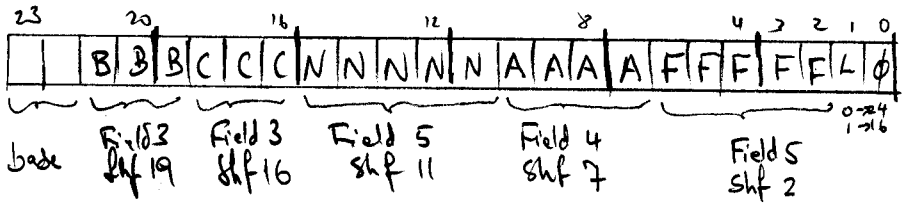
The mapping of the CAMAC address field has been taken from the CERN publication "CERN IMPLEMENTATION RECOMMENDATION for MC 68000 BASED CAMAC PORT CONTROLLERS'. Therefore, for the 24-bit address of VME the following bit allocation exists:

Bits <23..22>	=	1..0
Bits <21..19>	=	Branch address (0 to 7 = 8 branches)
Bits <18..16>	=	Crate address 1 - 7 standard addressing.
Bits <15..11>	=	N address - CAMAC station number
Bits <10..07>	=	A address - CAMAC sub-address
Bits <06..02>	=	F code - CAMAC function
Bit <01>	=	CAMAC Word length 0 = 24-bit 1 = 16-bit

Thus all the CAMAC system parameters are mapped onto the VME address field.

The CBD 8210 can only drive one CAMAC branch where the number of the branch to be driven is selected by a front panel switch.

In practice, when a cycle of 24 bits is to be carried out, the master effects a first cycle with AD01 = 0 (detection of a 24-bit cycle) followed by a cycle with AD01 = 1 allowing the utilization of the instructions 'LWORD' of the MC 68000.



1.3. Selection of Internal Registers

The internal registers are selected by using the command CR0 N29. They are as follows:

CSR	:	CR0 N29 A0 F0	Read/Write	
ITF	:	CR0 N29 A0 F4	Write	
INT. CONT.1	:	CR0 N29 A0 F5	Read/Write	Control
INT. CONT.1	:	CR0 N29 A0 F1	Read/Write	Data
INT. CONT.2	:	CR0 N29 A0 F6	Read/Write	
INT. CONT.2	:	CR0 N29 A0 F2	Read/Write	
INT. CONT.3	:	CR0 N29 A0 F7	Read/Write	
INT. CONT.3	:	CR0 N29 A0 F3	Read/Write	
CAR	:	CR0 N29 A0 F8	Read/Write	
BTB	:	CR0 N29 A0 F9	Read	
BZ	:	CR0 N29 A0 F9	Write	
GL	:	CR0 N29 A0 F10	Read	

Chapter 2

INTERNAL REGISTERS

2.1. Control & Status Register - CSR

This read/write register contains all the information necessary to enable the correct functioning of the CBD 8210. It is formatted as follows:

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Q	X	TO	BD	MNOX	SY5	SY4	SY3	SY2	SY1	MTO	MLAM	MIT2	MIT4	IT2	IT4

0x8000 0x4000

INIT = Power-up + SYSRESET

Definition of Bit Allocation:

<15> Q — Status of Q during the last CAMAC cycle. Read only.

<14> X — Status of X during the last CAMAC cycle. Read only.

<13> TO — Time-out status flag of the last CAMAC cycle. Read only.

<12> BD — CAMAC branch demand - transparent read of branch highway. Read only.

<11> MNOX — no X mask. Allows masking of the BERR when the CAMAC cycle with X = 0.
MNOX = 1 NOX gives DTACK
MNOX = 0 NOX gives BERR
Read/write INIT = 1

<10..06> SY5..SY1 — Identification SY1 and SY2 monitored on the front panel.
Read/write INIT = 0

<05> MTO — Time-out mask. Allows removal of internal time-out.
MTO = 1 No time-out on board.
MTO = 0 time-out active.
Read/write INIT = 1

<04> MLAM — Interrupt mask for level 3 VME of the control of GLAM. It suppresses also the automatic scanning of BG on BD = 1.
Read/write INIT = 1

<03..02> MIT2,4 — Mask for the external interrupts.
Read/write INIT = 1

<01..00> IT2,4 — External interrupt flags give O/P on ACK Lemos.
Read only INIT = 0

The bits <00..01> - IT2, IT4 - are read only in the CSR register in order to prevent the erasure of interrupts.

2.2. Interrupt Flag Register - IFR

This register is write only and allows to set or reset the external interrupts by software. See chapter on external interrupts.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
-	-	-	-	-	-	-	-	-	-	-	-	-	-	IT2	IT1

2.3. Interrupt Controller Registers - ICR

These registers correspond to the internal registers of the AMD 9519. Each interrupt controller consists of two registers - one for DATA and one for CONTROL.

For a more detailed explanation see the section on LAM handling and the data sheet on the 9519A.

2.4 Crate Address Register - CAR

This register is used for multiple addressing of the crates on the CAMAC branch and allows selection of the crates required for this action.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Do not care								CR7	CR6	CR5	CR4	CR3	CR2	CR1	-

INIT = ?

Read/write.

N.B.: The CAR must not be READ when GL Scanning is ACTIVE.

2.5. BTB Registers - BTB

This register contains all the information regarding which crates in the branch are ON LINE. In addition, it removes the ambiguity of time-out.

This register is also used to generate the BG cycles and is 'read only'.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Do not care								BTB7	BTB6	BTB5	BTB4	BTB3	BTB2	BTB1	0

2.6. BZ Generation

The generation of BZ (reset CAMAC branch) is done by a write cycle to the address of the BTB register. The signal BZ is active for a period of approximately 15 µs.

BZ can also be generated by the front panel push button.

2.7. GL Register

In order to facilitate the use of this module the possibility to carry out BG cycles under program control has been included. During a read of this register the CBD 8210 carries out a standard CAMAC branch cycle using the BTB register to select the ON LINE crates. The logic of the 24-bit word is identical to the read CAMAC cycles.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
GL16	GL15	GL14	GL13	GL12	GL11	GL10	GL09	GL08	GL07	GL06	GL05	GL04	GL03	GL02	GL01

T=1

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	GL24	GL23	GL22	GL21	GL20	GL19	GL18	GL17

T=0

2.8. Address Modifier

Decoding of the address modifier is carried out by means of a PROM 24S10 and is therefore user programmable. (See explanatory note).

To reprogram the address modifier decoder:

A0 = AM0

A1 = AM1

A2 = AM2

A3 = AM3

A4 = AM4

A5 = AM5

A6 = 0

A7 = 0

Qo = AMOK

Standard VME AM decoded : 3D, 39.

Chapter 3

CAMAC TRANSFERS

3.1. Types of Transfer

The three types of transfer are separated inside the card. They are as follows:

READ function : F0 to F7

WRITE function : F16 to F23

COMMAND functions : F8 to F15 & F24 to F31

READ functions are executed by : MOV (CAMAC), (EA) cycle VME.

WRITE functions are executed by : MOV (EA), (CAMAC) cycle VME.

COMMAND functions are executed by : MOV (CAMAC), (EA) cycle VME
TST (CAMAC) cycle VME

For COMMAND functions the value of the CSR is transmitted during a READ cycle.

For an incorrect CAMAC cycle, e.g. VME WRITE with F0 A0, the CBD 8210 completes the cycle with DTACK but the CAMAC cycle is not executed.

3.2. Control and Execution of CAMAC Cycles

When a correct CAMAC cycle (R/W) is sent from VME, the decoding logic sends a CAMAC REQUEST to the CAMAC sequencer. From this moment the sequencer starts to get access to the branch by:

1. Generating BCR, BN, BF, (DATA) BA
2. Generating BTA.
3. Waiting until all the crates addressed generate their BTBs.
4. Confirming that VME cycle can complete.
5. Completing the CAMAC cycle.

The CBD 8210 finishes the VME handshake at the moment when all the BTBs are in a '1' state (called S1 in the CBD 8210). The logic of the beginning and the end of the cycle is included for multi-crate addressing.

The DATA are separated for READ and WRITE to eliminate overlap and not to stretch the length of the VME bus cycles.

In addition, the PAL-sequencer, controlling the CAMAC branch cycle, is protected against corruption in the event of a new branch cycle being requested before the end of the current cycle.

Multi-addressing is executed with the crate address code CR0. In such a case the crates addressed are those currently stored in the CAR.

For 16-bit CAMAC transfers (both READ and WRITE) the data are transmitted in a pseudo-transparent manner. The variables CR, N, F, A are stored at the start of each CAMAC cycle.

3.3. CAMAC Status Information

The CAMAC status bits Q, X and TO are updated during each CAMAC cycle. At the beginning of each cycle, the internal memory for these bits is reset. The values of Q and X are memorized at the moment of the internal S1 (all BTBs at 1). The generation of BERR due to the absence of X depends on the mask MNOX (MNOX =1 cause no BERR if X=0). In all other cases the CBD 8210 replies with DTACK.

3.4. CAMAC Time-out

For each CAMAC cycle a time-out circuit is triggered IF the mask MTO=0. In the event that the circuit timing is out before completion of the current CAMAC cycle the VME handshake is completed with BERR and the CAMAC branch cycle is aborted with the TO flip flop being set. The duration of the time-out circuit can be selected by jumpers. The value selected can be between 2 µs and 134 s. See section on jumper settings.

3.5. 24-bit CAMAC Transfers

24-bit CAMAC transfers are treated in the same way as with 32-bit 68000 transfers. Also, from the software point of view, 24-bit transfers are pseudo-transparent. From a hardware point of view, LWORD is realized in two steps:

1. Cycle with AD01 = 0 high word

2. Cycle with AD01 = 1 low word

Thus, for 24-bit READ and WRITE CAMAC cycles each type of transfer is carried out in a different way:

24-bit READ:	T=0	Branch cycle with transparent read of bits 16 to 23.
	T=1	Read bits 0 to 15 from the temporary register.
24-bit WRITE:	T=0	Store bits 16 to 23 in the temporary register.
	T=1	Branch cycle with transparent write of bits 0 to 15 plus bits 16 to 24 from the temporary register.

For COMMAND functions the CBD 8210 only accepts these under the condition T = 1.

N.B.: On 24-bit READ the bits 24 to 31 are set to 0.

3.6. GL Cycles

Two types of GL cycles exist in the CBD 8210:

1) Automatic scan for interrupt level 3.

2) Programmed cycle.

Automatic scan cycles are discussed in the section on interrupts.

Programmed cycles are similar to a CAMAC read. For this cycle, the crate addresses are those crates given by the BTB register.

e.g. MOVE.W(GL),(EA)

The 24-bit transfer (LWORD) is treated in the same way as a 24-bit CAMAC read

e.g. MOVE.L(GL),(EA)

Chapter 4

INTERRUPTS

4.1. General Information

The CBD 8210 contains an interrupt structure at several levels as follows:

- Two external interrupts on levels 2 and 4.
- One internal interrupt for LAM handling on level 3.

Each source of interrupt can be masked separately. The interrupt vector for levels 2 and 4 can be selected by jumpers and for level 3 by software. The interrupt logic corresponds to the VME standard revision B with a transit-time of the daisy chain of 40 ns.

Initialization sets the interrupt masks to '1' and the interrupt flags are cleared.

4.2. External Interrupts - IT2 and IT4

External interrupts (activated on the negative edge) can be selected for action by either NIM or TTL I/Ps. In addition, there is an ACK O/P allowing a handshake action with the source.

The timing diagram is as follows:

50 ns. max.

Ext. Source

ACK IACK or Int. FF clear.

This method of operation enables external synchronization with the whole interrupt process.

The interrupt flip flop can be SET, RESET and READ by the master, allowing the use of individual masks, as follows:

1. To use the external interrupt inputs for polling.

2. To use the ACK output for external synchronization.

3. To generate interrupts by software.

The vector associated with each external interrupt can be selected by jumper (8 bits) - see the section on jumper settings for vector and NIM/TTL selection.

The use of the input/output sockets INT and ACK allows the connection of a second CBD 8210 on the same branch with a system of handshaking.

4.3. LAM Handling

LAM handling is carried out by three interrupt controllers of type AMD 9519. This choice allows sophisticated GLAM handling with a minimum of hardware. The AMD 9519 is a complicated device, and it is recommended to study carefully the manufacturers data sheet.

The 24 GLAMs are connected to the three AMD 9519s, as follows:

GL1 to GL8 INT. CONTR. 1

GL9 to GL16 INT. CONTR. 2

GL17 to GL24 INT. CONTR. 3
(GL1 has the highest priority)

For correct GLAM handling it is important to use the interrupt controllers, as follows:

Number of BYTE : 1
Interrupt input : negative edge
GINT polarity : negative

4.3.1. GL Scanning

In order to simplify the use of the module the generation of GL cycles is done autonomously and is interleaved with CAMAC cycles. The repetition rate of GL cycles has been set to 10 µs.

The generation of BG cycles is done only if the mask MLAM = 0 and the signal BD is active.

4.3.2. Information on Interrupt Handling.

The three interrupt controllers are connected in series and the priority of the 24 sources of interrupts can be defined by three separate groups. However, group 1 has always a higher priority than group 2 which has a higher one than group 3. The vectors must be programmed before use. It is also possible to carry out interrupt polling by using the internal masks of the AMD 9519s.

It should be noted that in order not to block the action of a higher priority GL, the handling of IRQ3 VME should not stop the generation of BG cycles. Thus it is part of the requirements of the user program that it resets the AMD 9519 interrupt, which has just been handled, to zero.