Table 9-1. VXIbus P2 connector, slot 0.

VXIbus P2/J2 Connector, Slot 0			
Pin Number	Row A	Row B	Row C
1	ECLTRG0	+5 VDC	CLK10+
2	-2V	GND	CLK10-
3	ECLTRG1	RSV1	GND
4	GND	A24	-5.2V
5	MODID12	A25	LBUSC00
6	MODID11	A26	LBUSC01
7	-5.2V	A27	GND
8	MODID10	A28	LBUSC02
9	MODID09	A29	LBUSC03
10	GND	A30	GND
11	MODID08	A31	LBUSC04
12	MODID07	GND	LBUSC05
13	-5.2V	+5 VDC	-2V
14	MODID06	D16	LBUSC06
15	MODID05	D17	LBUSC07
16	GND	D18	GND
17	MODID04	D19	LBUSC08
18	MODID03	D20	LBUSC09
19	-5.2V	D21	-5.2V
20	MODID02	D22	LBUSC10
21	MODID01	D23	LBUSC11
22	GND	GND	GND
23	TTLTRG0*	D24	TTLTRG1*
24	TTLTRG2*	D25	TTLTRG3*
25	+5V	D26	GND
26	TTLTRG4*	D27	TTLTRG5*
27	TTLTRG6*	D28	TTLTRG7*
28	GND	D29	GND
29	RSV2	D30	RSV3
30	MODID	D31	GND
31	GND	GND	+24V
32	SUMBUS	+5 VDC	-24V

Table 9-2. VXIbus P2 connector, slots 1 - 12.

VXIbus P2/J2 Connector, Slots 1 - 12			
Pin Number	Row A	Row B	Row C
1	ECLTRG0	+5 VDC	CLK10+
2	-2V	GND	CLK10-
3	ECLTRG1	RSV1	GND
4	GND	A24	-5.2V
5	LBUSA00	A25	LBUSC00
6	LBUSA01	A26	LBUSC01
7	-5.2V	A27	GND
8	LBUSA02	A28	LBUSC02
9	LBUSA03	A29	LBUSC03
10	GND	A30	GND
11	LBUSA04	A31	LBUSC04
12	LBUSA05	GND	LBUSC05
13	-5.2V	+5 VDC	-2V
14	LBUSA06	D16	LBUSC06
15	LBUSA07	D17	LBUSC07
16	GND	D18	GND
17	LBUSA08	D19	LBUSC08
18	LBUSA09	D20	LBUSC09
19	-5.2V	D21	-5.2V
20	LBUSA10	D22	LBUSC10
21	LBUSA11	D23	LBUSC11
22	GND	GND	GND
23	TTLTRG0*	D24	TTLTRG1*
24	TTLTRG2*	D25	TTLTRG3*
25	+5V	D26	GND
26	TTLTRG4*	D27	TTLTRG5*
27	TTLTRG6*	D28	TTLTRG7*
28	GND	D29	GND
29	RSV2	D30	RSV3
30	MODID	D31	GND
31	GND	GND	+24V
32	SUMBUS	+5 VDC	-24V

Table 9-3. VXIbus P3 connector, slot 0

VXIbus P3/J3 Connector, Slot 0			
Pin Number	Row A	Row B	Row C
1	ECLTRG2	+24V	+12V
2	GND	-24V	-12V
3	ECLTRG3	GND	RSV4
4	-2V	RSV5	+5V
5	ECLTRG4	-5.2V	RSV6
6	GND	RSV7	GND
7	ECLTRG5	+5V	-5.2V
8	-2V	GND	GND
9	STARY12+	+5V	STARX01+
10	STARY12-	STARY01-	STARX01-
11	STARX12+	STARX12-	STARY01+
12	STARY11+	GND	STARX02+
13	STARY11-	STARY02-	STARX02-
14	STARX11+	STARX11-	STARY02+
15	STARY10+	+5V	STARX03+
16	STARY10-	STARY03-	STARX03-
17	STARX10+	STARX10-	STARY03+
18	STARY09+	-2V	STARX04+
19	STARY09-	STARY04-	STARX04-
20	STARX09+	STARX09-	STARY04+
21	STARY08+	GND	STARX05+
22	STARY08-	STARY05-	STARX05-
23	STARX08+	STARX08-	STARY05+
24	STARY07+	+5V	STARX06+
25	STARY07-	STARY06-	STARX06-
26	STARX07+	STARX07-	STARY06+
27	GND	GND	GND
28	STARX+	-5.2V	STARY+
29	STARX-	GND	STARY-
30	GND	-5.2V	-5.2V
31	CLK100+	-2V	SYNC100+
32	CLK100-	GND	SYNC100-

Table 9-4. VXIbus P3 connector, slots 1 - 12.

VXIbus P3/J3 Connector, Slots 1 - 12			
Pin Number	Row A	Row B	Row C
1	ECLTRG2	+24V	+12V
2	GND	-24V	-12V
3	ECLTRG3	GND	RSV4
4	-2V	RSV5	+5V
5	ECLTRG4	-5.2V	RSV6
6	GND	RSV7	GND
7	ECLTRG5	+5V	-5.2V
8	-2V	GND	GND
9	LBUSA12	+5V	LBUSC12
10	LBUSA13	LBUSC15	LBUSC13
11	LBUSA14	LBUSA15	LBUSC14
12	LBUSA16	GND	LBUSC16
13	LBUSA17	LBUSC19	LBUSC17
14	LBUSA18	LBUSA19	LBUSC18
15	LBUSA20	+5V	LBUSC20
16	LBUSA21	LBUSC23	LBUSC21
17	LBUSA22	LBUSA23	LBUSC22
18	LBUSA24	-2V	LBUSC24
19	LBUSA25	LBUSC27	LBUSC25
20	LBUSA26	LBUSA27	LBUSC26
21	LBUSA28	GND	LBUSC28
22	LBUSA29	LBUSC31	LBUSC29
23	LBUSA30	LBUSA31	LBUSC30
24	LBUSA32	+5V	LBUSC32
25	LBUSA33	LBUSC35	LBUSC33
26	LBUSA34	LBUSA35	LBUSC34
27	GND	GND	GND
28	STARX+	-5.2V	STARY+
29	STARX-	GND	STARY-
30	GND	-5.2V	-5.2V
31	CLK100+	-2V	SYNC100+
32	CLK100-	GND	SYNC100-

9.3.1 VXIbus Clock Bus

The clock bus provides two clocks and a synchronization signal. A 10 MHz clock (CLK10) is located on the P2 connector, and a 100 MHz clock (CLK100) with a synchronization signal (SYNC100) is located on the P3 connector. CLK10, CLK100 and SYNC100 are differential ECL signals, and are located at the ends of the P2 and P3 connectors. They are isolated as much as possible with AC grounds (GND, +5V, -2V, etc.) to minimize noise jitter. The CLK10 and CLK100 signals are synchronized with each other.

Table 1-1. Features of some popular microcomputer buses.

Bus	Sync(S) or Async (A)	Multiplexed	Data bus width (bits)	Address width (bits)	Interrupts (levels)	Multiprocessing	Card size (mm)	Connector style	Governing body
Compact PCI	S	Y	32/64	32	Y	?	160 X 100 or 233 Eurocard	2mm Metric	PIC MG
IBM-PC	A	N	8	20	Y (6)	N	335 X 106	Card edge	IBM MSFT
Multibus	A	N	8,16	8,16, 20,24	Y (8)	Y	305 X 171	Card edge	IEEE 796
Multibus II	S	Y	8,16, 24,32	32	N	Y	233 X 220 Eurocard	DIN-41612	IEEE 1296
Nubus	S	Y	32	32	N	Y	233 X 160, 220 or 280 Eurocard	DIN-41612	TI
Q-Bus	A	Y	8,16	16,18 22	Y (4)	Y	214 X 132, 257 or 393	Card edge	Digital Equip. Corp.
STD Bus	A	N	8	16	Y (2)	Y	114 X 165	Card edge	IEEE 961
S-100	A	N	8,16	16,24	Y (8)	Y	254 X 130	Card edge	IEEE 696
VERSAbus	A	N	8,16, 32	16,24, 32	Y (7)	Y	368 X 235	Card edge	IEEE 970
VMEbus	A	N Y	8,16, 24,32, 64	16,24, 32, 64	Y (7)	Y	160 X 100 or 233 Eurocard	DIN-41612	ANSI VITA 1-1994

Notes: All dimensions rounded and presented in millimeters for comparison.
Y = Yes, N = No.

Table 1-3. VMEbus P1/J1 and P2/J2 pin assignments.

P1 / J1 Pin Assignments					
Pin	Row z (††)	Row a	Row b	Row c	Row d (††)
1	MPR	D00	BBSY*	D08	VPC (§)
2	GND	D01	BCLR*	D09	GND (§)
3	MCLK	D02	ACFAIL*	D10	+V1
4	GND	D03	BG0IN*	D11	+V2
5	MSD	D04	BG0OUT*	D12	RsvU
6	GND	D05	BG1IN*	D13	-V1
7	MMD	D06	BG1OUT*	D14	-V2
8	GND	D07	BG2IN*	D15	RsvU
9	MCTL	GND	BG2OUT*	GND	GAP*
10	GND	SYSCLK	BG3IN*	SYSFAIL*	GA0*
11	RESP*	GND	BG3OUT*	BERR*	GA1*
12	GND	DS1*	BR0*	SYSRESET*	+3.3V
13	RsvBus	DS0*	BR1*	LWORD*	GA2*
14	GND	WRITE*	BR2*	AM5	+3.3V
15	RsvBus	GND	BR3*	A23	GA3*
16	GND	DTACK*	AM0	A22	+3.3V
17	RsvBus	GND	AM1	A21	GA4*
18	GND	AS*	AM2	A20	+3.3V
19	RsvBus	GND	AM3	A19	RsvBus
20	GND	IACK*	GND	A18	+3.3V
21	RsvBus	IACKIN*	SERA (†)	A17	RsvBus
22	GND	IACKOUT*	SERB (†)	A16	+3.3V
23	RsvBus	AM4	GND	A15	RsvBus
24	GND	A07	IRQ7*	A14	+3.3V
25	RsvBus	A06	IRQ6*	A13	RsvBus
26	GND	A05	IRQ5*	A12	+3.3V
27	RsvBus	A04	IRQ4*	A11	LI/I*
28	GND	A03	IRQ3*	A10	+3.3V
29	RsvBus	A02	IRQ2*	A09	LI/O*
30	GND	A01	IRQ1*	A08	+3.3V
31	RsvBus	-12 VDC	+5VSTDBY	+12 VDC	GND (§)
32	GND	+5 VDC	+ 5VDC	+5 VDC	VPC (§)

Table 1-3 (con't).

P2 / J2 Pin Assignments					
Pin	Row z (††)	Row a	Row b	Row c	Row d (††)
1	UsrDef	UsrDef	+5 VDC	UsrDef	UsrDef (§)
2	GND	UsrDef	GND	UsrDef	UsrDef (§)
3	UsrDef	UsrDef	RETRY* (†)	UsrDef	UsrDef
4	GND	UsrDef	A24	UsrDef	UsrDef
5	UsrDef	UsrDef	A25	UsrDef	UsrDef
6	GND	UsrDef	A26	UsrDef	UsrDef
7	UsrDef	UsrDef	A27	UsrDef	UsrDef
8	GND	UsrDef	A28	UsrDef	UsrDef
9	UsrDef	UsrDef	A29	UsrDef	UsrDef
10	GND	UsrDef	A30	UsrDef	UsrDef
11	UsrDef	UsrDef	A31	UsrDef	UsrDef
12	GND	UsrDef	GND	UsrDef	UsrDef
13	UsrDef	UsrDef	+5 VDC	UsrDef	UsrDef
14	GND	UsrDef	D16	UsrDef	UsrDef
15	UsrDef	UsrDef	D17	UsrDef	UsrDef
16	GND	UsrDef	D18	UsrDef	UsrDef
17	UsrDef	UsrDef	D19	UsrDef	UsrDef
18	GND	UsrDef	D20	UsrDef	UsrDef
19	UsrDef	UsrDef	D21	UsrDef	UsrDef
20	GND	UsrDef	D22	UsrDef	UsrDef
21	UsrDef	UsrDef	D23	UsrDef	UsrDef
22	GND	UsrDef	GND	UsrDef	UsrDef
23	UsrDef	UsrDef	D24	UsrDef	UsrDef
24	GND	UsrDef	D25	UsrDef	UsrDef
25	UsrDef	UsrDef	D26	UsrDef	UsrDef
26	GND	UsrDef	D27	UsrDef	UsrDef
27	UsrDef	UsrDef	D28	UsrDef	UsrDef
28	GND	UsrDef	D29	UsrDef	UsrDef
29	UsrDef	UsrDef	D30	UsrDef	UsrDef
30	GND	UsrDef	D31	UsrDef	UsrDef
31	UsrDef	UsrDef	GND	UsrDef	GND (§)
32	GND	UsrDef	+5 VDC	UsrDef	VPC (§)

Notes: (†) Pin(s) redefined under the VME64 specification.
(††) Pin(s) redefined under the VME64x specification.
(§) Elongated (mate first, break last) connector contact.

Table 1-4. P0/J0 pin assignments.

P0 / J0 / RJ0 / RP0 Connector Pinout							
Pos.	Row f	Row e	Row d	Row c	Row b	Row a	Row z
1	GND	UsrDef	UsrDef	UsrDef	UsrDef	UsrDef	GND
2	GND	UsrDef	UsrDef	UsrDef	UsrDef	UsrDef	GND
3	GND	UsrDef	UsrDef	UsrDef	UsrDef	UsrDef	GND
4	GND	UsrDef	UsrDef	UsrDef	UsrDef	UsrDef	GND
5	GND	UsrDef	UsrDef	UsrDef	UsrDef	UsrDef	GND
6	GND	UsrDef	UsrDef	UsrDef	UsrDef	UsrDef	GND
7	GND	UsrDef	UsrDef	UsrDef	UsrDef	UsrDef	GND
8	GND	UsrDef	UsrDef	UsrDef	UsrDef	UsrDef	GND
9	GND	UsrDef	UsrDef	UsrDef	UsrDef	UsrDef	GND
10	GND	UsrDef	UsrDef	UsrDef	UsrDef	UsrDef	GND
11	GND	UsrDef	UsrDef	UsrDef	UsrDef	UsrDef	GND
12	GND	UsrDef	UsrDef	UsrDef	UsrDef	UsrDef	GND
13	GND	UsrDef	UsrDef	UsrDef	UsrDef	UsrDef	GND
14	GND	UsrDef	UsrDef	UsrDef	UsrDef	UsrDef	GND
15	GND	UsrDef	UsrDef	UsrDef	UsrDef	UsrDef	GND
16	GND	UsrDef	UsrDef	UsrDef	UsrDef	UsrDef	GND
17	GND	UsrDef	UsrDef	UsrDef	UsrDef	UsrDef	GND
18	GND	UsrDef	UsrDef	UsrDef	UsrDef	UsrDef	GND
19	GND	UsrDef	UsrDef	UsrDef	UsrDef	UsrDef	GND

1.2.7.8 BG0IN* - BG3IN* / BG0OUT* - BG3OUT*

The bus grant signals [BG0IN* - BG3IN* and BG0OUT* - BG3OUT*] are part of the bus grant daisy-chain and are driven by arbiters and requesters. The slot 01 arbiter asserts a bus grant in response to a bus request on the same level [BR0* - BR3*]. The bus grant daisy-chain starts at the slot 01 system controller and propagates from module to module until it reaches the module that initially requested the bus. Each VMEbus module has a bus grant input and a bus grant output. They are standard totem-pole class signals.

1.2.7.9 BR0* - BR3*

Bus requests [BR0* - BR3*] are asserted by a requester whenever its master or interrupt handler needs the bus. Before accepting the bus, the master waits until the arbiter grants the bus by way of the bus grant daisy-chain [BG0IN* - BG3IN*]. They are open-collector class signals.