TRIUMF Multi-Purpose VME I/O Module

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A report prepared for the CHAOS and DAQ groups.

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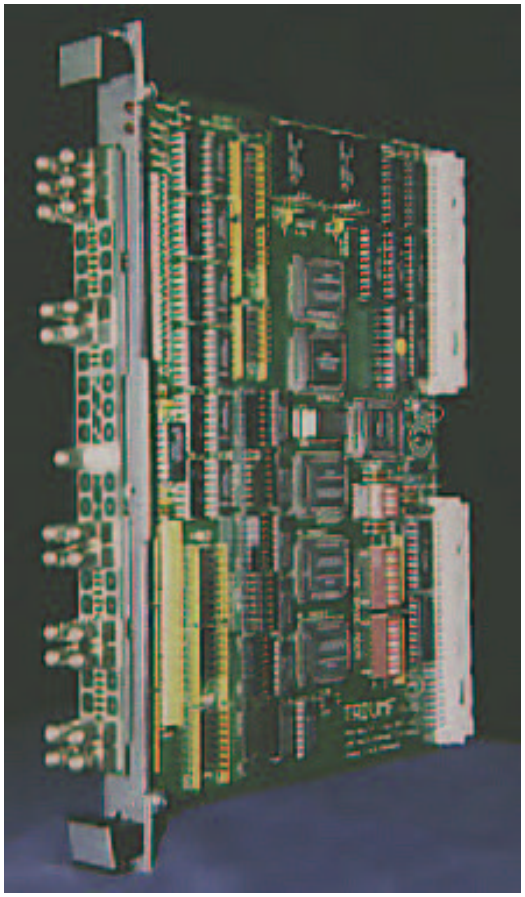

In keeping with the ongoing trend within the CHAOS group of translating CAMAC data acquisition elements to VME, we have designed and constructed a VME module to replace CAMAC Pattern-unit and Output-register functions. Notable features are:

- **24 Output Channels with:**
- **Independent Pulse and Latch modes**
- **Simultaneous NIM and ECL Outputs**
- **24 Input Channels with:**
- **Independent Synchronous and Asynchronous modes**
- **Selectable NIM or ECL inputs**
- **Prioritized Synchronous/Asynchronous VME Interrupts on 8 Input Channels**
- **A32 / A24 and D32 (only) access modes**
- **Uses standard VME backplane**
- **Reprogrammable functionality**

PRELIMINARY

1.0 Functional Description

This module makes extensive use of Altera's series of programmable logic devices to achieve higher channel densities and handle all VME-bus handshaking. All on-board logic is contained in six EPM7064LC44-15 devices, allowing for easy functional and maintenance updates. All necessary design software and programming hardware is available on-site.[1]

All I/O channels are available as ECL or NIM levels, depending on jumper setups. ECL -5V power is supplied from the standard -12V by means of efficient switching regulators, thus obviating the need for a CERN Jaux Dataway connector.

The VME interrupt generator is a ROAK type, and drives IRQ7* on the VME bus — the highest interrupt level. The returned D08 status byte is suitable for use as an interrupt vector on MC68XXX processors. It encodes the value of the highest input channel (#1 — #8) generating the interrupt in the lower 3 bits.

Interrupts may be synchronous — generated by a coincidence between a STROBE and an input channel — or asynchronous — initiated by a low-to-high transition on one of the first 8 input channels. The current interrupt type may be read out in a status register, and an 8-bit interrupt-enable register may also be written to the module. Interrupts must be re-enabled via a CLSTB or INTSRC command.

24 output channels are available, each selectable as a latched or pulsing output. Output in one mode does not affect the previous state of the other mode. That is, a Latch-Mode output set high may be switched to Pulse-Mode, used for output, and then switched back maintaining the high state. Outputs may be jumper disabled to reduce power consumption.

24 input channels are available, the first 8 of which are shared with the interrupt system. Data may be clocked in by a STROBE signal, or read asynchronously without affecting previously clocked data. Synchronous acquisition must be re-armed after each STROBE. The state of the STROBE (Armed/Triggered) may be read out in a status register.

1. Contact Daryl Bishop, TRIUMF Electronics and Computing Division, for more information.

2.0 Specifications

2.1 General

2.1.1 Physical Specifications

A single width 6 U VME board, in conformance with VME specifications. A front-panel daughter-card provides for NIM I/O via LEMO connectors.

2.1.2 Power Requirements

+5V @ 1060 mA, -12V @ 940 mA.

2.1.3 Module State On Power-Up Reset

The interrupt source is set to synchronous, and interrupts are disabled. Synchronous and asynchronous input registers are cleared, and the external STROBE is armed. All output registers are set to latch-mode and each latch is cleared.

2.1.4 Input Timing Specifications

STROBE:	10 ns min. pulse width
INPUTS:	
Synchronous:	0 ns setup time, 20 ns hold time
Asynchronous:	10 ns min. pulse width for generating interrupts

2.2 VME Control

Device Type:	A32/A24 (jumper select) D32 (only)
Base Address:	Switch selectable, A31-A16
Address Mod.:	AM = 39, AM = 09 (standard/extended non-privileged)
DTACK*:	Asserted on valid function

2.3 Inputs / Outputs

NIM:	24 output + 24 inputs + 1 strobe all on a front-panel daughter card
ECL:	24 differential outputs (32-way and 16-way connectors) 24 + 1 strobe differential inputs (34-way and 16-way connectors) STROBE is pins 33/34

(only the first 8 ECL and NIM inputs are interruptible)

LEDS:	One for strobe input; one for valid VME access

2.4 VME Addresses and Functions

Table 1 lists the valid VME addresses recognized by the module, whether they are read or write access, and the associated function. An 'X' indicates don't-care address bits. The entire 64K address space is populated with images of this table. Note that all access is in D32 mode.

TABLE 1. VME Addressing

Address	R/W	Function
XXX0	W	IRQENBL
XXX4	W	INTSRC
XXX8	W	OUTSET
XXXC	W	OUTPULSE
XX10	W	OUTLATCH
XX14	R	RDSYNC
XX18	R	RDASYNC
XX1C	R	RDCNTL
XX1C	W	CLSTB

2.4.1 IRQENBL

This writes the 8-bit interrupt-enable register. Bit = 1 allows the corresponding input channel to generate interrupts.

2.4.2 INTSRC

Selects the interrupt source. Writing a 1 to the LSB selects synchronous interrupts, while writing a 0 selects asynchronous interrupts. When switching sources, it is recommended interrupts be disabled first with the IRQENBL command. The INTSRC command also re-enables asynchronous interrupts.

2.4.3 OUTSET

This writes a 24-bit output-type register which defines the mode of each output channel. Bit = 1 sets the corresponding output channel to pulse-mode, bit = 0 sets it to latch-mode.

2.4.4 OUTPULSE

For each of 24 bits set, pulses the corresponding output channel if its current mode allows. The pulse width is nominally 60 ns.

2.4.5 OUTLATCH

Writes a 24-bit register, where a 1 sets and a 0 clears the latched output of the corresponding channel if its current mode allows.

2.4.6 RDSYNC

Unconditionally reads a synchronous data register of the form 0xFFhhhhhh, where hhhhhh corresponds to the 24 input channels, regardless of whether or not a STROBE has been received. The RDCNTL function can be used to determine if data has been clocked into the module.

2.4.7 RDASYNC

Returns 24 bits of data sampled at the time of the function. Synchronous data acquisition is unaffected and may proceed in tandem, possibly even generating interrupts.

2.4.8 RDCNTL

Reads an 8-bit control register of the form 0xAB. B = F indicates a STROBE has been received. A = F / 0 indicates sync/async as the currently selected interrupt source.

2.4.9 CLSTB

Any data written to this address will re-arm the STROBE and, hence, re-enable synchronous input and synchronous interrupts if so enabled.

2.5 Connector, Jumper and Switch Setup

The various switch and jumper settings affecting the module are summarized in Table 2, followed by brief descriptions. The designators used are those found on the board.

TABLE 2. Connector, Switch, and Jumper Settings

Switch or Jumper	Description
S1	VEC[0..3]
S3	VME base address [16..23]
S4	VME base address [24..31]
J1	NIM/ECL input select [1..8]
J2	NIM/ECL input select [9..16]
J3	NIM/ECL input select [17..24]
J4	NIM/ECL input select STROBE
JP1	ECL input [1..16], STROBE
JP5	ECL input [17..24]
JP3	NIM input STROBE, [1..24]
JP2	ECL output [1..16]
JP6	ECL output [17..24]
JP4	NIM output [1..24]
JP7	NIM output enable
JP8	ECL output enable
JP10	ECL/NIM output enable
JP9	Select VME address mode: A24 (IN) / A32 (OUT)

2.5.1 Address Decoding

The upper 16 bits [16..31] of the VME base address are set using the S3 and S4 dip switches. S4 is irrelevant in A24 mode, which is enabled by installing jumper JP9.

2.5.2 Interrupt Status Byte

The status byte returned by the module is of the form 1SSSSVVV, where SSSS corresponds to the settings on switch S1. The bits VVV encode the value of the highest channel generating the interrupt, from 0 to 7.

2.5.3 Input Selection

Input sources may be ECL or NIM on a per channel basis, the selection made using four blocks of 3-pin wide headers, J1 - J4. Blocks J1 - J3 are 8 data channels each, while J4 is for the external strobe. Each channel represents a differential signal, hence J1 is a 3x16 pin connector. Using a 2x16 jumper block on one side of J1 selects NIM inputs for the first 8 channels, and ECL inputs when used on the other side. A single channel, such as the STROBE, may be switched using a 2x2 jumper block.

2.5.4 Output Enables[1]

To reduce the load on the -12V supply, it is possible to selectively disable pull-downs and I.C.'s generating the NIM and ECL outputs. Removing JP7 disables NIM output with negligible change in current drain; removing JP8 disables ECL output and reduces drain by ~200 mA; further removing JP10 disables all output and reduces current drain by an additional ~100 mA.

2.5.5 I/O Connections

The JP3 and JP4 connectors are used to attach a front-panel daughter card that incorporates the 49 LEMO connectors used for NIM input and output. ECL I/O is through connectors JP1, JP2, JP5, and JP6. *Note: the daughter card is currently not keyed; it is possible to insert it upside down and short all the NIM outputs together.*

3.0 Desiderata

C86 and C87 should both be changed to 47 nF. This allows low rate LED flashes to be visible.

1. Author's note: these current savings are not worth the hassle of providing enables. Omit them in future versions.