NIM I/O
Sheet 8

Power/Clock Distribution
Sheet 9

FPGA
Sheets 3 + 4

VME Interface
Sheet 6 + 7

MEMORY
(SRAM and FLASH)
Sheet 4

CPLD
Sheet 5

XKE0822

J7 TSW-102-07

J5 TSW-102-07

P1 3M, 2x34 pin Right Angle Condip Header w/ Latch, 0.1" Pitch, 3M Pak 100 3-Wall Condo Header

IN[33..48]p,IN[33..48]n

IN[25..32]p,IN[25..32]n

IN[17..24]p,IN[17..24]n

ASDCLK, ASDIN, ASDLOAD, ASDDOWN, ASDOUT

ENCCONTM, ENCCONTP, RESETB, STROBEM, STROBEP, SERIOUTM, SERIOUTP, TRSTB, TCK, TDI, TMS, TDO, CLKOUT, ERRORB, CLKP, CLKM, TRIGGER, CLK0, EVENTRSTB, CLKOEN, BUNCHRSTB

D+3.3V, R95 10Kohms, C101 10uF 6V Tantalum, R97 10Kohms, D1 BAS81, R102 10Kohms, R103 10Kohms, R104 10Kohms, R105 10Kohms

CONFIG BYPASS, TSW-102-07 J11

TPthru TP1, TPthru TP2

D-3.3V, D+3.3V, D+2.5V, R85 4.7Kohms LED2, R101 4.7Kohms LED3, R111 4.7Kohms LED4, LTST-190KRKT

lvds_CLKOUTn, lvds_CLKOUTp, lvds_DATAINn, lvds_CLKINp, lvds_CLKINn, lvds_DATAINp, lvds_DATAOUTn, lvds_DATAOUTp, SHIELD

AMP 1-1416603-1 Low Profile RJ45 Jack, AMP 1-1116503-1 AMP Ultra Low Profile RJ45 Jack

R126 10Kohms, SW3 B3F-1020, pb_CPU_RESET

LED1 90-1882-2781, R1 330ohms, R2 330ohms, R3 330ohms, led_STATUS, led_VMEbusy

R110 10Kohms, SW2 B3F-1020, pb_SAFEn

R4 10Kohms, SW1 B3F-3152, pb_HRESETn

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THESE DESIGNS WERE REALIZED USING MENTOR GRAPHICS PRODUCTS UNDER THE HIGHER EDUCATION PROGRAM.

PROJECT: VME Readout Electronics
DESIGNED: Chris Ohlmann
DRAWN: Chris Ohlmann
CHECKED: -
APPROVED: -

VT48 - 48 Channel VME TDC (AMT3)
Top Level Schematic
Channels 25 to 48

REVISIONS ARE DETAILED IN THE DOCUMENT: No Revisions
LIST: VT48.xls
DATE: 3/28/2006
SHEET: 01 OF 09

DOCUMENT NUMBER XKE-0820C REV. A

Last Modified: 4:07:24 PM on 3/28/2006
Last Archived: 3:41:11 PM on 3/28/2006
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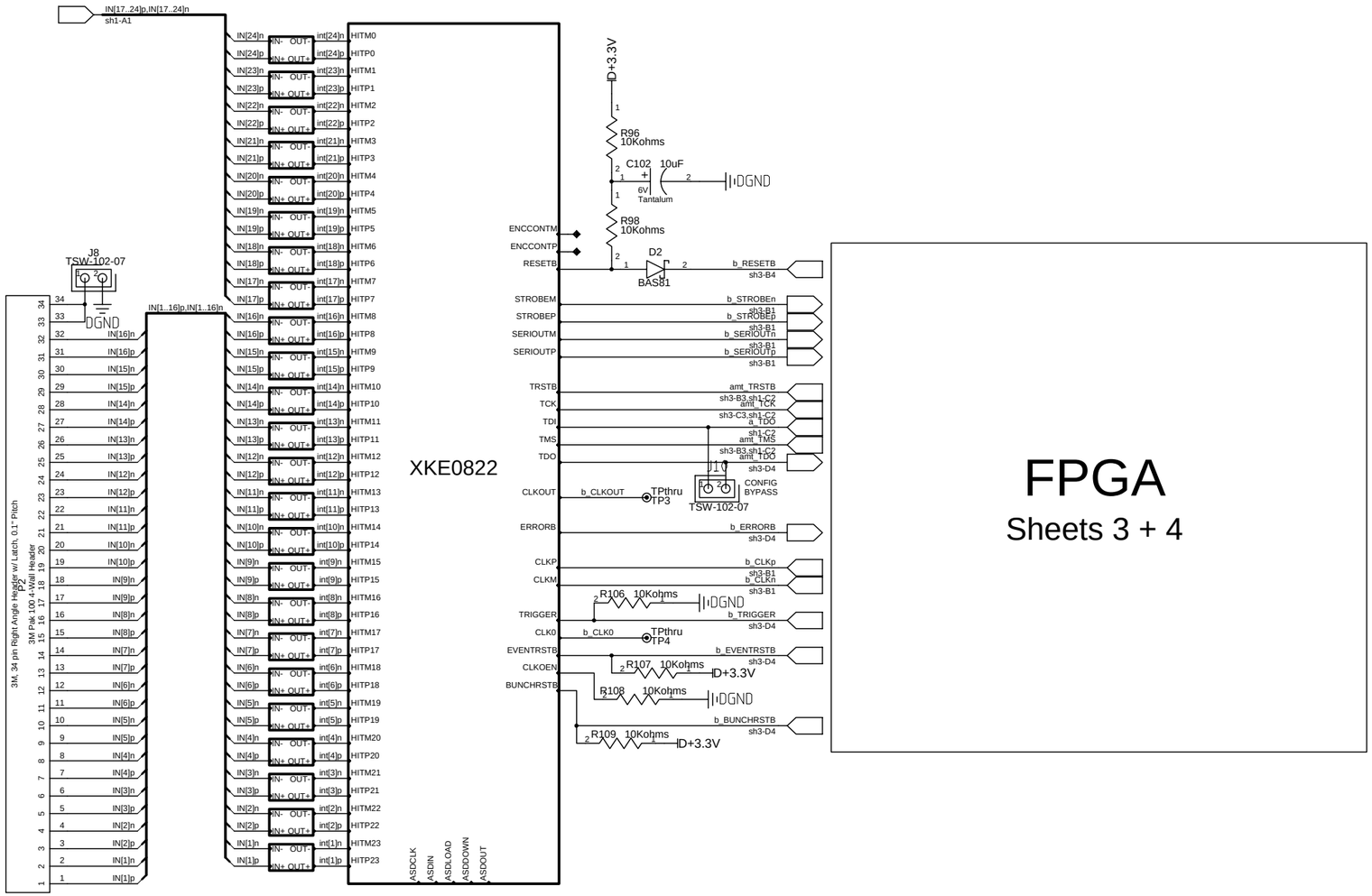

TRIUMF Canada's National Laboratory for Particle and Nuclear Physics, 4004 Wesbrook Mall, Vancouver, BC, Canada V6T 2A3, Tel: [604] 222-1047 www.triumf.ca Fax: [604] 222-1074	VT48 - 48 Channel VME TDC (AMT3) Top Level Schematic Channels 1 to 24	
THESE DESIGNS WERE REALIZED USING MENTOR GRAPHICS PRODUCTS UNDER THE HIGHER EDUCATION PROGRAM.		
PROJECT: VME Readout Electronics		
DESIGNED: Chris Ohlmann	REVISIONS ARE DETAILED IN THE DOCUMENT:	No Revisions
DRAWN: Chris Ohlmann	LIST: VT48.xls	DOCUMENT NUMBER XKE-0820C REV. A
CHECKED: -	DATE: 3/28/2006	
APPROVED: -	SHEET: 02 OF 09	

Last Modified at: 7:07:42 PM on 3/28/2006
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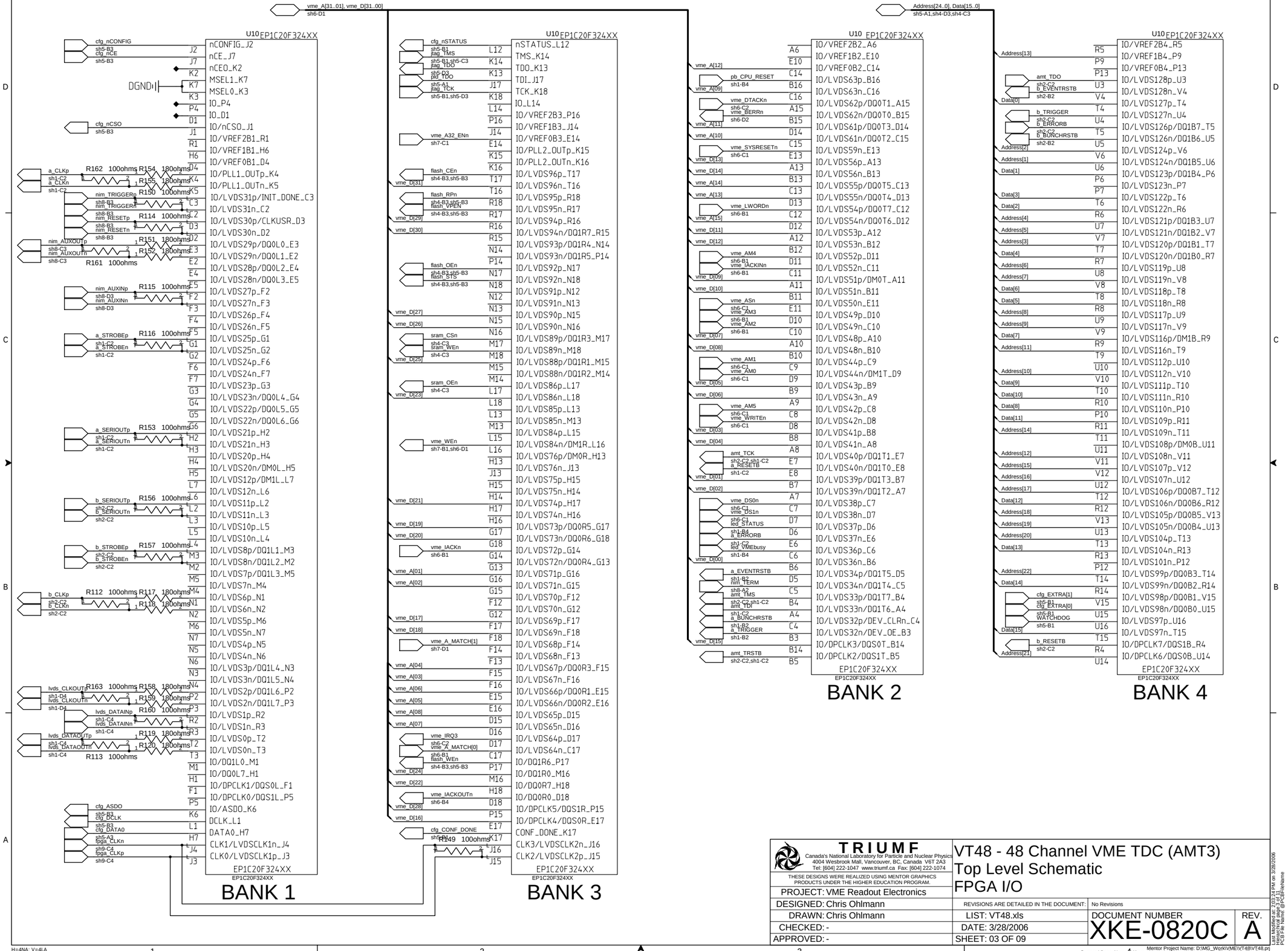
vme_A[31..01], vme_D[31..00]
sh6-D1
Address[24..0], Data[15..0]
sh5-A1,sh4-D3,sh4-C3
U10 EP1C20F324XX
nCONFIG_J2
nCE_J7
nCEO_K2
MSEL1_K7
MSEL0_K3
IO_P4
IO_D1
IO/nCSO_J1
IO/VREF2B1_R1
IO/VREF1B1_H6
IO/VREF0B1_D4
IO/PLL1_OUTp_K4
IO/PLL1_OUTn_K5
IO/LVDS31p/INIT_DONE_C3
IO/LVDS31n_C2
IO/LVDS30p/CLKUSR_D3
IO/LVDS30n_D2
IO/LVDS29p/DQ0L0_E3
IO/LVDS29n/DQ0L1_E2
IO/LVDS28p/DQ0L2_E4
IO/LVDS28n/DQ0L3_E5
IO/LVDS27p_F2
IO/LVDS27n_F3
IO/LVDS26p_F4
IO/LVDS26n_F5
IO/LVDS25p_G1
IO/LVDS25n_G2
IO/LVDS24p_F6
IO/LVDS24n_F7
IO/LVDS23p_G3
IO/LVDS23n/DQ0L4_G4
IO/LVDS22p/DQ0L5_G5
IO/LVDS22n/DQ0L6_G6
IO/LVDS21p_H2
IO/LVDS21n_H3
IO/LVDS20p_H4
IO/LVDS20n/DM0L_H5
IO/LVDS12p/DM1L_L7
IO/LVDS12n_L6
IO/LVDS11p_L2
IO/LVDS11n_L3
IO/LVDS10p_L5
IO/LVDS10n_L4
IO/LVDS8p/DQ1L1_M3
IO/LVDS8n/DQ1L2_M2
IO/LVDS7p/DQ1L3_M5
IO/LVDS7n_M4
IO/LVDS6p_N1
IO/LVDS6n_N2
IO/LVDS5p_M6
IO/LVDS5n_N7
IO/LVDS4p_N5
IO/LVDS4n_N6
IO/LVDS3p/DQ1L4_N3
IO/LVDS3n/DQ1L5_N4
IO/LVDS2p/DQ1L6_P2
IO/LVDS2n/DQ1L7_P3
IO/LVDS1p_R2
IO/LVDS1n_R3
IO/LVDS0p_T2
IO/LVDS0n_T3
IO/DQ1L0_M1
IO/DQ0L7_H1
IO/DPCLK1/DQS0L_F1
IO/DPCLK0/DQS1L_P5
IO/ASDO_K6
DCLK_L1
DATA0_H7
CLK1/LVDSCLK1n_J4
CLK0/LVDSCLK1p_J3
EP1C20F324XX
BANK 1
cfg_nCONFIG
cfg_nCE
cfg_nCSO
DGND
a_CLKp
a_CLKn
nim_TRIGGERp
nim_TRIGGERn
nim_RESETp
nim_RESETn
nim_AUXOUTp
nim_AUXOUTn
nim_AUXINp
nim_AUXINn
a_STROBEp
a_STROBEn
a_SERIOUTp
a_SERIOUTn
b_SERIOUTp
b_SERIOUTn
b_STROBEp
b_STROBEn
b_CLKp
b_CLKn
lvds_CLKOUTp
lvds_CLKOUTn
lvds_DATAINp
lvds_DATAINn
lvds_DATAOUTp
lvds_DATAOUTn
R162 100ohms
R154 180ohms
R155 180ohms
R150 100ohms
R114 100ohms
R151 180ohms
R152 180ohms
R161 100ohms
R115 100ohms
R116 100ohms
R153 100ohms
R156 100ohms
R157 100ohms
R112 100ohms
R117 180ohms
R118 180ohms
R163 100ohms
R158 180ohms
R159 180ohms
R160 100ohms
R119 180ohms
R120 180ohms
R113 100ohms
cfg_ASDO
cfg_DCLK
cfg_DATA0
fpga_CLKn
fpga_CLKp
U10 EP1C20F324XX
nSTATUS_L12
TMS_K14
TDO_K13
TDI_J17
TCK_K18
IO_L14
IO/VREF2B3_P16
IO/VREF1B3_J14
IO/VREF0B3_E14
IO/PLL2_OUTp_K15
IO/PLL2_OUTn_K16
IO/LVDS96p_T17
IO/LVDS96n_T16
IO/LVDS95p_R18
IO/LVDS95n_R17
IO/LVDS94p_R16
IO/LVDS94n/DQ1R7_R15
IO/LVDS93p/DQ1R4_N14
IO/LVDS93n/DQ1R5_P14
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IO/LVDS90n_N16
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IO/LVDS89n_M18
IO/LVDS88p/DQ1R1_M15
IO/LVDS88n/DQ1R2_M14
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IO/LVDS86n_L18
IO/LVDS85p_L13
IO/LVDS85n_M13
IO/LVDS84p_L15
IO/LVDS84n/DM1R_L16
IO/LVDS76p/DM0R_H13
IO/LVDS76n_J13
IO/LVDS75p_H15
IO/LVDS75n_H14
IO/LVDS74p_H17
IO/LVDS74n_H16
IO/LVDS73p/DQ0R5_G17
IO/LVDS73n/DQ0R6_G18
IO/LVDS72p_G14
IO/LVDS72n/DQ0R4_G13
IO/LVDS71p_G16
IO/LVDS71n_G15
IO/LVDS70p_F12
IO/LVDS70n_G12
IO/LVDS69p_F17
IO/LVDS69n_F18
IO/LVDS68p_F14
IO/LVDS68n_F13
IO/LVDS67p/DQ0R3_F15
IO/LVDS67n_F16
IO/LVDS66p/DQ0R1_E15
IO/LVDS66n/DQ0R2_E16
IO/LVDS65p_D15
IO/LVDS65n_D16
IO/LVDS64p_D17
IO/LVDS64n_C17
IO/DQ1R6_P17
IO/DQ1R0_M16
IO/DQ0R7_H18
IO/DQ0R0_D18
IO/DPCLK5/DQS1R_P15
IO/DPCLK4/DQS0R_E17
CONF_DONE_K17
CLK3/LVDSCLK2n_J16
CLK2/LVDSCLK2p_J15
EP1C20F324XX
BANK 3
cfg_nSTATUS
jtag_TMS
jtag_TDO
jtag_TCK
vme_A32_ENn
flash_CEn
flash_RPn
flash_VPEN
flash_OEn
flash_STS
sram_CSn
sram_WEn
sram_OEn
vme_WEn
vme_IACKn
vme_IACKOUTn
cfg_CONF_DONE
R149 100ohms
IO/VREF2B2_A6
IO/VREF1B2_E10
IO/VREF0B2_C14
IO/LVDS63p_B16
IO/LVDS63n_C16
IO/LVDS62p/DQ0T1_A15
IO/LVDS62n/DQ0T0_B15
IO/LVDS61p/DQ0T3_D14
IO/LVDS61n/DQ0T2_C15
IO/LVDS59n_E13
IO/LVDS56p_A13
IO/LVDS56n_B13
IO/LVDS55p/DQ0T5_C13
IO/LVDS55n/DQ0T4_D13
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IO/LVDS54n/DQ0T6_D12
IO/LVDS53p_A12
IO/LVDS53n_B12
IO/LVDS52p_D11
IO/LVDS52n_C11
IO/LVDS51p/DM0T_A11
IO/LVDS51n_B11
IO/LVDS50n_E11
IO/LVDS49p_D10
IO/LVDS49n_C10
IO/LVDS48p_A10
IO/LVDS48n_B10
IO/LVDS44p_C9
IO/LVDS44n/DM1T_D9
IO/LVDS43p_B9
IO/LVDS43n_A9
IO/LVDS42p_C8
IO/LVDS42n_D8
IO/LVDS41p_B8
IO/LVDS41n_A8
IO/LVDS40p/DQ1T1_E7
IO/LVDS40n/DQ1T0_E8
IO/LVDS39p/DQ1T3_B7
IO/LVDS39n/DQ1T2_A7
IO/LVDS38p_C7
IO/LVDS38n_D7
IO/LVDS37p_D6
IO/LVDS37n_E6
IO/LVDS36p_C6
IO/LVDS36n_B6
IO/LVDS34p/DQ1T5_D5
IO/LVDS34n/DQ1T4_C5
IO/LVDS33p/DQ1T7_B4
IO/LVDS33n/DQ1T6_A4
IO/LVDS32p/DEV_CLRn_C4
IO/LVDS32n/DEV_OE_B3
IO/DPCLK3/DQS0T_B14
IO/DPCLK2/DQS1T_B5
EP1C20F324XX
BANK 2
pb_CPU_RESET
vme_DTACKn
vme_SYSRESETn
vme_LWORDn
vme_AM4
vme_IACKINn
vme_ASn
vme_AM3
vme_AM2
vme_AM1
vme_AM0
vme_AM5
vme_WRITEn
amt_TCK
a_RESETB
vme_DS0n
vme_DS1n
led_STATUS
a_ERRORB
led_VMEbusy
a_EVENTRSTB
nim_TERM
amt_TMS
amt_TDI
a_BUNCHRSTB
a_TRIGGER
amt_TRSTB
IO/VREF2B4_R5
IO/VREF1B4_P9
IO/VREF0B4_P13
IO/LVDS128p_U3
IO/LVDS128n_V4
IO/LVDS127p_T4
IO/LVDS127n_U4
IO/LVDS126p/DQ1B7_T5
IO/LVDS126n/DQ1B6_U5
IO/LVDS124p_V6
IO/LVDS124n/DQ1B5_U6
IO/LVDS123p/DQ1B4_P6
IO/LVDS123n_P7
IO/LVDS122p_T6
IO/LVDS122n_R6
IO/LVDS121p/DQ1B3_U7
IO/LVDS121n/DQ1B2_V7
IO/LVDS120p/DQ1B1_T7
IO/LVDS120n/DQ1B0_R7
IO/LVDS119p_U8
IO/LVDS119n_V8
IO/LVDS118p_T8
IO/LVDS118n_R8
IO/LVDS117p_U9
IO/LVDS117n_V9
IO/LVDS116p/DM1B_R9
IO/LVDS116n_T9
IO/LVDS112p_U10
IO/LVDS112n_V10
IO/LVDS111p_T10
IO/LVDS111n_R10
IO/LVDS110n_P10
IO/LVDS109p_R11
IO/LVDS109n_T11
IO/LVDS108p/DM0B_U11
IO/LVDS108n_V11
IO/LVDS107p_V12
IO/LVDS107n_U12
IO/LVDS106p/DQ0B7_T12
IO/LVDS106n/DQ0B6_R12
IO/LVDS105p/DQ0B5_V13
IO/LVDS105n/DQ0B4_U13
IO/LVDS104p_T13
IO/LVDS104n_R13
IO/LVDS101n_P12
IO/LVDS99p/DQ0B3_T14
IO/LVDS99n/DQ0B2_R14
IO/LVDS98p/DQ0B1_V15
IO/LVDS98n/DQ0B0_U15
IO/LVDS97p_U16
IO/LVDS97n_T15
IO/DPCLK7/DQS1B_R4
IO/DPCLK6/DQS0B_U14
EP1C20F324XX
BANK 4
Address[13]
Address[2]
Address[1]
Data[1]
Data[3]
Data[2]
Address[4]
Address[5]
Address[3]
Data[4]
Address[6]
Address[7]
Data[5]
Address[8]
Address[9]
Data[7]
Address[11]
Address[10]
Data[9]
Data[10]
Data[8]
Data[11]
Address[14]
Address[12]
Address[15]
Address[16]
Address[17]
Data[12]
Address[18]
Address[19]
Address[20]
Data[13]
Address[22]
Data[14]
Data[15]
Address[21]
Data[0]
b_EVENTRSTB
b_TRIGGER
b_ERRORB
b_BUNCHRSTB
b_RESETB
cfg_EXTRA[1]
cfg_EXTRA[0]
WATCHDOG
TRIUMF
Canada's National Laboratory for Particle and Nuclear Physics
4004 Wesbrook Mall, Vancouver, BC, Canada V6T 2A3
Tel: [604] 222-1047 www.triumf.ca Fax: [604] 222-1074
THESE DESIGNS WERE REALIZED USING MENTOR GRAPHICS PRODUCTS UNDER THE HIGHER EDUCATION PROGRAM.
PROJECT: VME Readout Electronics
DESIGNED: Chris Ohlmann
DRAWN: Chris Ohlmann
CHECKED: -
APPROVED: -
VT48 - 48 Channel VME TDC (AMT3)
Top Level Schematic
FPGA I/O
REVISIONS ARE DETAILED IN THE DOCUMENT: No Revisions
LIST: VT48.xls
DATE: 3/28/2006
SHEET: 03 OF 09
DOCUMENT NUMBER
XKE-0820C
REV.
A
Last Modified: 3/30/2006 2:47:24 PM on 3/28/2006
Hierarchical page 3 of 11
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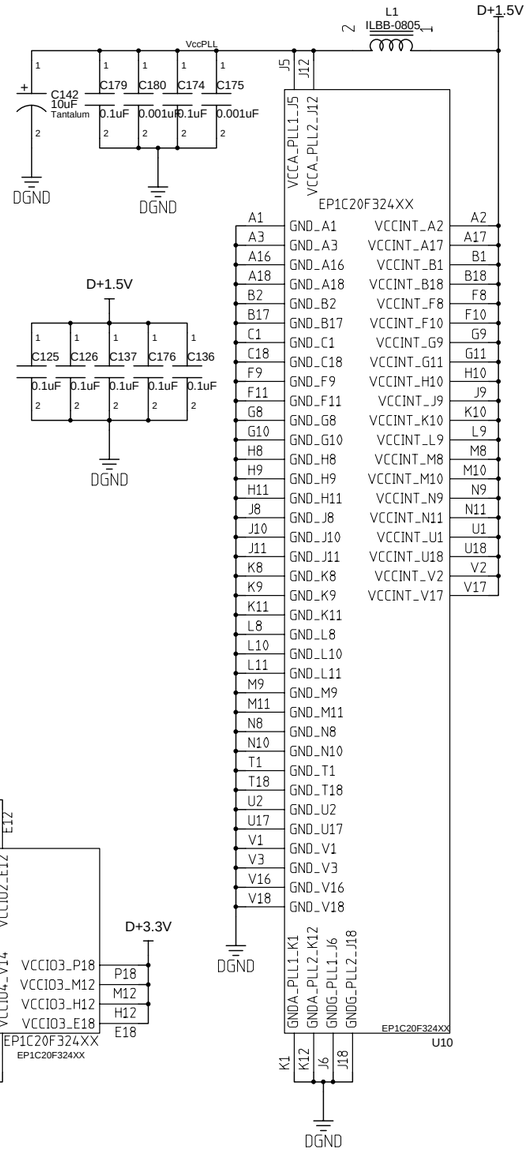
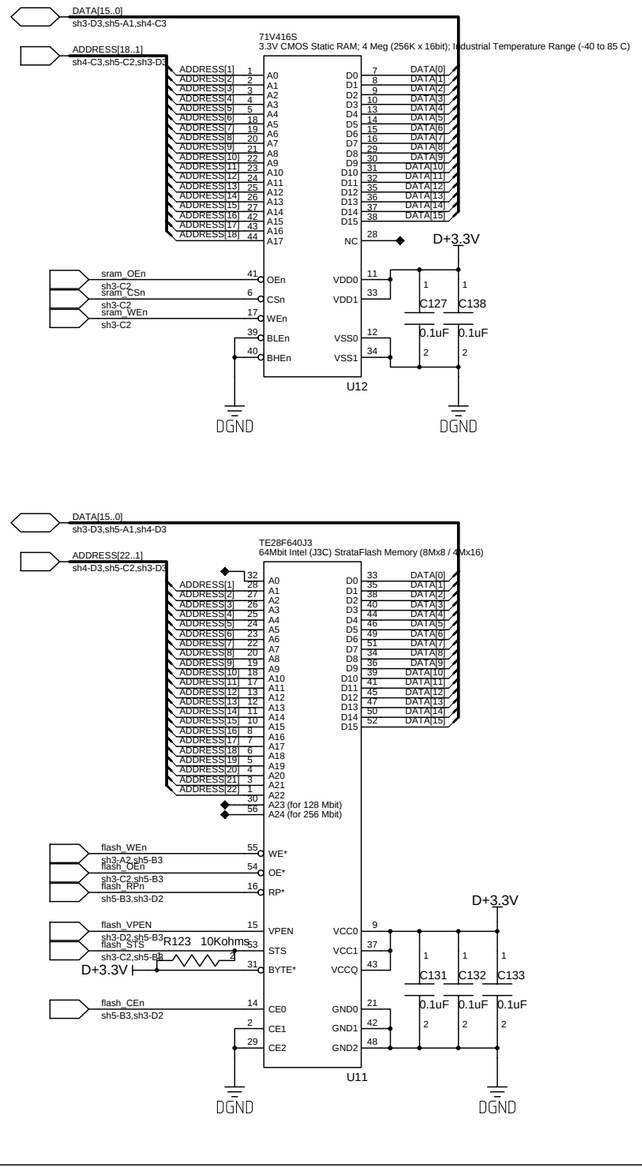
H=4NA; V=4LA

FPGA POWER



MEMORY - SRAM AND FLASH

Address[0] is not used... Both the SRAM and FLASH are using 16-bit addressing.



TRIUMF Canada's National Laboratory for Particle and Nuclear Physics, 4004 Wesbrook Mall, Vancouver, BC, Canada V6T 2A3, Tel: [604] 222-1047 www.triumf.ca Fax: [604] 222-1074	VT48 - 48 Channel VME TDC (AMT3)	
THESE DESIGNS WERE REALIZED USING MENTOR GRAPHICS PRODUCTS UNDER THE HIGHER EDUCATION PROGRAM.	Top Level Schematic	
	FPGA Power and Board Memory (Flash + SRAM)	
PROJECT: VME Readout Electronics		
DESIGNED: Chris Ohlmann	REVISIONS ARE DETAILED IN THIS DOCUMENT: No Revisions	
DRAWN: Chris Ohlmann	LIST: VT48.xls	DOCUMENT NUMBER XKE-0820C / REV. A
CHECKED: -	DATE: 3/28/2006	
APPROVED: -	SHEET: 04 OF 09	

Last Modified on: 2/27/2006 at 3:28:20
Last Archived on: 4:03:13
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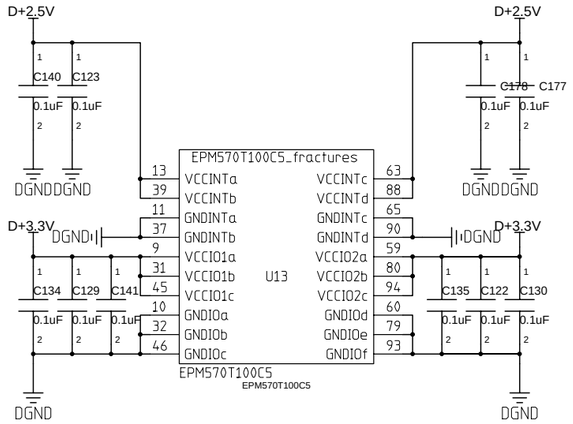

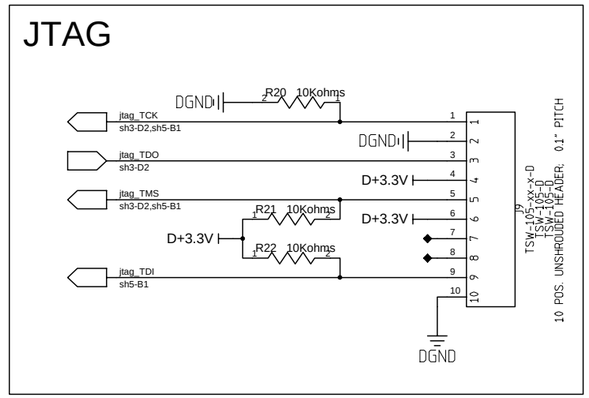

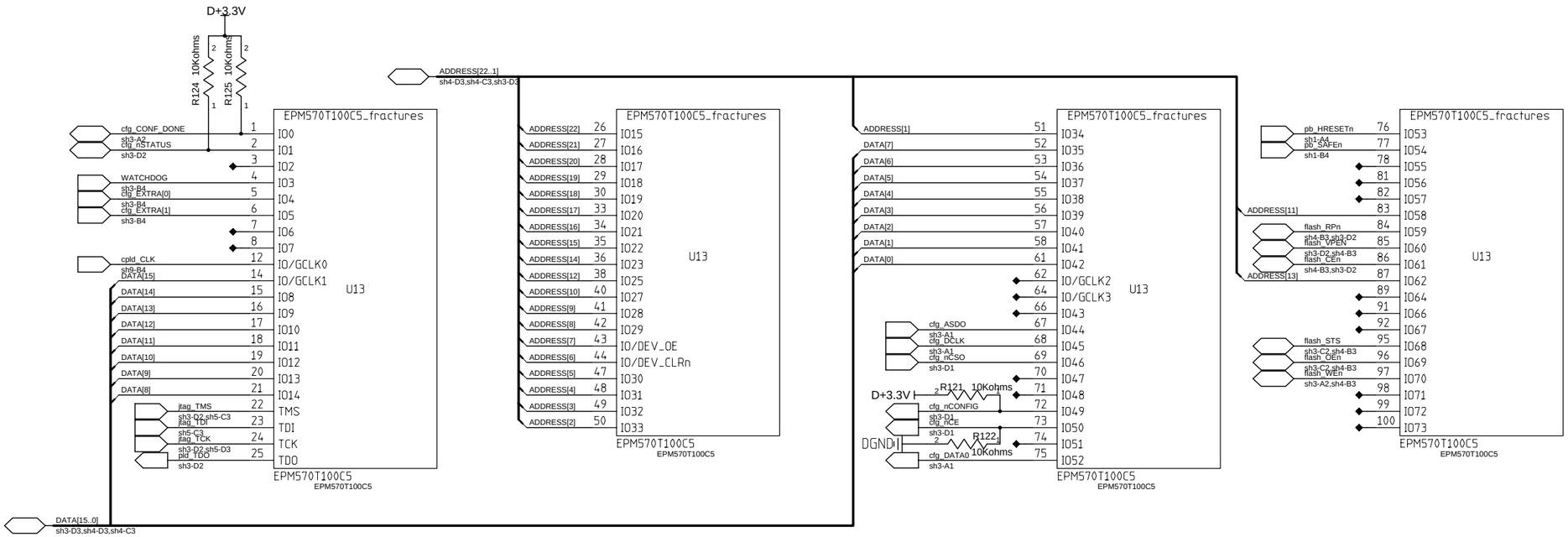

TRIUMF Canada's National Laboratory for Particle and Nuclear Physics, 4004 Wesbrook Mall, Vancouver, BC, Canada V6T 2A3, Tel: [604] 222-1047 www.triumf.ca Fax: [604] 222-1074	VT48 - 48 Channel VME TDC (AMT3) Top Level Schematic Configuration - PLD and JTAG	
THESE DESIGNS WERE REALIZED USING MENTOR GRAPHICS PRODUCTS UNDER THE HIGHER EDUCATION PROGRAM.	REVISIONS ARE DETAILED IN THE DOCUMENT:	No Revisions
PROJECT: VME Readout Electronics		
DESIGNED: Chris Ohlmann	LIST: VT48.xls	DOCUMENT NUMBER XKE-0820C REV. A
DRAWN: Chris Ohlmann	DATE: 3/28/2006	
CHECKED: -	SHEET: 05 OF 09	
APPROVED: -		

Last Modified at 7:20:22 PM on 3/28/2006
Schematic Size: 5 x 11
PCB File Name: @PCBFileName

H=4NA; V=4LA

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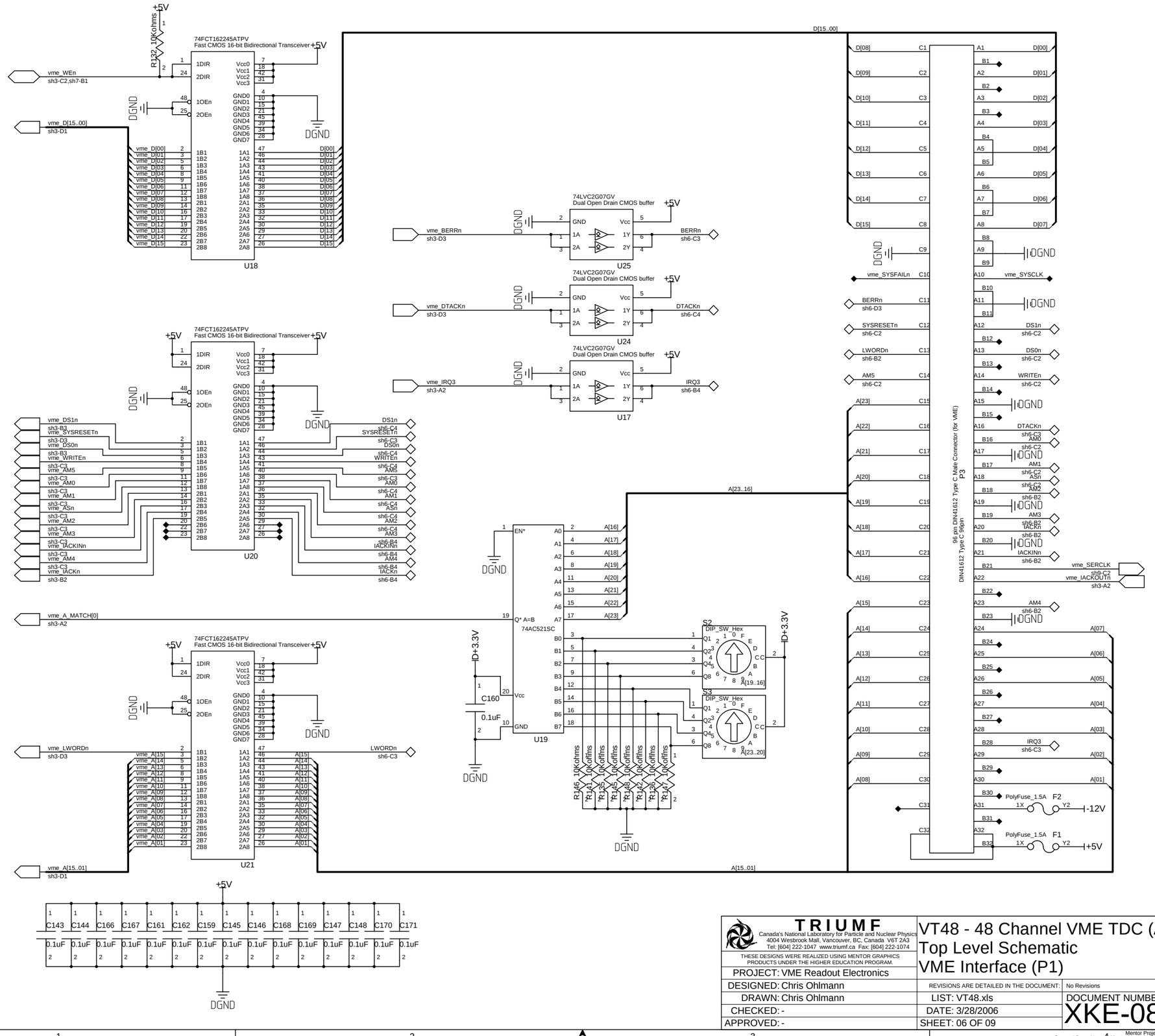

TRIUMF Canada's National Laboratory for Particle and Nuclear Physics 4004 Wesbrook Mall, Vancouver, BC, Canada V6T 2A3 Tel: [604] 222-1047 www.triumf.ca Fax: [604] 222-1074	VT48 - 48 Channel VME TDC (AMT3) Top Level Schematic VME Interface (P1)
THESE DESIGNS WERE REALIZED USING MENTOR GRAPHICS PRODUCTS UNDER THE HIGHER EDUCATION PROGRAM.	
PROJECT: VME Readout Electronics	
DESIGNED: Chris Ohlmann	REVISIONS ARE DETAILED IN THE DOCUMENT: No Revisions
DRAWN: Chris Ohlmann	LIST: VT48.xls
CHECKED: -	DATE: 3/28/2006
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	DOCUMENT NUMBER XKE-0820C REV. A

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Last Schematic Edit: 6.0.11
PCB File Name: @PCBFileName

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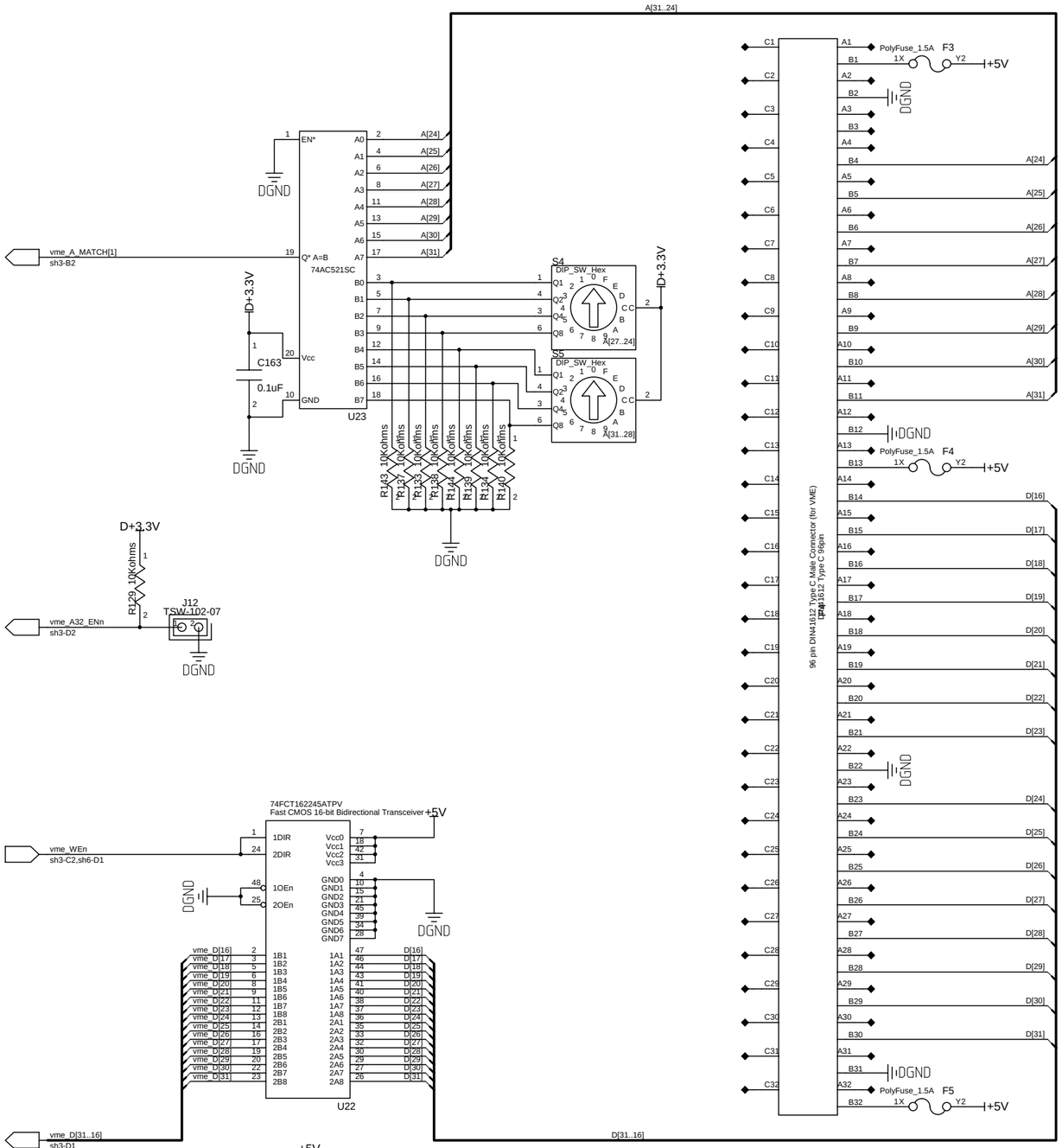

TRIUMF Canada's National Laboratory for Particle and Nuclear Physics 4004 Wesbrook Mall, Vancouver, BC, Canada V6T 2A3 Tel: [604] 222-1047 www.triumf.ca Fax: [604] 222-1074	VT48 - 48 Channel VME TDC (AMT3) Top Level Schematic VME Interface (P2)
THESE DESIGNS WERE REALIZED USING MENTOR GRAPHICS PRODUCTS UNDER THE HIGHER EDUCATION PROGRAM.	
PROJECT: VME Readout Electronics	
DESIGNED: Chris Ohlmann	REVISIONS ARE DETAILED IN THE DOCUMENT: No Revisions
DRAWN: Chris Ohlmann	LIST: VT48.xls — DOCUMENT NUMBER XKE-0820C — REV. A
CHECKED: -	DATE: 3/28/2006
APPROVED: -	SHEET: 07 OF 09

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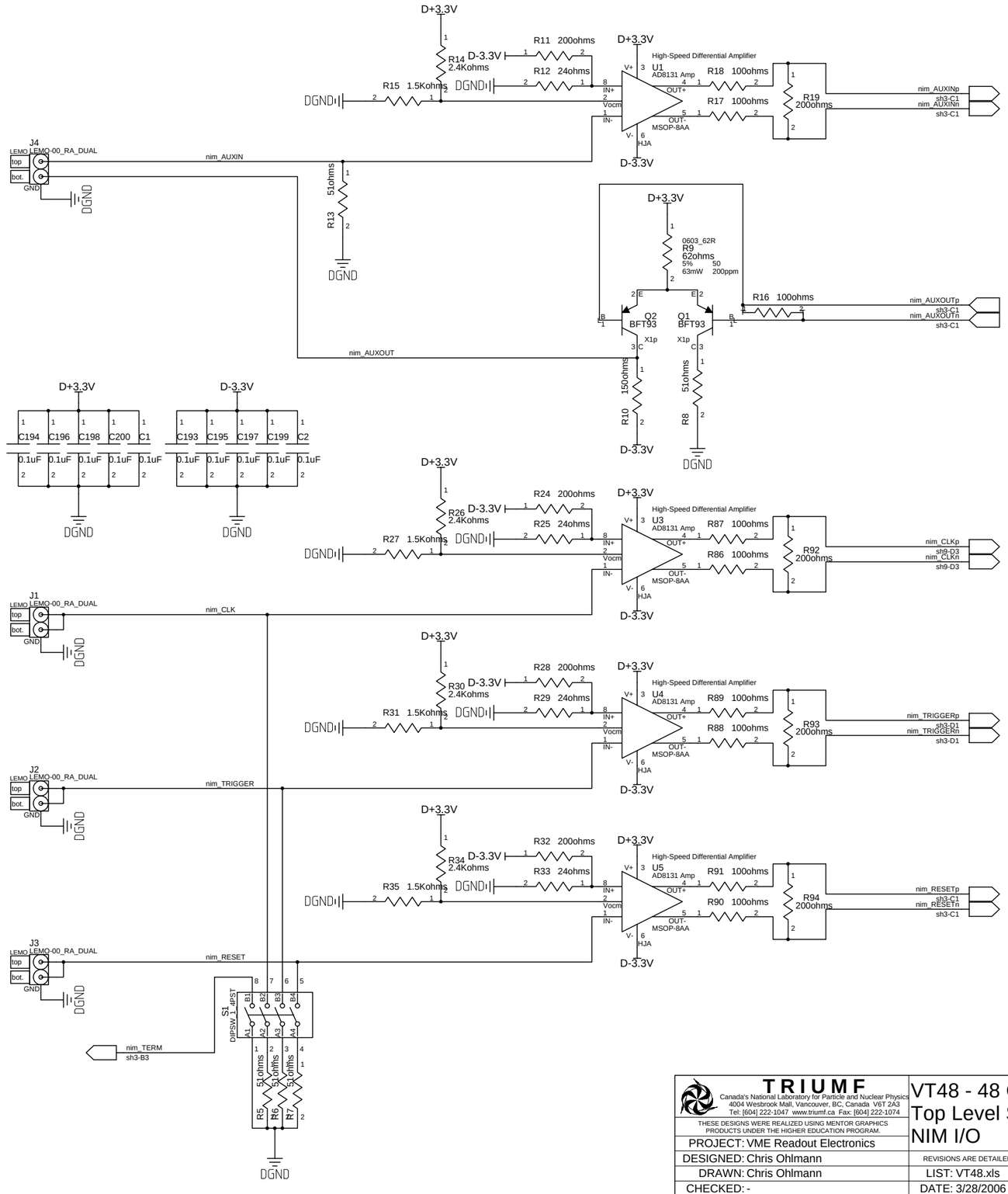

TRIUMF Canada's National Laboratory for Particle and Nuclear Physics, 4004 Westbrook Mall, Vancouver, BC, Canada V6T 2A3, Tel: [604] 222-1047 www.triumf.ca Fax: [604] 222-1074	VT48 - 48 Channel VME TDC (AMT3) Top Level Schematic NIM I/O	
THESE DESIGNS WERE REALIZED USING MENTOR GRAPHICS PRODUCTS UNDER THE HIGHER EDUCATION PROGRAM.		
PROJECT: VME Readout Electronics	REVISIONS ARE DETAILED IN THE DOCUMENT:	No Revisions
DESIGNED: Chris Ohlmann	LIST: VT48.xls	DOCUMENT NUMBER XKE-0820C / REV. A
DRAWN: Chris Ohlmann	DATE: 3/28/2006	
CHECKED: -	SHEET: 08 OF 09	
APPROVED: -		

Last Modified: 3/28/2006 2:07:24 PM on 3/28/2006
Hierarchical page 3 of 11
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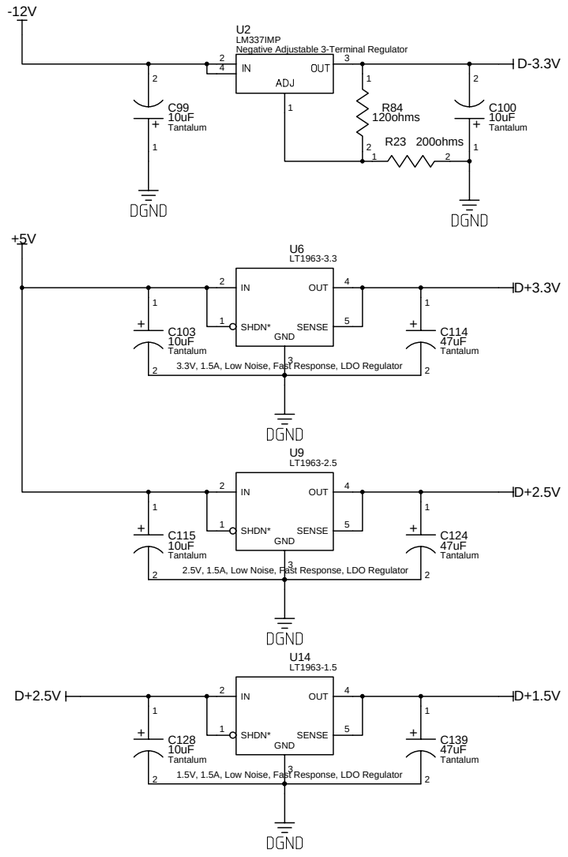
POWER REGULATORS



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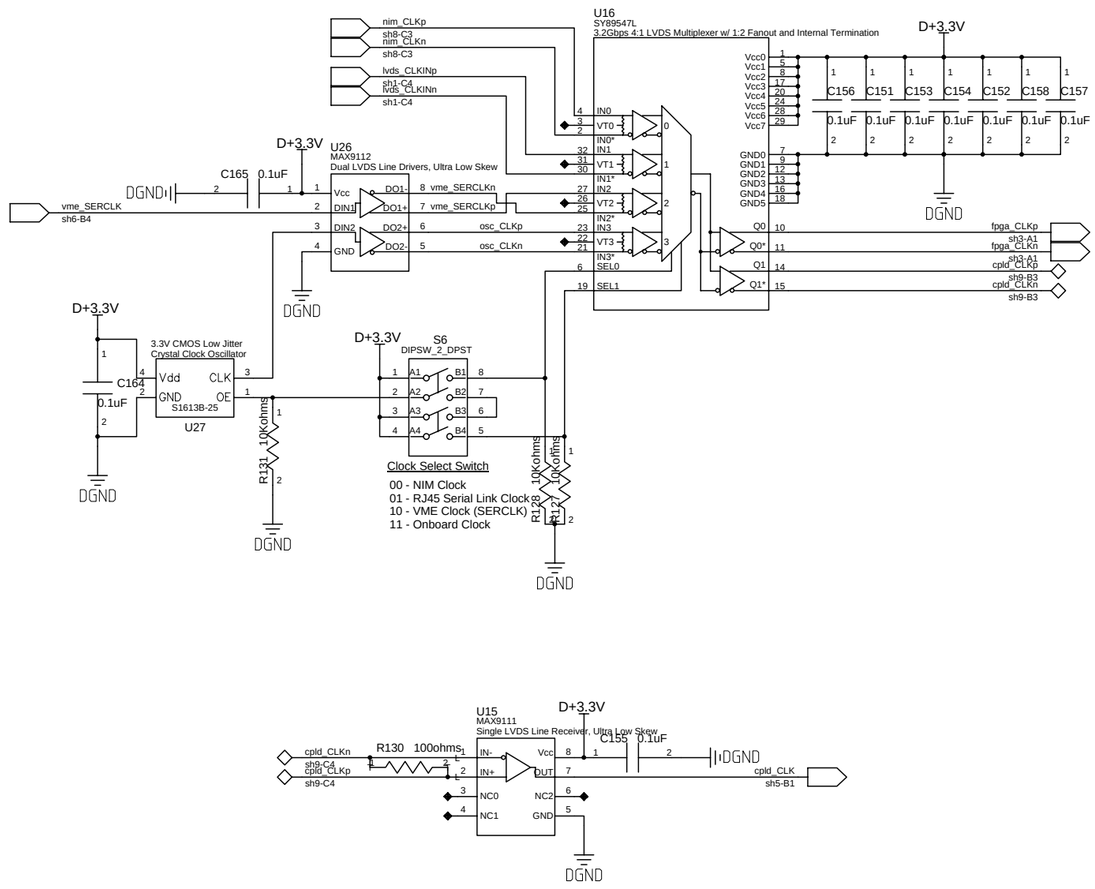

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THESE DESIGNS WERE REALIZED USING MENTOR GRAPHICS PRODUCTS UNDER THE HIGHER EDUCATION PROGRAM.		
PROJECT: VME Readout Electronics		
DESIGNED: Chris Ohlmann	REVISIONS ARE DETAILED IN THE DOCUMENT:	No Revisions
DRAWN: Chris Ohlmann	LIST: VT48.xls	DOCUMENT NUMBER XKE-0820C / REV. A
CHECKED: -	DATE: 3/28/2006	
APPROVED: -	SHEET: 09 OF 09	

Last Modified on 3/28/2006 2:07:27 PM on 3/28/2006
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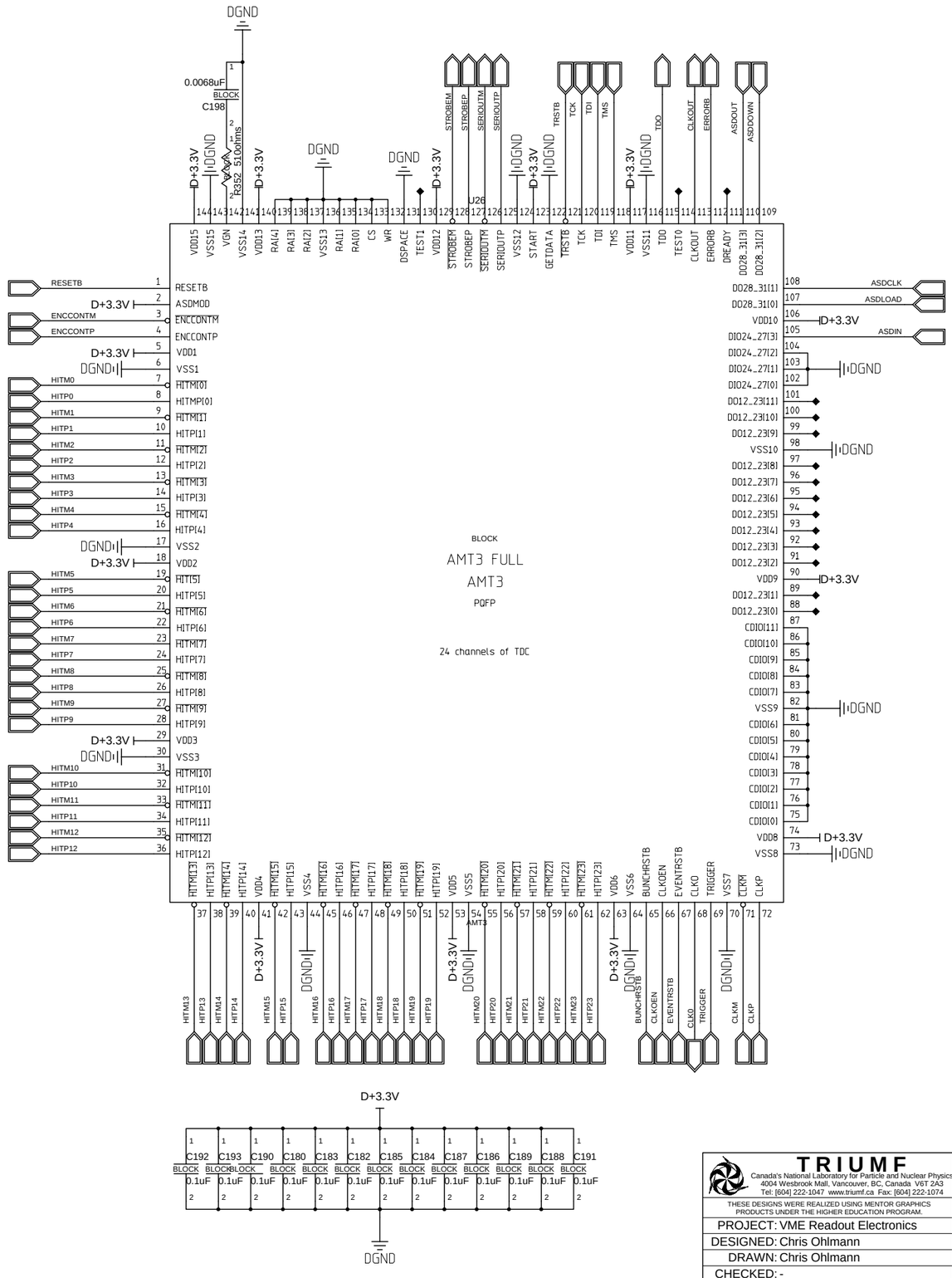

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THESE DESIGNS WERE REALIZED USING MENTOR GRAPHICS PRODUCTS UNDER THE HIGHER EDUCATION PROGRAM.		
PROJECT: VME Readout Electronics		
DESIGNED: Chris Ohlmann	REVISIONS ARE DETAILED IN THE DOCUMENT:	No Revisions
DRAWN: Chris Ohlmann	LIST: VT48.xls	DOCUMENT NUMBER XKE-0822C / REV. A
CHECKED: -	DATE: 3/28/2006	
APPROVED: -	SHEET: 01 OF 01	

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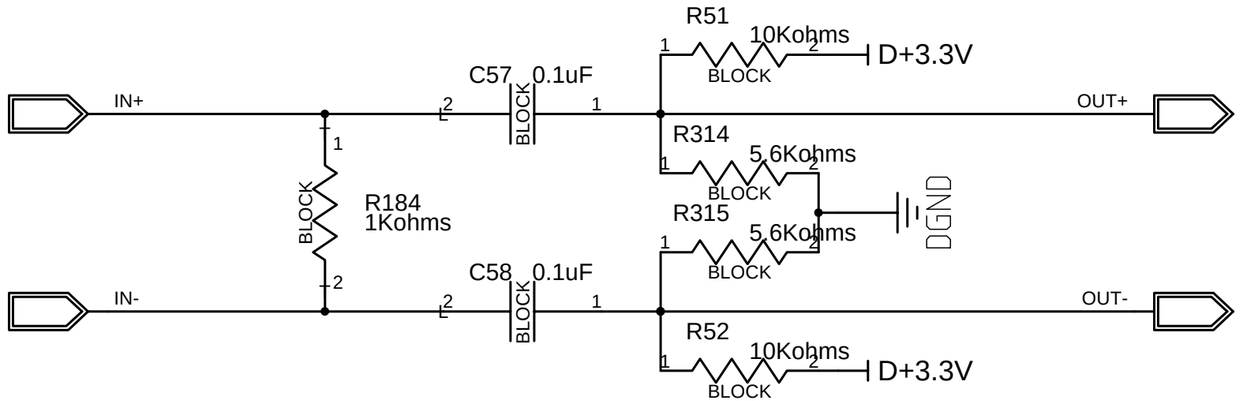

TRIUMF Canada's National Laboratory for Particle and Nuclear Physics 4004 Wesbrook Mall, Vancouver, BC, Canada V6T 2A3 Tel: [604] 222-1047 www.triumf.ca Fax: [604] 222-1074	VT48 - 48 Channel VME TDC (AMT3) ECL/LVDS Input Schematic -	
THESE DESIGNS WERE REALIZED USING MENTOR GRAPHICS PRODUCTS UNDER THE HIGHER EDUCATION PROGRAM.		
PROJECT: VME Readout Electronics		
DESIGNED: Chris Ohlmann	REVISIONS ARE DETAILED IN THE DOCUMENT:	No Revisions
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CHECKED: -	DATE: 3/28/2006	
APPROVED: -	SHEET: 01 OF 01	

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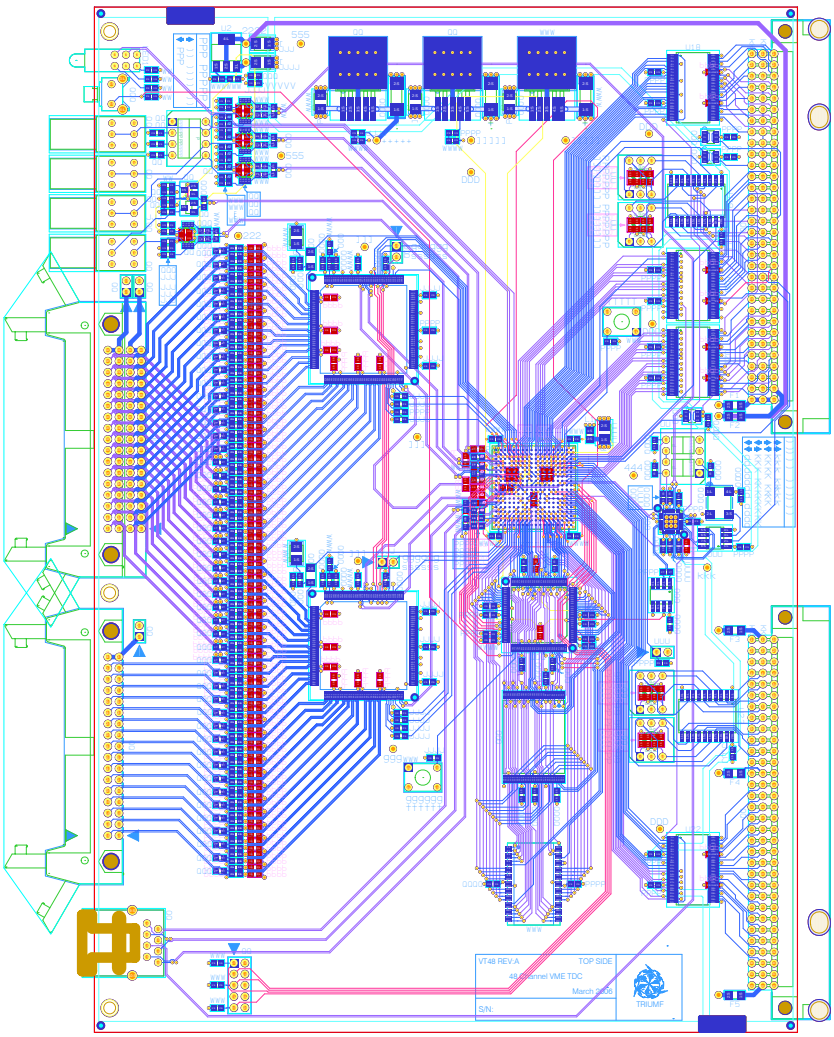
VT48 REV:A
TOP SIDE
48-Channel VME TDC
March 2015
S/N:
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