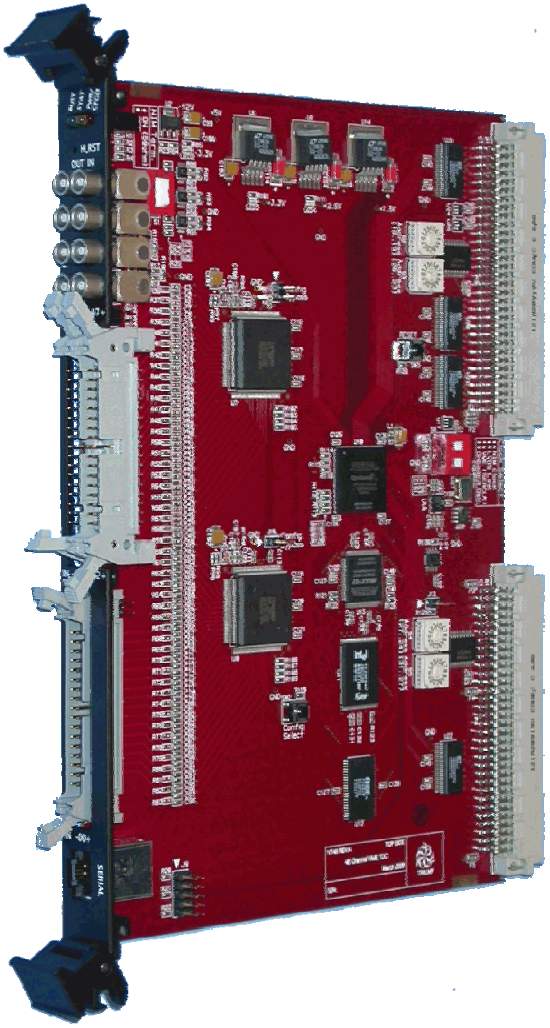
VT48 Rev. A

48-Channel Time-to-Digital (TDC) Module
User's Manual



July 9, 2007

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Table of Contents

TABLE OF CONTENTS ..... **I**

INTRODUCTION **1**

VME INTERFACE **2**

MODULE ADDRESSING 2
MEMORY MAP 2
VT48 Status Register 0x0000, Read Only *3*
Command Register 0x0004, Write Only *4*
AMT3 Device ID Register (Ch0-23) 0x0008, Read Only *4*
AMT3 Device ID Register (Ch24-47) 0x000C, Read Only *5*
Interrupt Vector Register 0x0010, Read / Write *5*
VT48 Control Register 0x0014, Read / Write *5*
AMT3 Status Registers 0x0020 – 0x0034, Read Only *6*
AMT3 Control Registers 0x0040 – 0x0078, Read / Write *7*
AMT3 Control Read-back Registers 0x0080 – 0x00B8, Read Only *9*
Input Buffer Status Register (DEBUG) 0x00FC, Read Only *10*
Input Buffer Ch0-23 (DEBUG) 0x0100, Read Only *11*
Input Buffer Ch24-47 (DEBUG) 0x0200, Read Only *11*
Readout FIFO 0x1000 – 0xFFFF, Read Only *11*

FRONT PANEL INTERFACE **12**

DATA INPUT PORTS 12
FRONT PANEL STATUS LEDS 12
HARD RESET SWITCH – H_RST 13
SERIAL COMMUNICATION PORT 13
NIM USER I/O 13

CLOCK DISTRIBUTION **15**

NIM CLOCK 15
LVDS SERIAL LINK 16
VME (SERCLK) 16
ONBOARD OSCILLATOR 16

EVENT DATA FORMAT **17**

Introduction

The VT48 is a 48 channel Time-to-Digital Converter (TDC) module. It is fully compliant with the VME specification supporting ALL addressing modes and D32 and D16 data access modes. The module was developed around the AMT-3 TDC that was originally designed for Monitored Drift Tube (MDT) readout in the ATLAS experiment.

Each of the 48 channels in the VT48 supports both LVDS and ECL differential signals and is capable of providing up to 0.450ns time resolution for rising edge and falling edge measurement (0.625ns resolution in standard configuration). If a module is configured for LVDS only then paired measurements are also possible. On any channel, the minimum for both pulse width and pulse separation is 5ns.

The VT48 was designed in conjunction with the VF48 Analog-to-Digital Converter (ADC) and VPC6 front-end power and control module. With the appropriate preamplifiers, these modules provide a complete VME data acquisition system that can be scaled up to support as many channels as desired.

VME Interface

The VT48 is fully compliant with the VME specification supporting ALL addressing modes and D32 and D16 data access modes.

Module Addressing

The address of a specific VT48 module may be set using the four (4) hexadecimal rotary switches: S2, S3, S4, and S5. The switches correspond to A[16..19], A[20..23], A[24..27], and A[28..31] respectively. Depending on the type of cycle presented on the VME bus (as determined by the AM[5..0] lines) the switches are treated differently:

- Extended (A32) mode, all switches are decoded.
- Standard (A24) mode, only switch S2 and S3 are decoded.
- Short (A16) mode, all switches are ignored. This mode is not recommended as only one module may be present on the bus unless a hard coded address is set in the firmware.

Memory Map

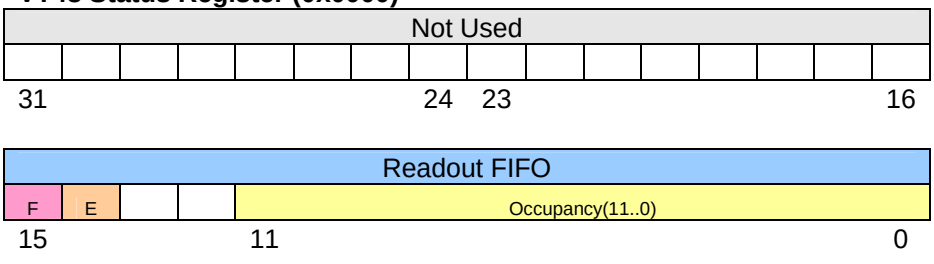
Address	Description	Access Type
0x0000	VT48 Status Register	Read Only
0x0004	Command Register	Write Only
0x0008	AMT3 Device ID Register (Ch0-23)	Read Only
0x000C	AMT3 Device ID Register (Ch24-47)	Read Only
0x0010	Interrupt Vector Register	Read / Write
0x0014	VT48 Control Register	Read / Write
0x0020	AMT3 Status (CSR16)	Read Only
0x0024	AMT3 Status (CSR17)	Read Only
0x0028	AMT3 Status (CSR18)	Read Only
0x002C	AMT3 Status (CSR19)	Read Only
0x0030	AMT3 Status (CSR20)	Read Only
0x0034	AMT3 Status (CSR21)	Read Only
0x0040	AMT3 Control (CSR0)	Read / Write
0x0044	AMT3 Control (CSR1)	Read / Write
0x0048	AMT3 Control (CSR2)	Read / Write
0x004C	AMT3 Control (CSR3)	Read / Write
0x0050	AMT3 Control (CSR4)	Read / Write
0x0054	AMT3 Control (CSR5)	Read / Write
0x0058	AMT3 Control (CSR6)	Read / Write
0x005C	AMT3 Control (CSR7)	Read / Write
0x0060	AMT3 Control (CSR8)	Read / Write
0x0064	AMT3 Control (CSR9)	Read / Write
0x0068	AMT3 Control (CSR10)	Read / Write
0x006C	AMT3 Control (CSR11)	Read / Write

Address	Description	Access Type
0x0070	AMT3 Control (CSR12)	Read / Write
0x0074	AMT3 Control (CSR13)	Read / Write
0x0078	AMT3 Control (CSR14)	Read / Write
0x0080	AMT3 Control Read-back (CSR0)	Read Only
0x0084	AMT3 Control Read-back (CSR1)	Read Only
0x0088	AMT3 Control Read-back (CSR2)	Read Only
0x008C	AMT3 Control Read-back (CSR3)	Read Only
0x0090	AMT3 Control Read-back (CSR4)	Read Only
0x0094	AMT3 Control Read-back (CSR5)	Read Only
0x0098	AMT3 Control Read-back (CSR6)	Read Only
0x009C	AMT3 Control Read-back (CSR7)	Read Only
0x00A0	AMT3 Control Read-back (CSR8)	Read Only
0x00A4	AMT3 Control Read-back (CSR9)	Read Only
0x00A8	AMT3 Control Read-back (CSR10)	Read Only
0x00AC	AMT3 Control Read-back (CSR11)	Read Only
0x00B0	AMT3 Control Read-back (CSR12)	Read Only
0x00B4	AMT3 Control Read-back (CSR13)	Read Only
0x00B8	AMT3 Control Read-back (CSR14)	Read Only
0x00FC	Input Buffer Status (Debug Only)	Read Only
0x0100	Ch0-23 Input Buffer (Debug Only)	Read Only
0x0200	Ch24-47 Input Buffer (Debug Only)	Read Only
0x1000	Readout FIFO	Read Only
.	.	.
.	.	.
.	.	.
0xFFFF	Readout FIFO	Read Only

VT48 Status Register 0x0000, Read Only

The status register is a read only register that contains information concerning the operational status of the VT48 module, such as buffer occupancy and error flags.

VT48 Status Register (0x0000)



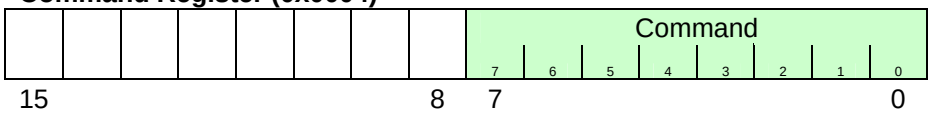
Bits	Description
31..16	Not used – Available for future use

Bits	Description
15	Full flag for Readout FIFO
14	Empty flag for Readout FIFO
13..12	Not Used – Available for future use
12..0	Occupancy Readout FIFO

Command Register 0x0004, Write Only

The command register is a write only register used to issue instructions to the VT48 for starting a variety of complex processes and simple tasks.

Command Register (0x0004)



Bits	Description
15..8	Not Used – Available for future use
7..0	Command

Command	Description
0x1	Write Configuration - loads values from AMT3 Control Registers into the actual devices - loads previous device configurations into Control Read-back Registers
0x2	Read Status - loads AMT3 Status Registers with current status from the devices
0x3	Read Device IDs - loads AMT3 device IDs into AMT3 Device ID Registers
0xF	Trigger
0x10	Global Reset
0x11	Event Count Reset
0x12	Bunch Count Reset

AMT3 Device ID Register (Ch0-23) 0x0008, Read Only

This device ID register is a read only register that contains the 32-bit chip identification code for the AMT3 controlling channels 0 through 23. Provided the AMT3 devices are operational and at least one “Read Device IDs” command has been issued, reading this register should always return 0x38B85031.

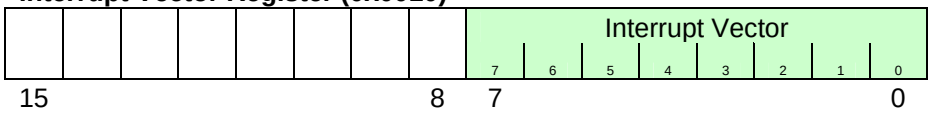
AMT3 Device ID Register (Ch24-47) 0x000C, Read Only

This device ID register is a read only register that contains the 32-bit chip identification code for the AMT3 controlling channels 24 through 47. Provided the AMT3 devices are operational and at least one "Read Device IDs" command has been issued, reading this register should always return 0x38B85031.

Interrupt Vector Register 0x0010, Read / Write

The interrupt vector register is a read / write register that holds the VT48 modules interrupt 'STATUS/ID', as specified in the VME priority interrupt bus. 32-bit access is supported, however, only an 8-bit vector is actually stored. This was done to enable support for all types of interrupt handlers.

Interrupt Vector Register (0x0010)

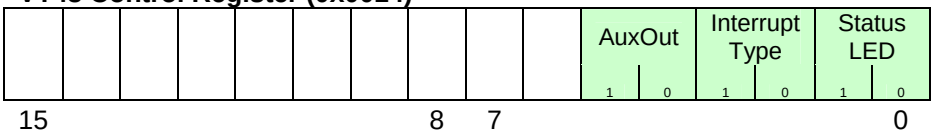


Bits	Description
31..8	Returns '0' if accessing in D16 or D32 modes
7..0	Interrupt Vector

VT48 Control Register 0x0014, Read / Write

The VT48 control register is a read / write register that holds various configuration parameters for the VT48 modules.

VT48 Control Register (0x0014)



Bits	Description
15..6	Not Used – Available for future use
5..4	Auxiliary Output (AUX_OUT) Function 0 – Auxiliary Input (AUX_IN)… Allows daisy chain configuration [default] 1 – Interrupt Request 2 – Force Logic '0' 3 – Force Logic '1'

Bits	Description
3..2	Interrupt Type 0 – Readout FIFO Almost Full [default] 1 – Event Ready for Readout 2 – External Interrupt from AUX_IN 3 – Disable Interrupts
1..0	Status LED Source 0 – Event Ready for Readout [default] 1 – AMT3 Device Error 2 – AMT3 Serial Link Activity 3 – Not used (available for future use)

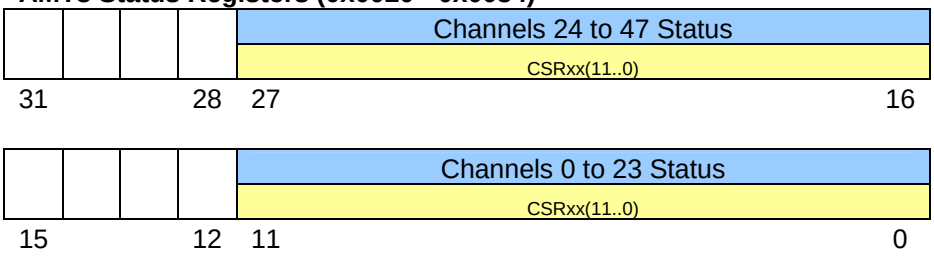
AMT3 Status Registers 0x0020 – 0x0034, Read Only

There are six (6) AMT3 status registers for the VT48 module. Each register is 32-bits wide and combines the two (2) appropriate 12-bit registers from the AMT3 device (CSR16 – CSR21). AMT status for Channels 0 to 23 and 24 to 47 are stored in the least significant and most significant words respectively. The AMT3 Status registers are refreshed when a "Read Status" command is issued, therefore, this command must be sent before reading these registers to obtain current device status.

Address	Description
0x0020	CSR16
0x0024	CSR17
0x0028	CSR18
0x002C	CSR19
0x0030	CSR20
0x0034	CSR21

The data format for each of the status registers is as follows:

AMT3 Status Registers (0x0020 - 0x0034)



Bits	Description
31..28	Not Used – Available for future use
27..16	CSRxx for AMT3 controlling channels 24 to 47
15..12	Not Used – Available for future use
11..0	CSRxx for AMT3 controlling channels 0 to 23

The following excerpt from the AMT3 User's Manual describes the information contained in each of the status registers. For more detail please see the AMT3 users manual.

Table. 5. Bit assignment of the status registers (all these registers are read only).

Address		11	10	9	8	7	6	5	4	3	2	1	0
0x0020	CSR16	rfifo_ empty (1) {11}	rfifo_ full (0) {10}	control_ parity (1) {9}	error_ flags (0) {8:0}								
0x0024	CSR17	ll_ empty (1) {23}	ll_ nearly_ full (0) {22}	ll_ over_ recover (1) {21}	ll_ over flow (0) {20}	ll_ write_address (0) {19:12}							
0x0028	CSR18	tfifo_ empty (1) {35}	tfifo_ nearly_ full (0) {34}	tfifo_ full (0) {33}	running (0) {32}	ll_ read_address (0) {31:24}							
0x002C	CSR19	coarse_ counter [0] (0) {47}	tfifo_ occupancy (0) {46:44}			ll_ start_address (0) {43:36}							
0x0030	CSR20	coarse_counter[12:1] (0) {59:48}											
0x0034	CSR21	general_ in[3:0] (DIO27~24) {71:68}				0 (0) {67}	0 (0) {66}	rfifo_ occupancy[5:0} (0) {65:60}					

() -- initial value at reset. {} --- JTAG bit No.

AMT3 Control Registers 0x0040 – 0x0078, Read / Write

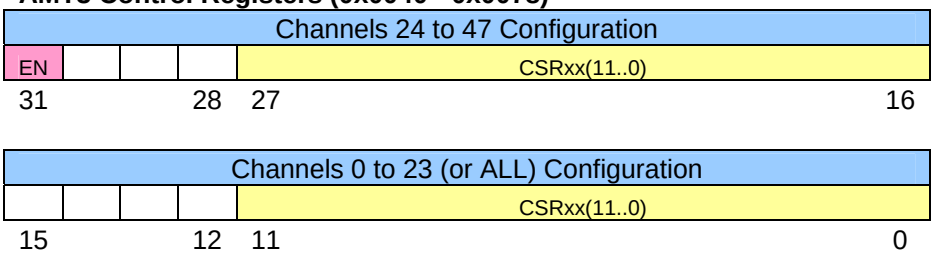
There are fifteen (15) control registers that hold the configuration data for the AMT3 devices on the VT48 module. Each register is 32-bits wide and holds data to be written into the two (2) appropriate 12-bit CSR registers from the AMT3 device (CSR0 – CSR14). Bit 31, of each register, is used to enable the most significant 16-bit word containing configuration data for the AMT3 controlling channels 24 – 47. If this bit is not set, the same data from the least significant word will be written into the appropriate CSR register for all channels or both AMT3s. After all AMT3 control registers have been set up as desired, a "Write Configuration" command must be written to the VT48 command register to load the configuration into the AMT3s.

Address	Description
0x0040	CSR0
0x0044	CSR1
0x0048	CSR2
0x004C	CSR3
0x0050	CSR4
0x0054	CSR5

0x0058	CSR6
0x005C	CSR7
0x0060	CSR8
0x0064	CSR9
0x0068	CSR10
0x006C	CSR11
0x0070	CSR12
0x0074	CSR13
0x0078	CSR14

The data format for each of the status registers is as follows:

AMT3 Control Registers (0x0040 - 0x0078)



Bits	Description
31	EN bit – Enables Configuration Word for Channels 24 – 47
30..28	Not Used – Available for future use
27..16	EN = 1: CSRxx for AMT3 controlling channels 24 to 47 EN = 0: Not Used
15..12	Not Used – Available for future use
11..0	EN = 1: CSRxx for AMT3 controlling channels 0 to 23 EN = 0: CSRxx for ALL channels

The following excerpt from the AMT3 User's Manual describes the information contained in each of the control registers. For more detail please see the AMT3 user's manual.

Address		BIT											
		11	10	9	8	7	6	5	4	3	2	1	0
0x0040	CSR0	global_reset (0) {11}	error_reset (0) {10}	disable_encode (0) {9}	enable_errrst_bcrevr (0) {8}	test_mode (0) {7}	test_invert (0) {6}	enable_direct (0) {5}	disable_ringosc (0) {4}	clkout_mode (0) {3:2}		pll_multi (0) {1:0}	
0x0044	CSR1	mask_window (0) {23:12}											
0x0048	CSR2	search_window (0) {35:24}											
0x004C	CSR3	match_window (0) {47:36}											
0x0050	CSR4	reject_count_offset (0) {59:48}											
0x0054	CSR5	event_count_offset (0) {71:60}											
0x0058	CSR6	bunch_count_offset (0) {83:72}											
0x005C	CSR7	coarse_time_offset (0) {95:84}											
0x0060	CSR8	count_roll_over (FFF) {107:96}											
0x0064	CSR9	strobe_select (1/0) {119:118}		readout_speed (0) {117:116}		width_select (0) {115:113}			error_test (0) {112}	tdc_id (0) {111:108}			
0x0068	CSR10	enable_auto_reject (1) {131}	enable_l1occup_readout (0) {130}	enable_match (1) {129}	enable_mask (0) {128}	enable_relative (0) {127}	enable_serial (0) {126}	enable_header (0) {125}	enable_trailer (0) {124}	enable_rejected (0) {123}	enable_pair (0) {122}	enable_trailing (0) {121}	enable_leading (1) {120}
0x006C	CSR11	enable_rofull_reject (0) {143}	enable_l1full_reject (0) {142}	enable_trfull_reject (0) {141}	enable_errmark (0) {140}	inclk_boost (0) {139}	enable_ermark_rejected (0) {138}	enable_errmark_ovr (0) {137}	enable_l1ovr_detect (0) {136}	enable_mreset_code (0) {135}	enable_resetcb_sepa (0) {134}	enable_mreset_evrst (0) {133}	enable_setcount_bcrst (0) {132}
0x0070	CSR12	enable_sepa_readout (0) {155}	enable_sepa_bcrst (0) {154}	enable_sepa_evrst (0) {153}	enable_error [8:0] (1FF) {152:144}								
0x0074	CSR13	enable_channel[11:0] (FFF) {167:156}											
0x0078	CSR14	enable_channel[23:12] (FFF) {179:168}											

AMT3 Control Read-back Registers 0x0080 – 0x00B8, Read Only

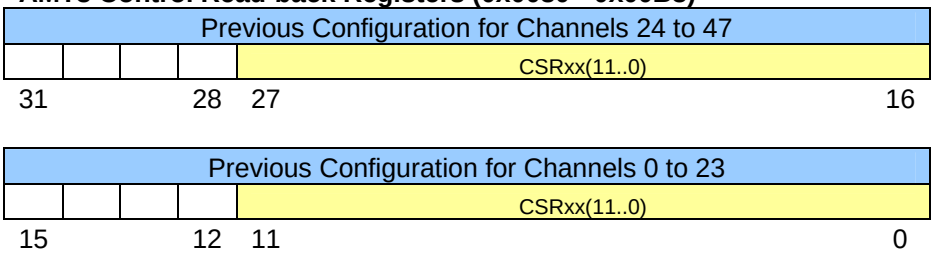
There are fifteen (15) AMT3 control read-back registers in the VT48 module. Each register is 32-bits wide and contains control data that has been read back from the two (2) appropriate 12-bit CSR registers (CSR0 – CSR14) in the AMT3 devices. The registers are updated when a "Write Configuration" command is written to the VT48 command register. Since the AMT3 devices only support destructive writing of control data, the

registers indicate the previous configuration that was present before the last “Write Configuration” command was issued.

Address	Description
0x0080	CSR0
0x0084	CSR1
0x0088	CSR2
0x008C	CSR3
0x0090	CSR4
0x0094	CSR5
0x0098	CSR6
0x009C	CSR7
0x00A0	CSR8
0x00A4	CSR9
0x00A8	CSR10
0x00AC	CSR11
0x00B0	CSR12
0x00B4	CSR13
0x00B8	CSR14

The data format for each of the status registers is as follows:

AMT3 Control Read-back Registers (0x0080 - 0x00B8)

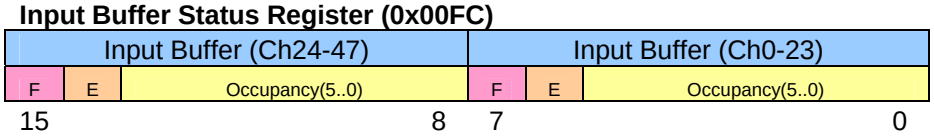


Bits	Description
31..28	Not Used – Available for future use
27..16	CSRxx for AMT3 controlling channels 24 to 47
15..12	Not Used – Available for future use
11..0	CSRxx for AMT3 controlling channels 0 to 23

Input Buffer Status Register (DEBUG) 0x00FC, Read Only

The input buffer status register is a read only register that contains the occupancy and status of the input FIFOs buffering event data from the two AMT3 devices.

Input Buffer Status Register (0x00FC)



Bits	Description
15	Full flag for Input Buffer (Channel 24 – 47)
14	Empty flag for Input Buffer (Channel 24 – 47)
13..8	Occupancy of Input Buffer (Channel 24 – 47)
7	Full flag for Input Buffer (Channel 0 – 23)
6	Empty flag for Input Buffer (Channel 0 – 23)
5..0	Occupancy of Input Buffer (Channel 0 – 23)

Input Buffer Ch0-23 (DEBUG) 0x0100, Read Only

The input buffer register, for channels 0 – 23, is a read only register containing the oldest 32-bit serial data packet that has been read from the AMT3. This register is for debug purposes only and should not be read in normal operation as it may cause problems with event synchronization.

Input Buffer Ch24-47 (DEBUG) 0x0200, Read Only

The input buffer register, for channels 24 – 47, is a read only register containing the oldest 32-bit serial data packet that has been read from the AMT3. This register is for debug purposes only and should not be read in normal operation as it may cause problems with event synchronization.

Readout FIFO 0x1000 – 0xFFFF, Read Only

The readout FIFO is a read only register that holds the event data that has been collected from the AMT3s. Provided the FIFO is not empty, reading any of the addresses within the range 0x1000 – 0xFFFF will return the oldest valid data packet. Occupancy status for the readout FIFO should be checked in the VT48 status register prior to reading data to ensure valid event data is obtained.

Front Panel Interface

Data Input Ports

The VT48 module supports 48 differential input channels organized in groups of 16 to easily interface with front-end electronics. Each input channel accepts both LVDS and ECL differential signals. In addition to the 16 differential input pairs, pins 33 and 34 of the input connectors may be connected to the module GND for cable shielding using jumpers J8, J5, and J7.

Pin	Description (P2)	Description (P1_bot)	Description (P1_top)
1	Channel 0 (+)	Channel 16 (+)	Channel 32 (+)
2	Channel 0 (-)	Channel 16 (-)	Channel 32 (-)
3	Channel 1 (+)	Channel 17 (+)	Channel 33 (+)
4	Channel 1 (-)	Channel 17 (-)	Channel 33 (-)
. . .	. . .	. . .	. . .
31	Channel 15 (+)	Channel 31 (+)	Channel 47 (+)
32	Channel 15 (-)	Channel 31 (-)	Channel 47 (-)
33	J8: ON – GND OFF – No connection	J5: ON – GND OFF – No connection	J7: ON – GND OFF – No connection
34	J8: ON – GND OFF – No connection	J5: ON – GND OFF – No connection	J7: ON – GND OFF – No connection

Front Panel Status LEDs

There are three (3) LEDs located to indicate the current status of the VT48 module. Their functionality is as follows:

BUSY – VME Busy LED (Green)

ON	The VT48 is being accessed through the VME interface
OFF	The VME interface on the VT48 is inactive

STAT – Status LED (Yellow)

Functionality of the status LED is defined by the Status LED Source setting in the VT48 control register. If the Status LED is turned on one of the following is true:

- A complete event is available for readout in the readout buffer
- An error has occurred in one of the AMT3 devices… for more detail on the error read the AMT3 status registers
- AMT3 Serial Link is Active

PWR/CFG – Power LED (Red)

ON	The VT48 module is being powered
OFF	The VT48 is not powered

Hard Reset Switch – H_RST

A hard reset switch, accessible through a pin hole on the front panel, may be used to reset the VT48 module to initial conditions. Pressing the hard reset switch reprograms the FPGA with the default configuration located in the on-board flash memory.

Serial Communication Port

The VT48 is equipped with an RJ45 communication port, located on the front panel. This port was added for interoperability with the VF48 ADC module, which implements a custom full duplex serial communication protocol developed by Jean-Pierre Martin at the University of Montreal. Currently this feature has not been implemented in VT48 firmware.

NIM User I/O

There are four (4) pairs of NIM input and output signals, accessible on the front panel, that are used to provide extra control and synchronization features for the VT48 module.

Each of the main control signals, CLK, TRIG, and RESET, have two lemo connectors that are functionally identical. The two connectors have been shorted together to allow a daisy chain configuration. One connector acts as an input and the other as an output that may be connected to the next module in the chain. Although these lines may be daisy chained between multiple modules care must be taken. Connecting them in this manner will introduce a delay between different modules in the system. Depending on the timing resolution required, this may need to be corrected through calibration in the data acquisition system.

When driving these signals in a daisy chain configuration using standard NIM logic, it is critical that the NIM Termination switch, S1, be set correctly. To maintain proper signal levels only one module in the chain should have its NIM termination jumper set to ON.

In addition to these signals, the VT48 module has both an auxiliary input and an auxiliary output. The input and output are not shorted together like the other NIM controls, but are rather true NIM inputs and outputs. Neither of auxiliary ports are affected by the NIM termination switch.

CLK – Clock Input / Output

The CLK ports enable the VT48 to operate from an external clock for synchronizing multiple modules within a system or experiment. Provided the clock select switch is correctly set to NIM Clock (00), the CLK signal is converted from standard NIM logic to LVDS before entering the PLL circuitry of the onboard FPGA. In the PLL, the frequency is doubled and distributed to the two (2) AMT3's.

TRIG – Trigger Input / Output

The TRIG signal is used to trigger VT48 module. The signal is converted from NIM logic to LVDS before it is routed to the FPGA where it is processed and redistributed to the two (2) AMT3's. It is important to note that up to one clock period of time walk can occur depending on when in the clock period the trigger occurs. This is not corrected automatically in the VT48 module and requires the user to dedicate one channel in the overall system for correcting this problem.

RESET – Counter Reset Input / Output

The RESET signal is used to reset the coarse time counters in the VT48 module. The signal is converted from NIM logic to LVDS before it is routed to the FPGA where it is processed. It is critical that this signal be generated identically for all VT48 modules in the system at least once. This is necessary to ensure that the time counters for all modules in the system are properly synchronized and have the same time reference.

AUX_IN Signal

The AUX_IN signal is used to provide an extra user definable input to the VT48 module. Functionality of this signal is defined by settings in the VT48 Control Register. The input may be used to generate an interrupt on the VME bus, basically acting as an external interrupt.

The AUX_IN signal is a standard NIM input with integrated 50ohm termination and is not affected by the NIM Termination Switch. For this reason, this signal can not be daisy chained between modules.

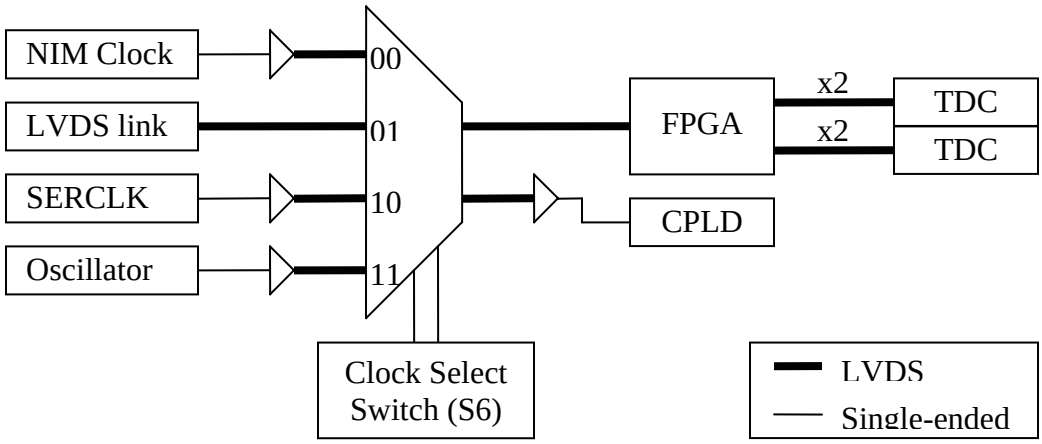
AUX_OUT Signal

The AUX_OUT signal is used to provide an extra user definable output to the VT48 module. Functionality of this signal is defined in the VT48 Control Register. By default, the AUX_OUT signal is tied directly to the AUX_IN signal to allow a daisy chain configuration. It may also be used to indicate that the VT48 module has a pending interrupt request on VME bus or as a general I/O by forcing the output high or low.

The AUX_OUT signal is a standard NIM logic output syncing 16mA (-0.8V with a 50ohm load).

Clock Distribution

The VT48 module has a variety of clock configurations that may be used depending on the desired overall system configuration. The Clock Select Switch, S6, must be set according to the desired system clock source.



Clock Select (S6)	Clock Mode	Maximum Jitter[1]	Module-Module Skew[2]
00	NIM Clock	**Nim-lvds + <10ps**	**<200ps ???**
01	LVDS Link	<10ps	<200ps
10	VME (SERCLK)	250ps	<1ns
11	Onboard Osc.	<250ps	< Clock Period / 2

NIM Clock

In this mode, the system clock is provided through the external NIM clock input.

This configuration allows the clock signal to be daisy chained from one VT48 to the next using standard lemo cables. Care must be taken in this configuration as daisy chaining will result in clock delays between modules. These delays must be taken into account during calibration of the system to achieve optimal performance from the TDCs.

[1] Jitter is a function of the random noise inherent in the clock distribution. There is no calibration that can improve the jitter performance of a VT48.

[2] Module-to-module skew is the maximum skew between different VT48 modules that are clocked with the same clock source. If a greater timing accuracy is required, the system may be calibrated by adding delays to the clock line.

It is also important to correctly set the NIM Termination switch, S1, when daisy chaining the NIM signals. Exactly one VT48 in the chain should have the NIM Termination enabled and all other modules in the chain should have it disabled.

LVDS Serial Link

In this mode, the system clock is provided through the external LVDS serial link. This interface was included to be compatible with the VF48 developed by Jean-Pierre Martin at the University of Montreal and all associated systems.

VME (SERCLK)

In this mode, the system clock is provided through the SERCLK line of the VME interface. This interface may be used to provide a system clock that is easily distributed to a number of modules through a standard VME backplane. Although it is convenient, it is not a recommended for systems that require high precision timing due to the inherent noise and delays on the VME bus.

Onboard Oscillator

In this mode, the system clock is provided using an clock oscillator present on the TDC48 board. This is the ideal configuration when using a single TDC48 module that is not synchronized with other external systems. However, if multiple modules are present or it is required to synchronize with other elements in the system this mode can not be used, as it is impossible to synchronize the oscillators between modules.

Event Data Format

Event data is automatically read from two AMT3 devices corresponding to channels 0-23 and 24-47. It is then processed and merged into the readout FIFO. A single event frame consists of a VT48 header, all relevant event data from both AMT3 devices, and a VT48 trailer.

Data received from each AMT3 depends on the device configuration and also on the number of hits received on the related channels. Typically there will be a device header, a number of single edge time measurements, and a device trailer. Under certain circumstances, error and mask flag packets may be included along with the measurement data. These indicate an error condition in the AMT device or that a hit has occurred within the defined mask window for the specified channel respectively. It should be noted that event data from the two AMT3 devices are merged as the data packets are received and not as complete events.

NOTE: It is critical that each AMT3 device in the readout system is configured with a unique TDC ID in order to properly decode the full channel number. If duplicate TDC IDs are present it will not be possible to uniquely identify a single channel. Please refer to the AMT3 Control Registers 0x0040 – 0x0078, Read / Write section of this manual for TDC ID settings.

VT48 Event Header:

0 0 0 1	CH0-23 TDC ID	CH24-47 TDC ID	0 0 0 0	Event ID
31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

AMT3 Device Header:

1 0 1 0	TDC ID	Event ID	Bunch ID
31 30 29 28	27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0

Single Edge Time Measurement Data:

0 0 1 1	TDC ID	Channel	T	E	Hit Time
31 30 29 28	27 26 25 24	23 22 21 20 19	18	17	16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

T: Edge Type (1 = leading edge, 0 = trailing edge)
E: Error

Paired Measurement Data:

0 1 0 0	TDC ID	Channel	Width	Hit Time (Leading Edge)
31 30 29 28	27 26 25 24	23 22 21 20 19	18 17 16 15 14 13 12 11	10 9 8 7 6 5 4 3 2 1 0

Mask Window Flags:

0 0 1 0	TDC ID	Channel Mask Flags
31 30 29 28	27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

AMT Device Error Flags:

0 1 1 0	TDC ID	0	0	0	0	0	0	0	0	0	0	Error Flags*
31 30 29 28	27 26 25 24	23	22	21	20	19	18	17	16	15	14	13 12 11 10 9 8 7 6 5 4 3 2 1 0

* For detailed description of AMT3 errors please see the device manual.

AMT3 Device Trailer:

1 1 0 0	TDC ID	Event ID	Word Count
31 30 29 28	27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

VT48 Event Trailer:

1 0 0 0	CH0-23 TDC ID	CH24-47 TDC ID	0 0 0 0	Event ID
31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0