UNI EN ISO 9001
CERT. N. 9105.CAEN

V1190 - V1290
a New Family of Multi-Hit TDC

HPTDC Workshop

CERN, 13th May 2003

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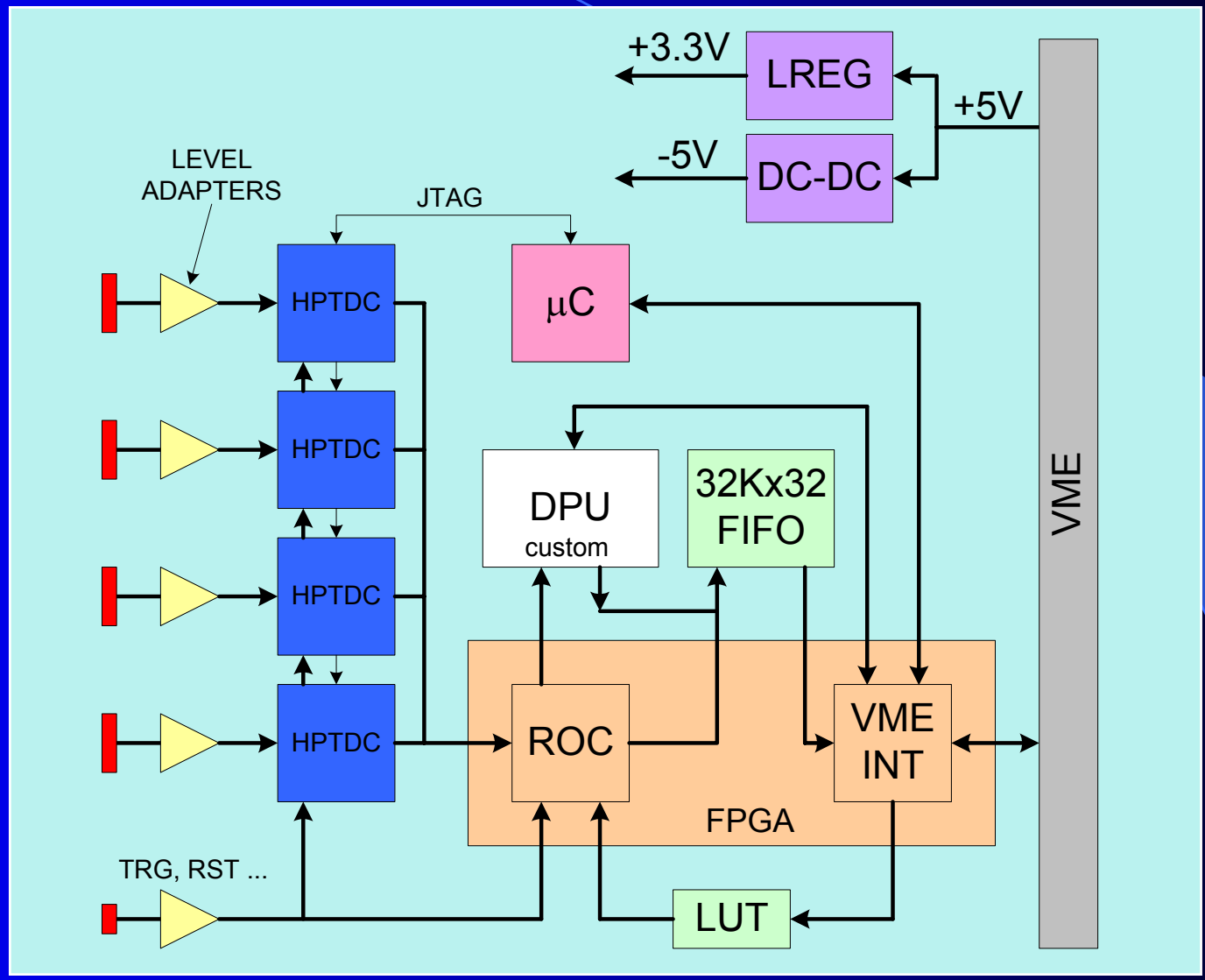
General description

- VME 6U modules for physics applications
- One board can house 4 HPTDC chips
- 128 channels $\Rightarrow$ 800/200/100ps LSB
- 32 channels $\Rightarrow$ 25ps LSB
- Automatic INL compensation
- Easy TDC programming via high level opcodes
- Advanced VME interface
- It can house a custom data processing unit

The Family

Model	# ch.	LSB	Range	Input	Connector
V1190A	128	100ps	50µs	ECL / LVDS	1.27 mm double density
V1190B	64	100ps	50µs	ECL / LVDS	1.27 mm double density
V1290A	32	25ps	50µs	ECL / LVDS	2.54 mm standard
V1290N	16	25ps	50µs	NIM	LEMO Coax

Block Diagram



VME Interface

- VME64x compliant
- Addressing: Standard, Geographical, Multicast
- Readout: D32, BLT, MBLT, CBLT32/64, up to ~40MB/s
- Event building oriented readout
- 7 level Interrupter
- 2eVME or 2eSST coming (~100MB/s expected)
- Live insertion
- Firmware upgrade via VME
- Power supply: +5V (about 15W)

Front Panel I/O

INPUTS

32/64/128 ECL / LVDS, flat cable	110 Ω
16 NIM, coaxial cable	50 Ω

CONTROL CONNECTOR

External Clock	ECL
TDC Reset (T_0)	ECL
Trigger (L1A)	ECL and NIM
Clear	ECL
L2A	ECL
L2R	ECL
Aux Input	ECL
Prog Output (Full, Data Ready…)	ECL

Data Processing Unit

- Optional DPU available for all the users which can develop their firmware (VHDL and/or C programs) for the specific applications
- 10x5 cm mezzanine card
- Interface to MB: two 32 bit data busses + 16 bit address bus + 20 general purpose I/Os
- The firmware of the DPU can be loaded from the VME
- DPU for Alice Group: DSP Shark,100Kgate FPGA, 64Kbytes memory buffer

TDC JTAG Programming

- The programming of the TDC chips via JTAG is completely managed by the internal microcontroller which receives instructions from the VME
- The μC takes care of:
  - trigger matching or continuous storage mode
  - trigger window
  - resolution
  - calibration parameters
  - error detection, etc.
- It is possible to save the user settings and load it at power-on

INL Compensation

- Data read from the TDCs are corrected by the ROC at 40MHz by means of a Look-Up Table
- The compensation is automatic and dead-time free
- The LUT has 1024 independent values per channel (single channel calibration)
- The calibration of the LUT is done by CAEN but it can be overwritten by the user

Test Results

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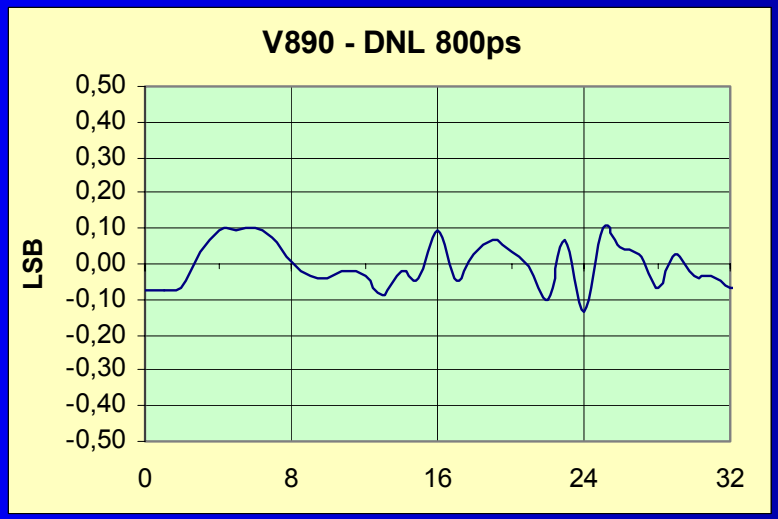
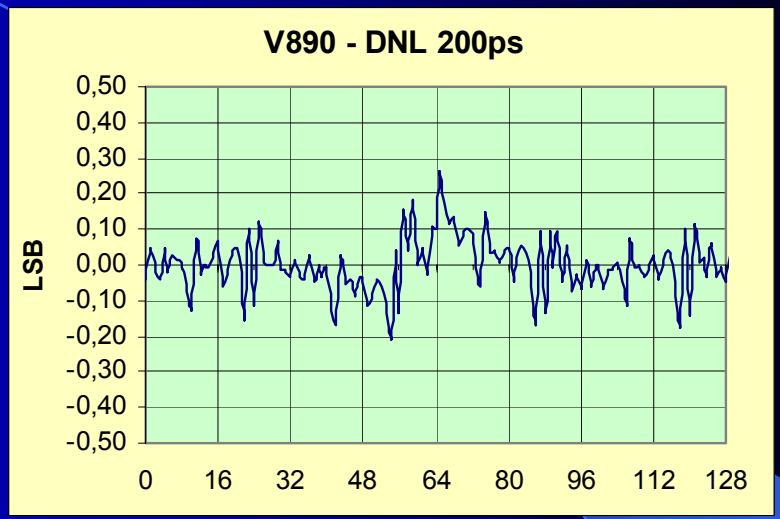
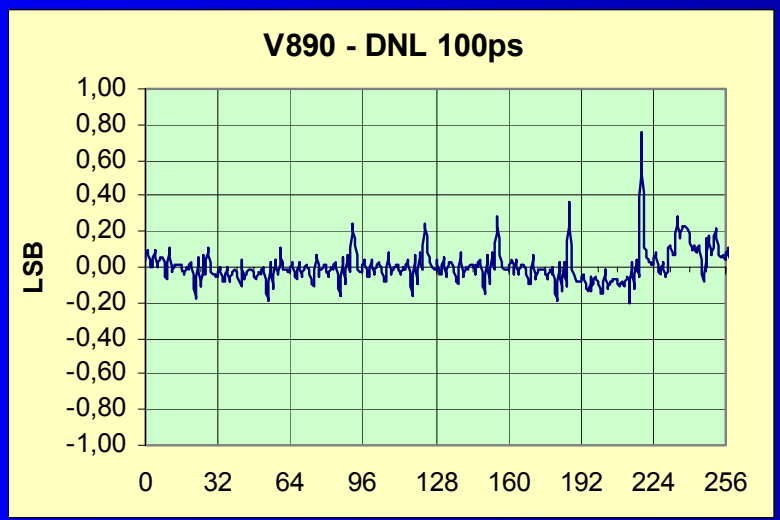
Test Setup

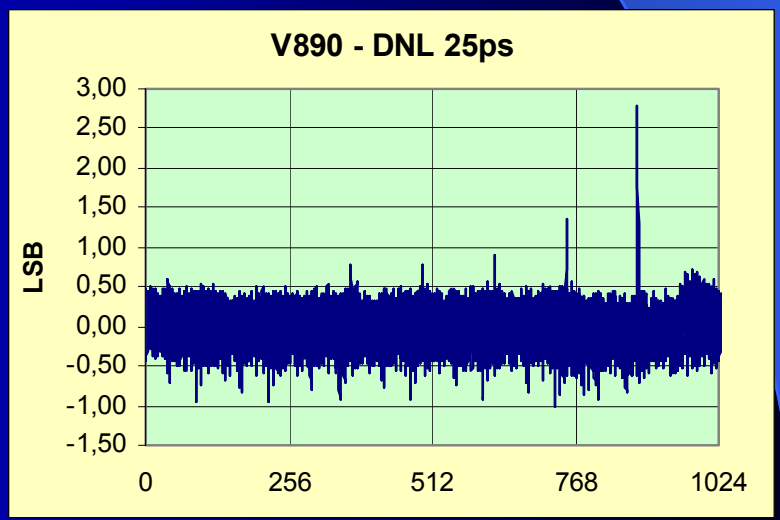
- All tests and measurements have been done on a previous prototype of the board called V890
- From the HPTDC point of view, the module V890 is identical to the family V1190/V1290
- The HPTDC used for linearity test is rev. 1.1 (July 2001)
- The V890 does not have the LUT for the automatic INL compensation; the LUT has been implemented by software after the readout
- Fixed delays are obtained with cables; random hit distribution is generated by means of two uncorrelated pulse generators
- INL is calculated from the DNL (not measured)

DNL (not compensated)



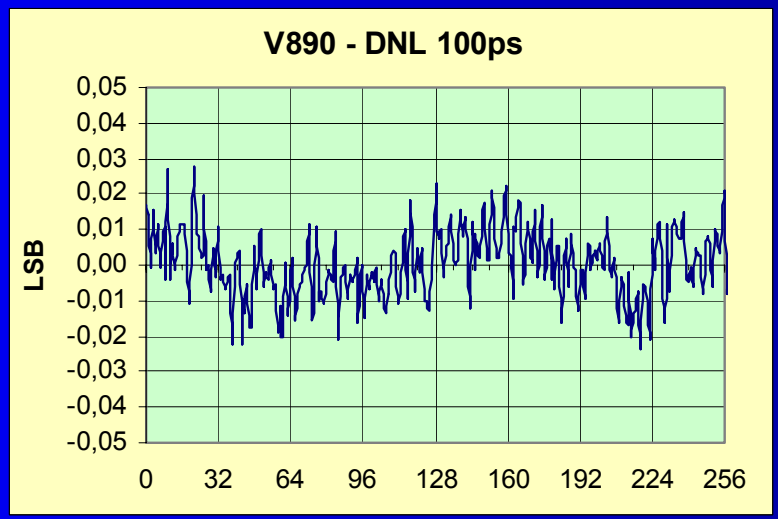


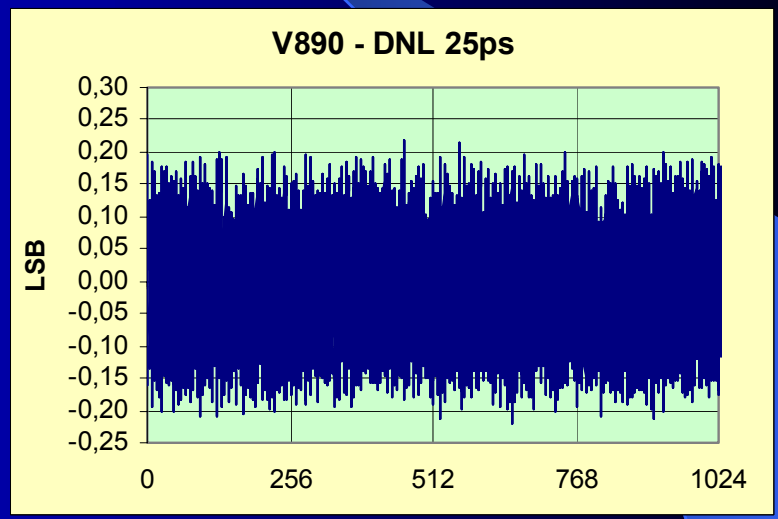




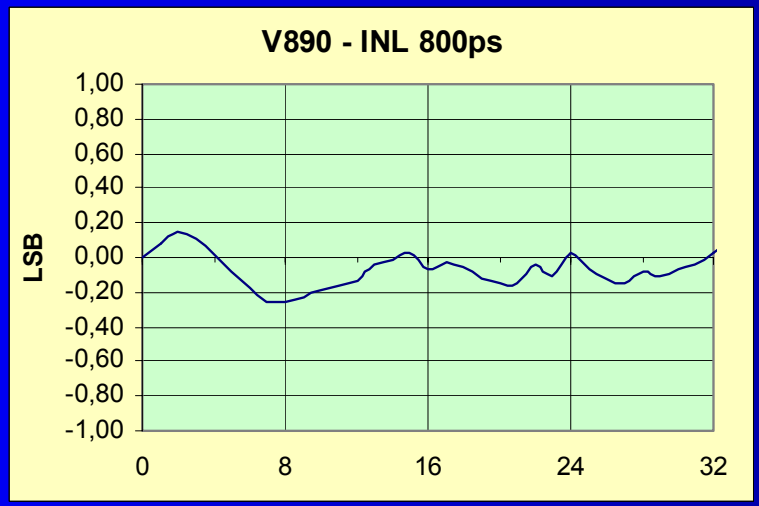
DNL (not compensated)

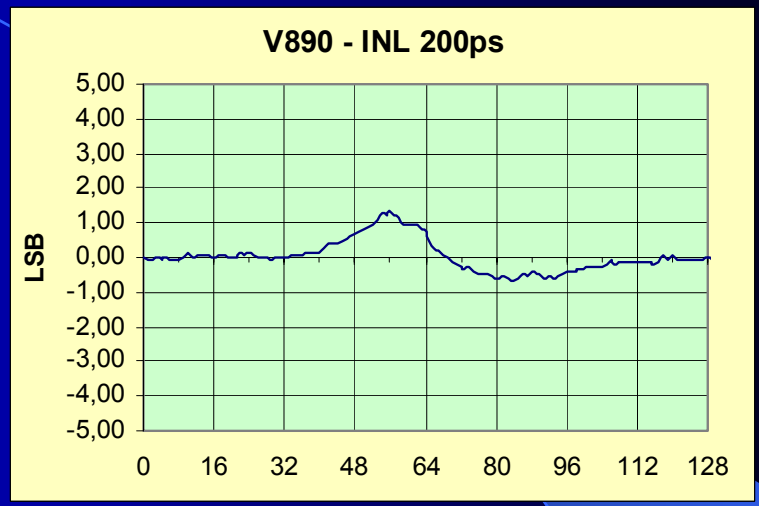
start-stop measurement

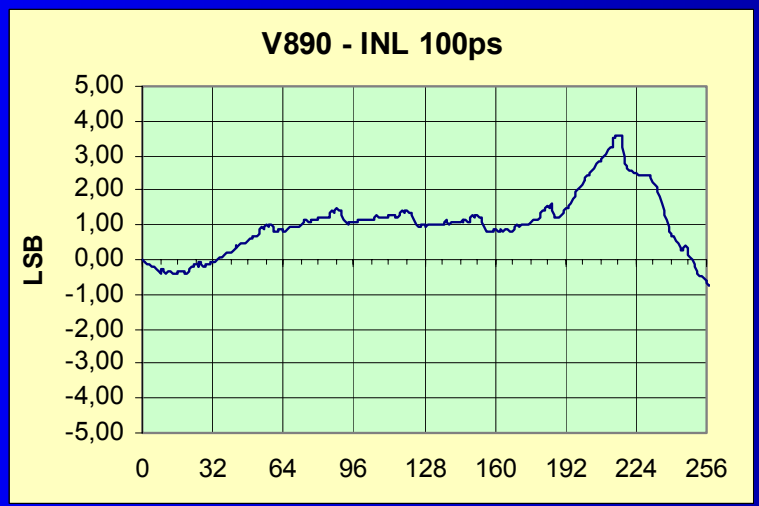


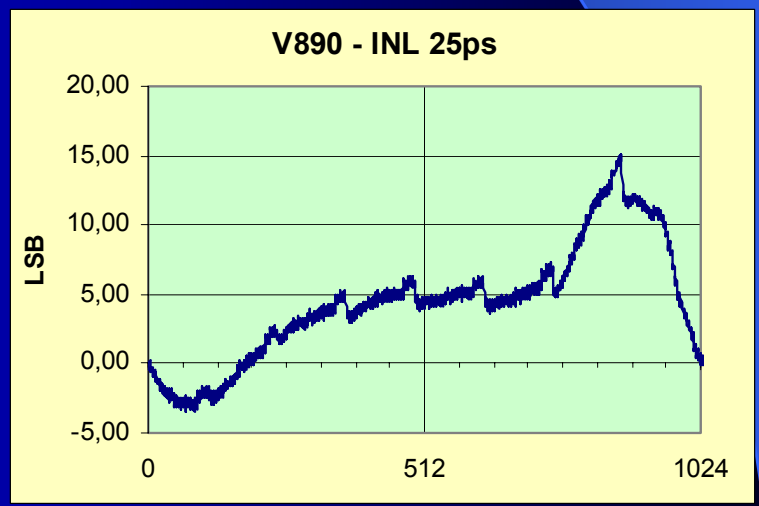


INL (not compensated)

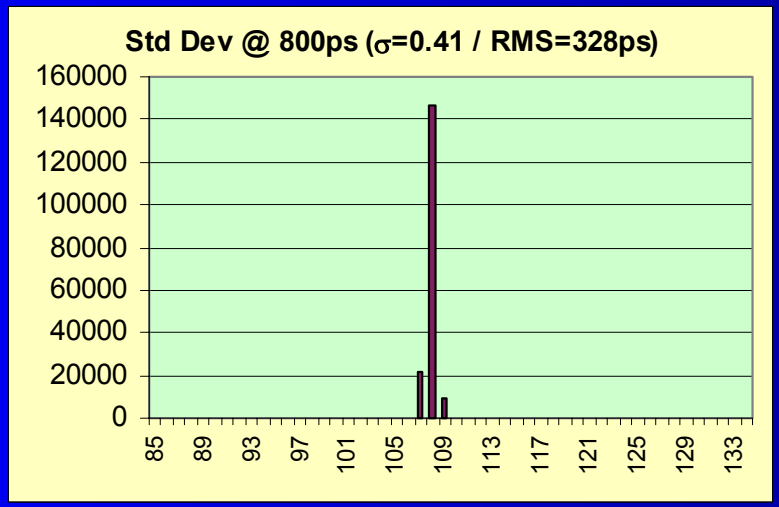


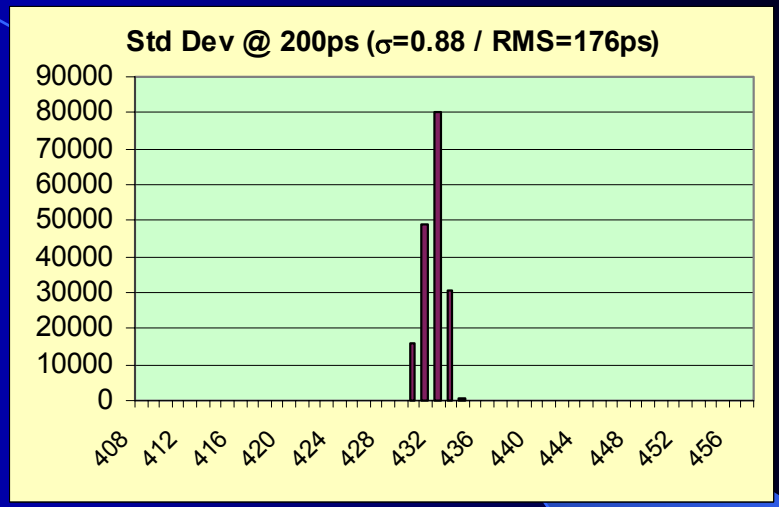


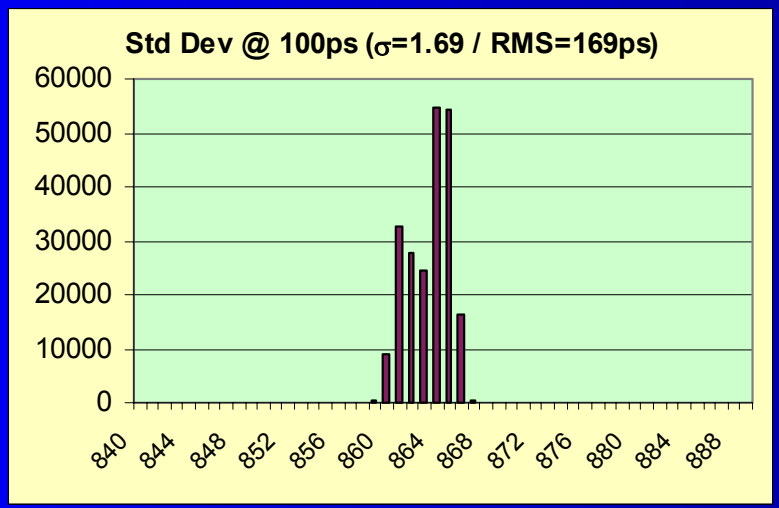


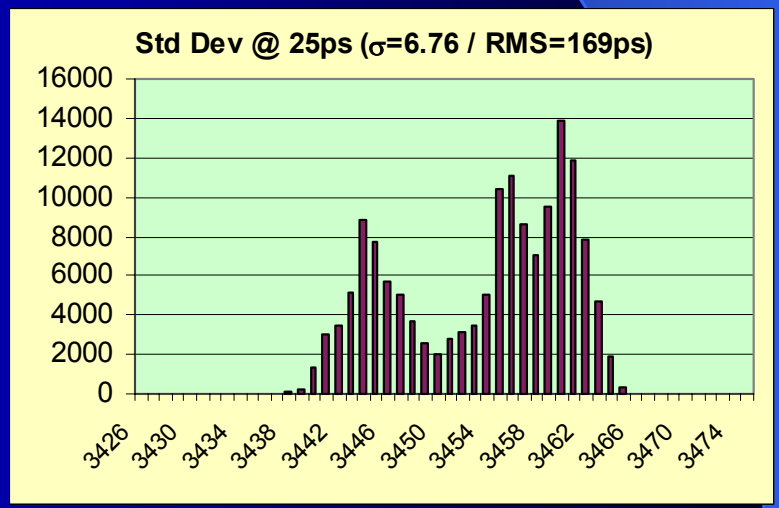


Std Dev (not compensated)

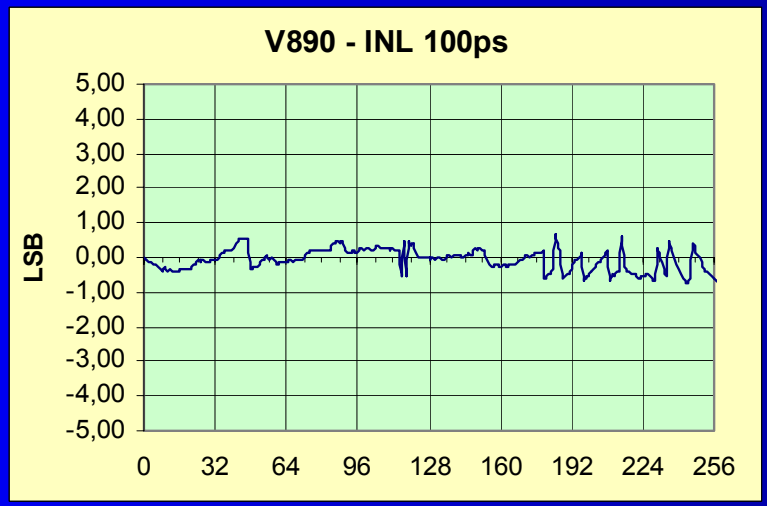


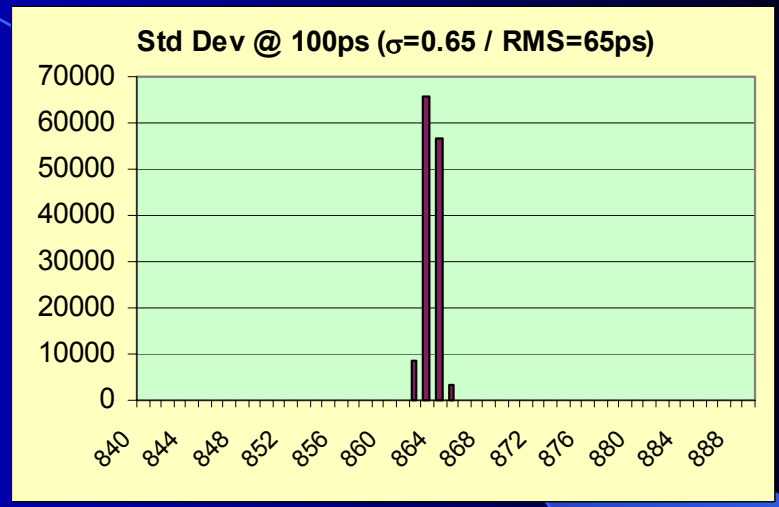


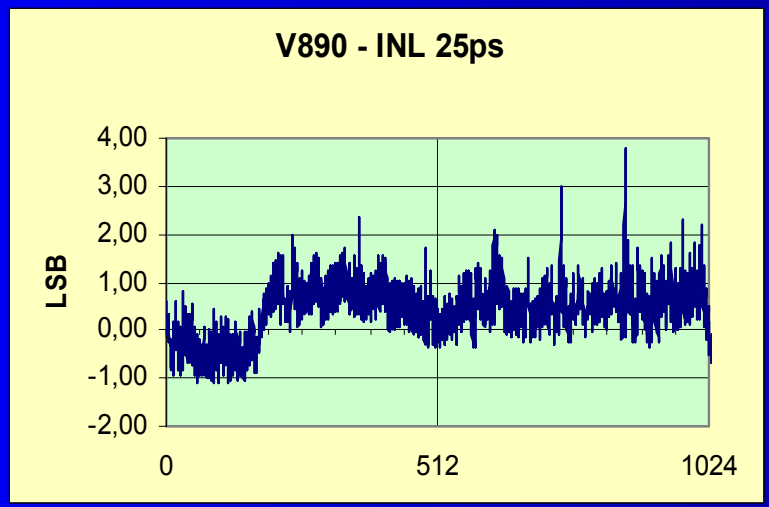


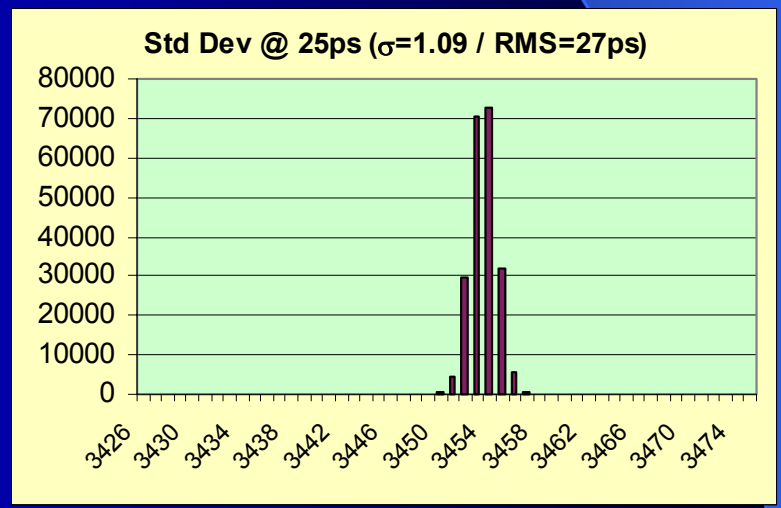


After Compensation









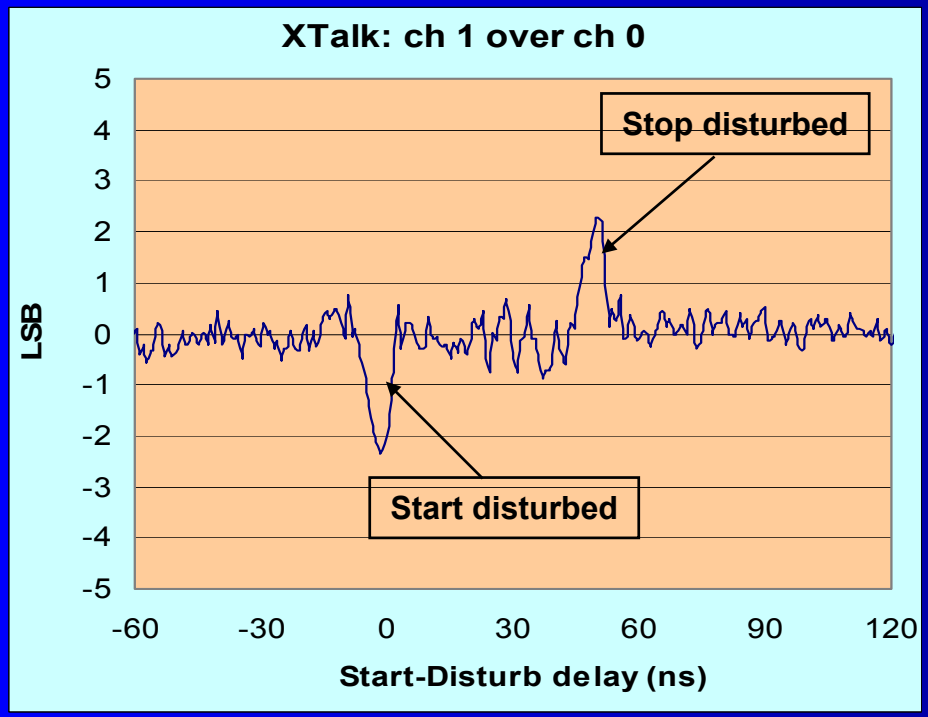
Summary

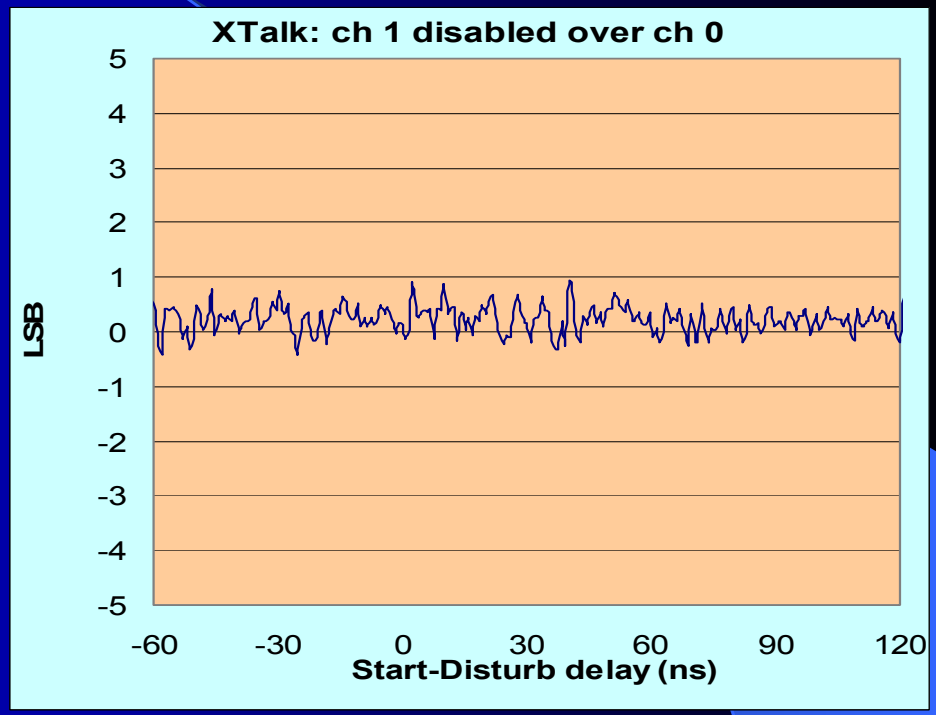
	DNL	INL	Sigma	RMS
800ps	0.1 LSB	0.3 LSB	0.41	328 ps
200ps	0.3 LSB	1.3 LSB	0.88	176 ps
100ps	0.8 LSB	3.6 LSB	1.69	169 ps
25ps	2.8 LSB	15 LSB	6.76	169 ps
100ps - LUT	-	0.8 LSB	0.65	65 ps
25ps - LUT	-	3.8 LSB	1.09	27 ps

Cross Talk (I)

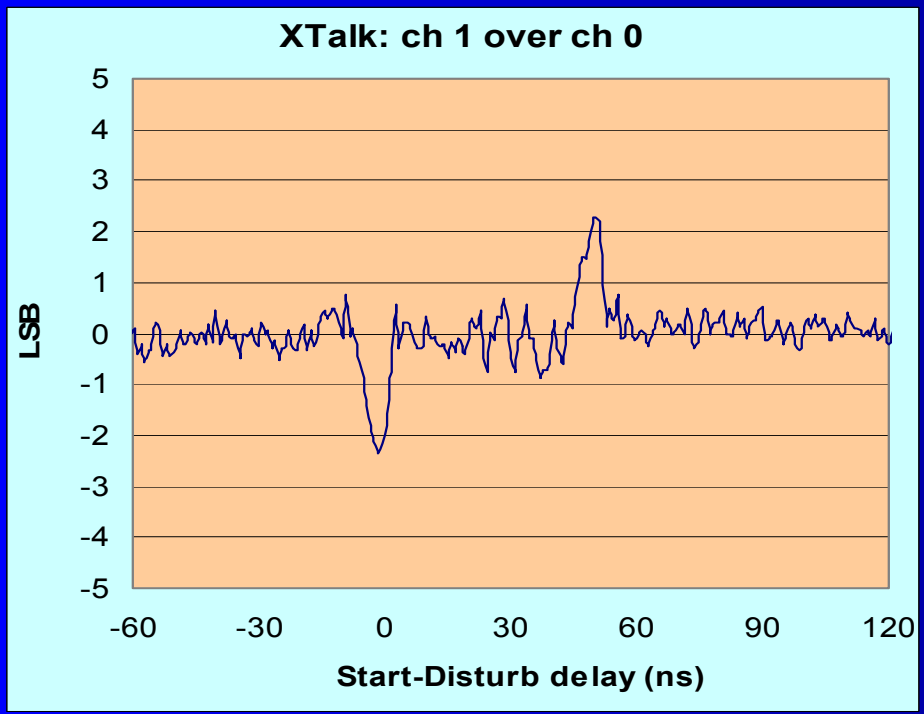
- Cross talk has been measured with HPTDC rev 1.3 programmed in very high resolution mode (25ps)
- There is a fixed start-stop measurement (~50ns) disturbed by a pulse with a sweeping delay respect to the start-stop
- Start is on channel 0 and stop on channel 7
- The disturb is connected to different channels of the same chip
- The measurement was also performed with the disturbing channel disabled: we didn't see any X-talk and this guarantees that the X-talk is not introduced by the external setup

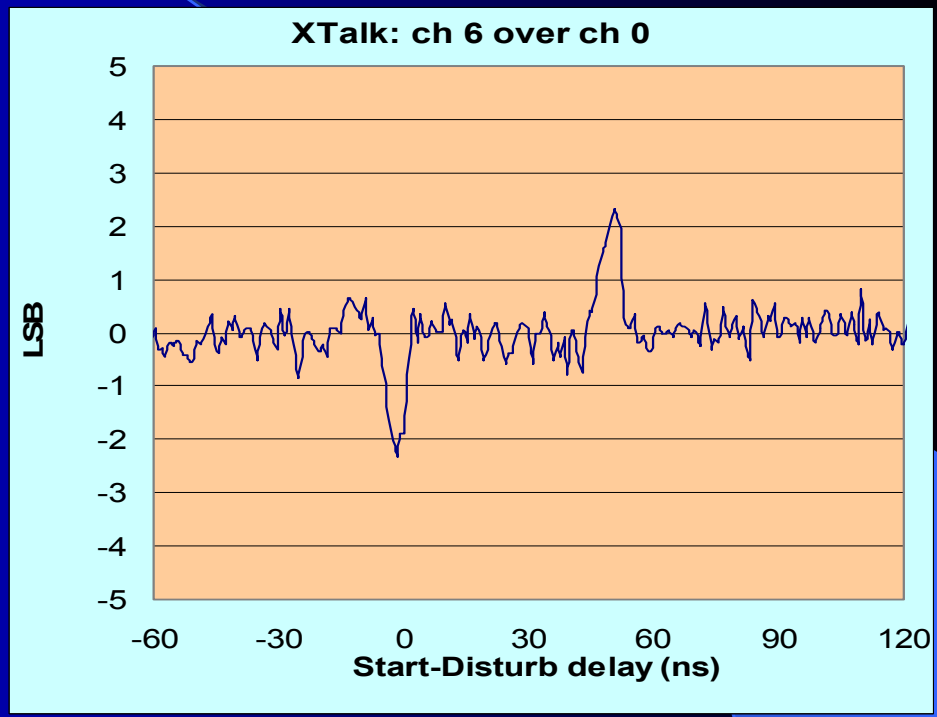
Cross Talk (II)



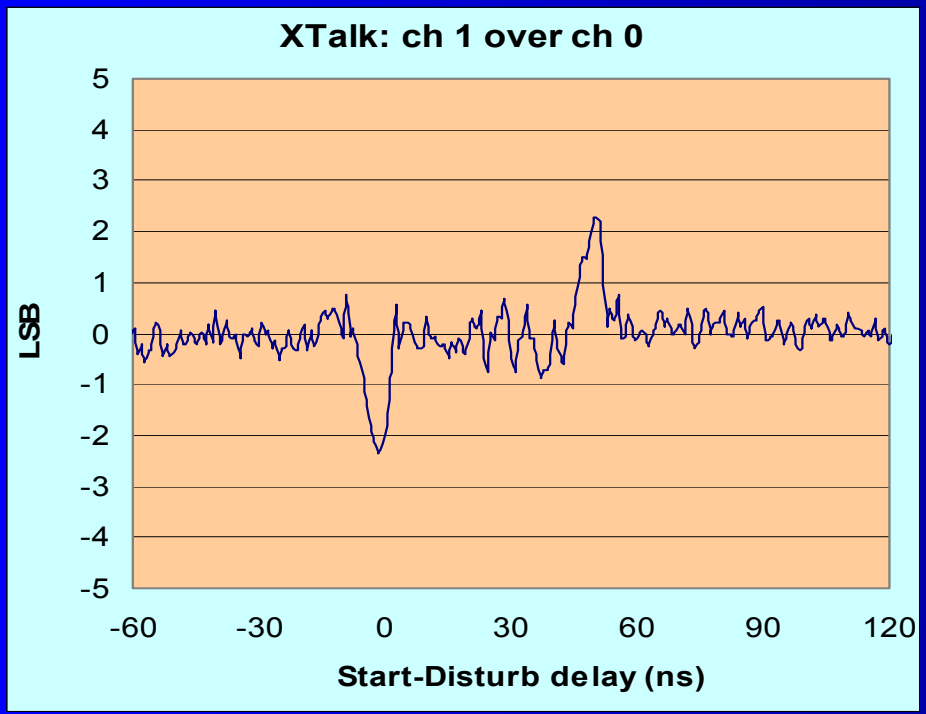


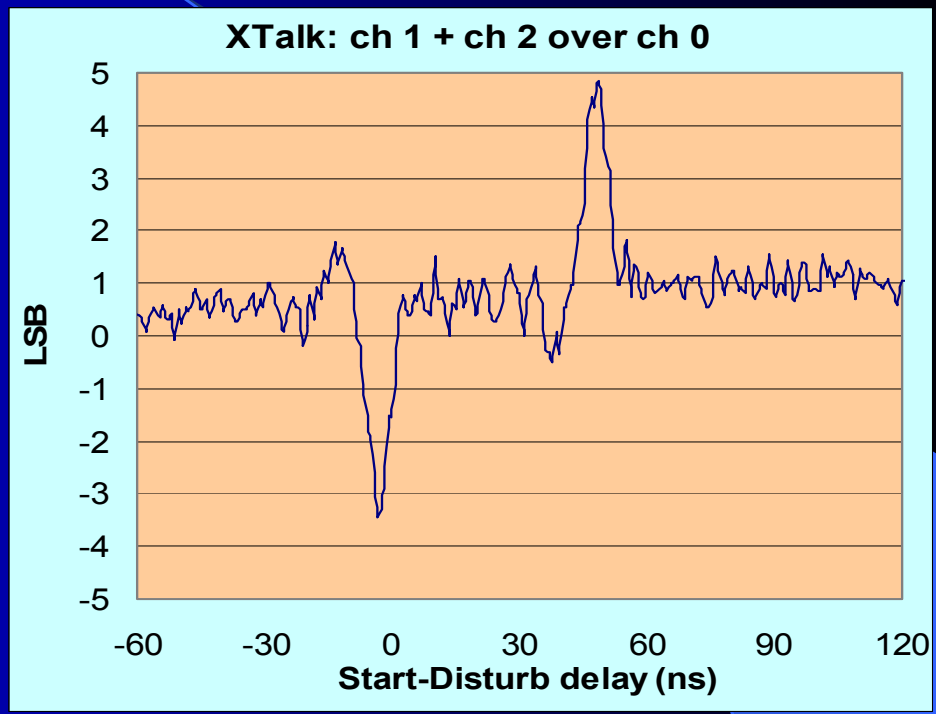
Cross Talk (III)





Cross Talk (IV)





New HPTDC Revision

- We did few linearity tests using the prototype V890 with the new revision of the HPTDC chip (1.3)
- The result obtained is still preliminary but it seems to be similar to the old one
- We are going to make more accurate tests using new board + new chips
- From the functional point of view, some bugs found in rev. 1.1 have been fixed
- We didn’t experience any memory error

Work Plan

IV Q 2001: the prototype V890 is ready

I&II Q 2002: debug of V890 and HPTDC rev. 1.1

III Q 2002: measurements and performances verify

IV Q 2002: design of the new family V1190-V1290 starts

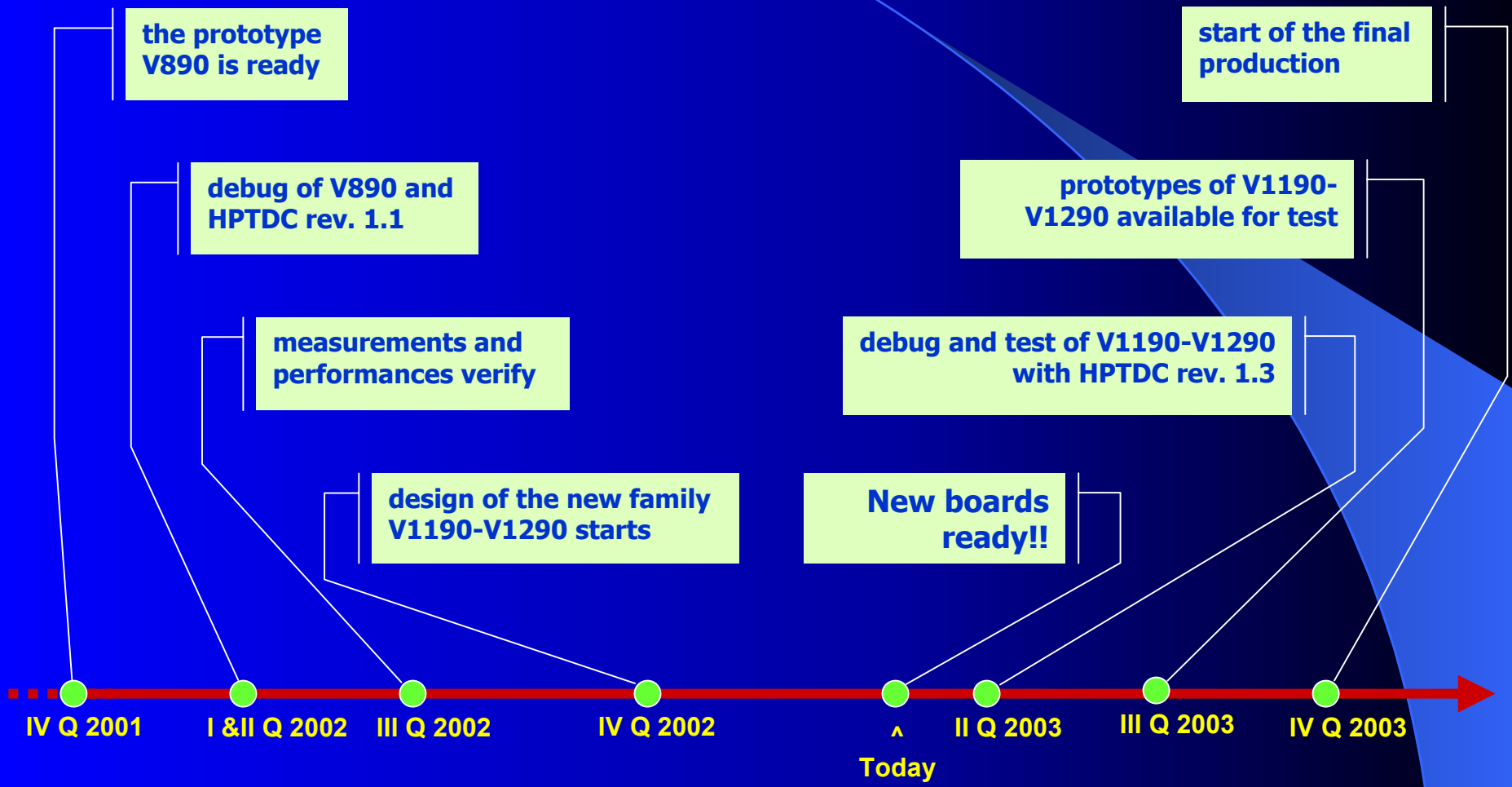
today: new boards ready

summer 2003: debug and test of V1190-V1290 with HPTDC rev. 1.3.

September 2003: prototypes of V1190-V1290 available for test

IV Q 2003: start of the final production

Milestones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start of the final production
debug of V890 and HPTDC rev. 1.1
prototypes of V1190-V1290 available for test
measurements and performances verify
debug and test of V1190-V1290 with HPTDC rev. 1.3
design of the new family V1190-V1290 starts
New boards ready!!
IV Q 2001
I &II Q 2002
III Q 2002
IV Q 2002
Today
II Q 2003
III Q 2003
IV Q 2003

Conclusions

- Comparing our results with those obtained at CERN and at INFN-Bologna we can confirm that the board does not worsen the performances of the HPTDC chip
- The linearity problems of the chip, still present in the latest revision, can be corrected at hardware level without dead-time
- One year of work for developing and verifying the previous prototype V890 makes us skilled in the use of the HPTDC chips in a VME board (clock distribution, power supply, interfacing…)