AMT-2 & 3 (ATLAS Muon TDC version 2 & 3)

Data Sheets

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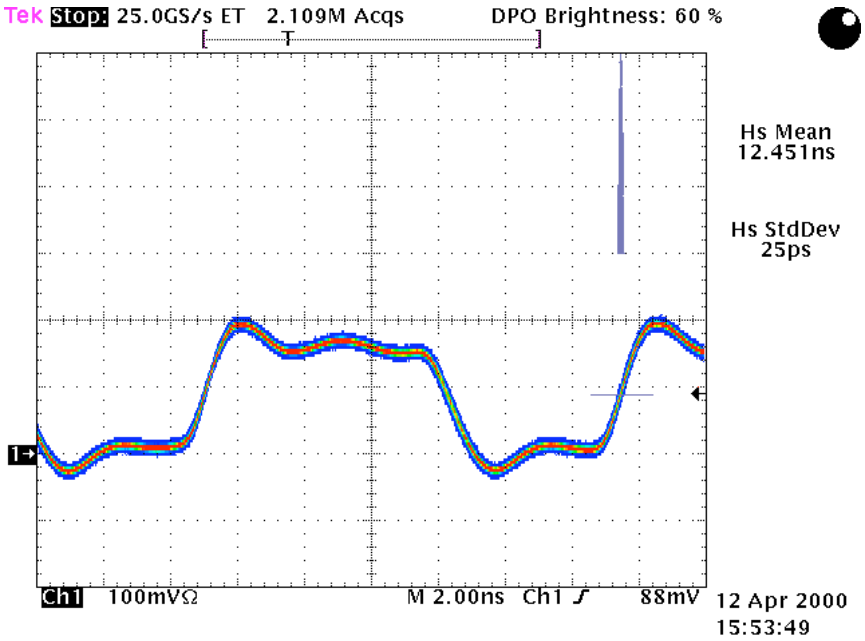


(Documents of Toshiba's LSI such as Reliability, Handling cautions and General guide, are available from http://doc.semicon.toshiba.co.jp/indexus.htm)

Contents

1. Signal, Package and Pin Assignment

1.1. Signal description

Table. 1. Signal description.

Name	I/O	Description
RESETB	I	Reset signal. (negative logic)
ASDMOD	I	ASD control mode
ENCCONTP / $\overline{\text{ENCCONTM}}$	LVI	Encoded Control Signal.
HITP0 - 23 / $\overline{\text{HITM0 - 23}}$	LVI	Hit inputs.
BUNCHRSTB	I	Bunch Count Reset signal. (negative logic)
CLKOEN	I	CLKO enable
EVENTRSTB	I	Event Count Reset signal. (negative logic)
CLKO	I	System clock output.
TRIGGER	I	Trigger signal.
CLKP / $\overline{\text{CLKM}}$	LVI	System clock input.
CDIO0 - 11	I, TO	CSR data lines and Parallel data output[11:0]
DIO12 - 23	TO	Parallel data output[23:12] / General Outputs
DIO24-27	I,TO	Parallel data output[27:24] /General Inputs
DIO28 - 31	TO	Parallel data output[31:28] / ASD Control Signals
DREADY	O	Data Ready signal.
ERRORB	OD	Error signal (negative logic)
CLKOUT	O	PLL Clock, Start and Carry output signal. Controlled by clkout_mode bits.
TEST0 - 1	I, PD	Test mode select inputs. TEST=0 : Normal Mode TEST=1 : Toshiba standard test mode, TEST=2 : IDDS test mode (disable all LVDS receivers), TEST=3 : Test clock mode (CLK signal is directly connected to internal clock line without PLL).
TDO	TO	JTAG TDO.
TMS	I, PU	JTAG TMS.
TDI	I, PU	JTAG TDI.
TCK	I	JTAG TCK. (Schmitt Trigger input buffer)
$\overline{\text{TRSTB}}$	I, PU	JTAG $\overline{\text{TRSTB}}$. (negative logic)
GETDATA	I	Get Data signal.
START	I	Start signal. Start coarse counter and enable channel inputs.
SERIOUTP / $\overline{\text{SERIOUTM}}$	LVO	Serial data output.
STROBEP / $\overline{\text{STROBEM}}$	LVO	Serial strobe output.
DSPACE	I	Data Space select signal. DSPACE = 1 : Parallel data, DSPACE = 0 : CSR space.
WR	I	CSR write signal.
CS	I	Chip Select signal.
RA0 - 4	I	CSR address signal
VGN	analog	PLL loop filter terminal. This pin should be connected to external capacitors of 6800 pF through 500 Ohm resister.

[I = CMOS Input, LVI = LVDS Input, O = CMOS Output, TO = Three State Output, LVO = LVDS Output, OD = Open drain output; PU = with internal pull-up resistor, PD = with internal pull-down resistor, $\overline{xxx}$ = negative logic]

* LVDS input has a internal 100 ohm termination resistor.

Table. 2 CDIO I/O Buffer Status ([TEST1,TEST0] != [0,1])

ASDMOD	CS	WR(1)	DSPACE(1)	CDIO0-11	CDIO12-23	CDIO24-27	CDIO28-31	Comment
L	L	X	X	HiZ	HiZ	HiZ	HiZ	Normal
	H	L	L	CSR Out	Out	Out	Out	CSR Read
	H	H	L	HiZ(CSR In)	HiZ	HiZ	HiZ	CSR Write
	H	X	H	Data Out	Data Out	Data Out	Data Out	Data Read
H	L	X	X	HiZ	Out	HiZ(In)	Out	Normal
	H	L	L	CSR Out	Out	HiZ(In)	Out	CSR Read
	H	H	L	HiZ(CSR In)	Out	HiZ(In)	Out	CSR Write
	H	X	H	[Data Out]	Out	HiZ(In)	Out	not use

(1) Signal level at CS up.

Table. 3 Dual Function Pins

	ASDMOD=0		ASDMOD=1	
Pin No.	Name	I/O	Name	I/O
88	DIO12	Out	OUT0	Out
89	DIO13	Out	OUT1	Out
91	DIO14	Out	OUT2	Out
92	DIO15	Out	OUT3	Out
93	DIO16	Out	OUT4	Out
94	DIO17	Out	OUT5	Out
95	DIO18	Out	OUT6	Out
96	DIO19	Out	OUT7	Out
97	DIO20	Out	OUT8	Out
99	DIO21	Out	OUT9	Out
100	DIO22	Out	OUT10	Out
101	DIO23	Out	OUT11	Out
102	DIO24	Out	IN0	In
103	DIO25	Out	IN1	In
104	DIO26	Out	IN2	In
105	DIO27	Out	ASDIN(IN3)	In
107	DIO28	Out	ASDLOAD	Out
108	DIO29	Out	ASDCLK	Out
109	DIO30	Out	ASDDOWN	Out
110	DIO31	Out	ASDOUT	Out

1.2. Pin Assignment

pin	Name	Buffer
1=	resetb,	IBUFN;
2=	asdmod,	IBUF;
3=	enccontm,	WLVDSINR1;
4=	enccontp,	WLVDSINR1;
5=	VDD;	
6=	VSS;	
7=	hitm[0],	WLVDSINR1;
8=	hitp[0],	WLVDSINR1;
9=	hitm[1],	WLVDSINR1;
10=	hitp[1],	WLVDSINR1;
11=	hitm[2],	WLVDSINR1;
12=	hitp[2],	WLVDSINR1;
13=	hitm[3],	WLVDSINR1;
14=	hitp[3],	WLVDSINR1;
15=	hitm[4],	WLVDSINR1;
16=	hitp[4],	WLVDSINR1;
17=	VSS;	
18=	VDD;	
19=	hitm[5],	WLVDSINR1;
20=	hitp[5],	WLVDSINR1;
21=	hitm[6],	WLVDSINR1;
22=	hitp[6],	WLVDSINR1;
23=	hitm[7],	WLVDSINR1;
24=	hitp[7],	WLVDSINR1;
25=	hitm[8],	WLVDSINR1;
26=	hitp[8],	WLVDSINR1;
27=	hitm[9],	WLVDSINR1;
28=	hitp[9],	WLVDSINR1;
29=	VDD;	
30=	VSS;	
31=	hitm[10],	WLVDSINR1;
32=	hitp[10],	WLVDSINR1;
33=	hitm[11],	WLVDSINR1;
34=	hitp[11],	WLVDSINR1;
35=	hitm[12],	WLVDSINR1;
36=	hitp[12],	WLVDSINR1;
37=	hitm[13],	WLVDSINR1;
38=	hitp[13],	WLVDSINR1;
39=	hitm[14],	WLVDSINR1;
40=	hitp[14],	WLVDSINR1;
41=	VDD;	
42=	hitm[15],	WLVDSINR1;
43=	hitp[15],	WLVDSINR1;
44=	VSS;	
45=	hitm[16],	WLVDSINR1;
46=	hitp[16],	WLVDSINR1;
47=	hitm[17],	WLVDSINR1;
48=	hitp[17],	WLVDSINR1;
49=	hitm[18],	WLVDSINR1;
50=	hitp[18],	WLVDSINR1;
51=	hitm[19],	WLVDSINR1;
52=	hitp[19],	WLVDSINR1;
53=	VDD;	
54=	VSS;	
55=	hitm[20],	WLVDSINR1;
56=	hitp[20],	WLVDSINR1;
57=	hitm[21],	WLVDSINR1;
58=	hitp[21],	WLVDSINR1;
59=	hitm[22],	WLVDSINR1;
60=	hitp[22],	WLVDSINR1;
61=	hitm[23],	WLVDSINR1;
62=	hitp[23],	WLVDSINR1;
63=	VDD;	
64=	VSS;	
65=	bunchrstb,	IBUFN;
66=	clkoen,	IBUFD;
67=	eventrstb,	IBUFN;
68=	clko,	BT8R;
69=	trigger,	IBUF;
70=	VSS;	
71=	clkm,	WLVDSINR1;
72=	clkp,	WLVDSINR1;

73=	VSS;	
74=	VDD;	
75=	cdio[0],	BD8RCD;
76=	cdio[1],	BD8RCD;
77=	cdio[2],	BD8RCD;
78=	cdio[3],	BD8RCD;
79=	cdio[4],	BD8RCD;
80=	cdio[5],	BD8RCD;
81=	cdio[6],	BD8RCD;
82=	VSS;	
83=	cdio[7],	BD8RCD;
84=	cdio[8],	BD8RCD;
85=	cdio[9],	BD8RCD;
86=	cdio[10],	BD8RCD;
87=	cdio[11],	BD8RCD;
88=	do12_23[0],	BT8R;
89=	do12_23[1],	BT8R;
90=	VDD;	
91=	do12_23[2],	BT8R;
92=	do12_23[3],	BT8R;
93=	do12_23[4],	BT8R;
94=	do12_23[5],	BT8R;
95=	do12_23[6],	BT8R;
96=	do12_23[7],	BT8R;
97=	do12_23[8],	BT8R;
98=	VSS;	
99=	do12_23[9],	BT8R;
100=	do12_23[10],	BT8R;
101=	do12_23[11],	BT8R;
102=	dio24_27[0],	BD8RCD;
103=	dio24_27[1],	BD8RCD;
104=	dio24_27[2],	BD8RCD;
105=	dio24_27[3],	BD8RCD;
106=	VDD;	
107=	do28_31[0],	BT8R;
108=	do28_31[1],	BT8R;

109=	do28_31[2],	BT8R;
110=	do28_31[3],	BT8R;
111=	dready,	B4R;
112=	errorb,	BT4ODFS;
113=	clkout,	B8R;
114=	test0,	IBUFD;
115=	tdo,	BT8R;
116=	VSS;	
117=	VDD;	
118=	tms,	IBUFU;
119=	tdi,	IBUFU;
120=	tck,	SMTC;
121=	trstb,	IBUFU;
122=	getdata,	IBUF;
123=	start,	IBUF;
124=	VSS;	
125=	serioutp,	WLVDSOUT;
126=	serioutm,	WLVDSOUT;
127=	strobep,	WLVDSOUT;
128=	strobem	WLVDSOUT;
129=	VDD;	
130=	test1,	IBUFD;
131=	dspace,	IBUF;
132=	wr,	IBUF;
133=	cs,	IBUF;
134=	ra[0],	IBUF;
135=	ra[1],	IBUF;
136=	VSS;	
137=	ra[2],	IBUF;
138=	ra[3],	IBUF;
139=	ra[4],	IBUF;
140=	VDD;	
141=	VSS;	
142=	vgn,	WDOUT;
143=	vgn return (VSS)	
144=	VDD;	

1.3.Package

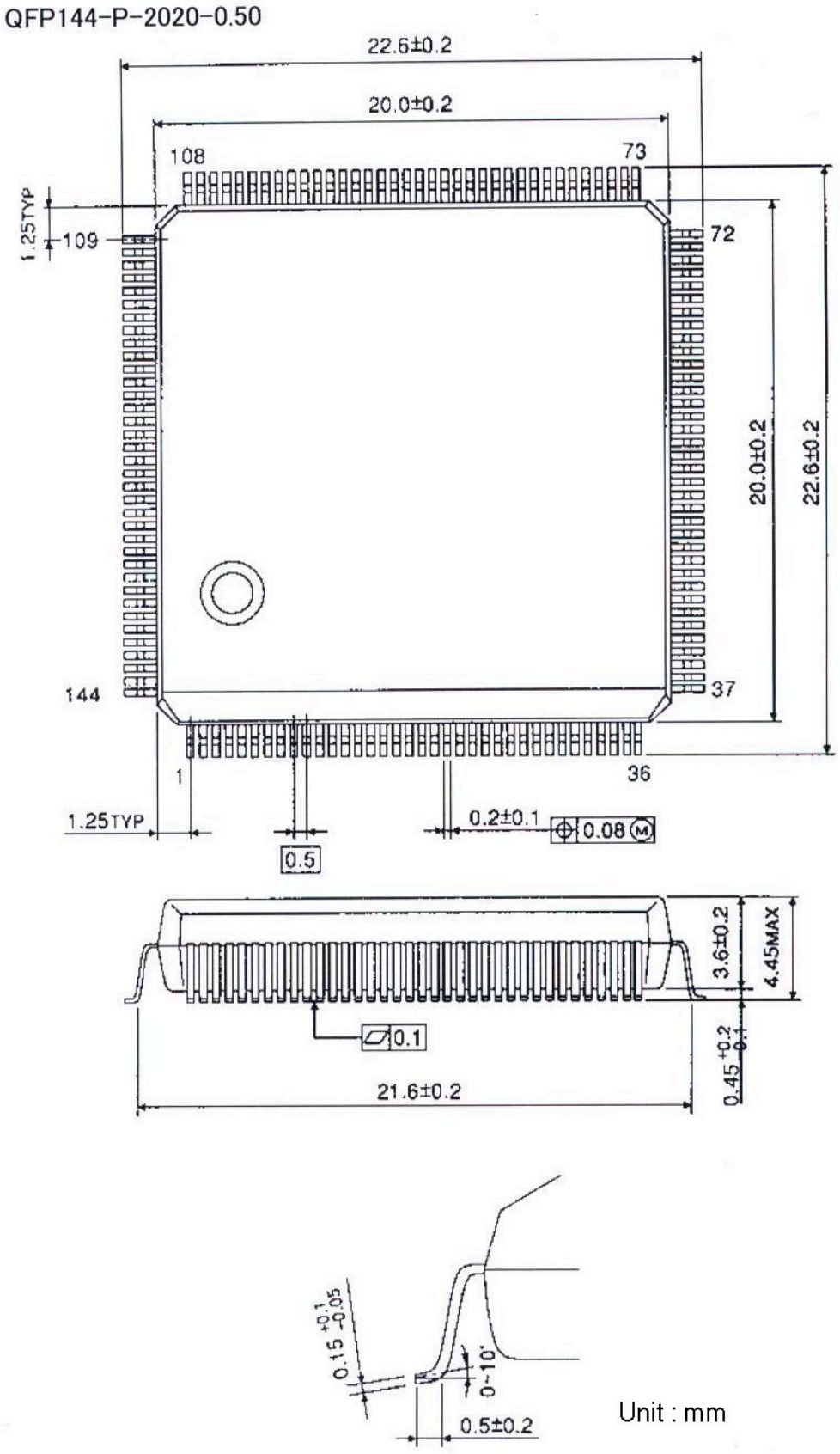


Fig. 1 QFP144 : 144-pin Plastic Flat Package

2.Electrical Characteristics

Pin 142 (VGN) is a PLL filter pin, and it must be connected to external resistor and a capacitor as shown in Fig. 2.

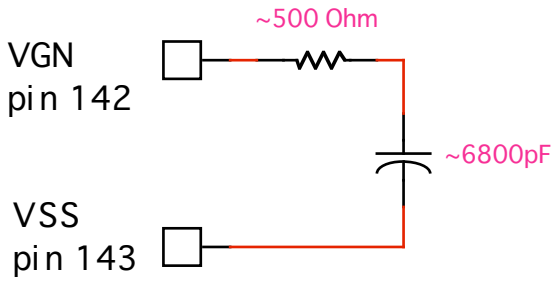


Fig. 2 VGN pin connection.

2.1.Maximum Ratings

Symbol	Parameter	Value
VDD	DC Supply Voltage	-0.3 to +5.0 V
VIN	Input Voltage	-0.3 to VDD+0.3 V
VOUT	Output Voltage	-0.3 to VDD+0.3 V
IIN	Input Current	±10 mA
T_{STG}	Storage Temperature	-40 to +125 °C

2.2. Recommended Operating Condition

(VSS = 0V)

Symbol	Parameter	Value
VDD(*)	DC Supply Voltage	3.3 ± 0.3 V
VIN	Input Voltage	VDD
Ta	Ambient Temperature	0 to +70 °C

(*) low noise/ripple is desirable for stable PLL operation.

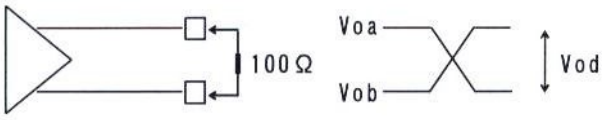
2.3.DC Characteristics

Symbol	Parameter	Condition	Min.	Typ	Max.	Unit
V_{IH}	Input High Voltage		V_{DD} x 0.8			
V_{IL}	Input Low Voltage				V_{DD} x 0.2	
I_{IH}	Input High Current	$V_{IN} = V_{DD}$	-10		10	µA
	(with pull down resistor)		-10		200	µA
I_{IL}	Input Low Current	$V_{IN} = V_{SS}$	-10		10	µA
	(with pull up resistor)		-200		10	µA
V_{OH}	High-level output voltage	I_{OH} = -4mA (B4: DREADY, ERRORB)	2.4			V
		I_{OH} = -8mA (B8: other output)	2.4			V
V_{OL}	Low-level output voltage	I_{OH}=4mA (B4: DREADY, ERRORB)			0.4	V
		I_{OH} = 8mA (B8:other output)			0.4	V
VH	Hysterisis of Schmidt Trigger Input	pin 120 tck		0.5		V
I_{OZ}	3-state output leakage current	$V_{OUT} = V_{DD}$ or V_{SS}	-10		10	µA
I_{DDS}	Quiescent device current(*)	$V_{IN} = V_{DD}$ or V_{SS} (TEST0 = 0, TEST1 = 1)			400	µA

LVDS Output (WLVDSOUT)

Symbol	Parameter	Min	Max	Unit	LVDS Spec(*) Min	LVDS Spec(*) Max
fmax	Output Frequency		100	MHz		
V_{oh}	Output voltage high		1550	mV		1475
V_{ol}	Output voltage low	800		mV	925	
V_{od}	Differential output voltage	200	400	mV	250	400
I_{oh}	V_{oh}=1.4V	1.5		mA		
I_{ol}	V_{ol}=1.4V	5		mA		

(*) The LVDS driver specifications of this chip are not compatible with the IEEE Std 1596.3-1996 LVDS standard.



LVDS Input (WLVDSINR1)

Symbol	Parameter	min	max	unit
fmax	Input Frequency		100	MHz
Tw	Input pulse width	5		ns
Vi	Input voltage range	0	2400	mV
|Vid|	Input differential	100		mV
Vicm	Input common mode levels	50	1700	mV
	(Vid >= 200 mV)	50	2000	mV
Ri	Internal Termination Resistor	80	120	Ω

(*) LVDS receiver contains an internal termination resistor Ri.
There is no internal pull-up resistor, so voltage of the pin becomes undefined when it is open. Therefore **unused LVDS input pins (both xxxP and xxxM) should be connected to VDD or pull-up to VDD through a resistor (~10kohm)** to reduce power consumption and to avoid instability of LVDS receiver.

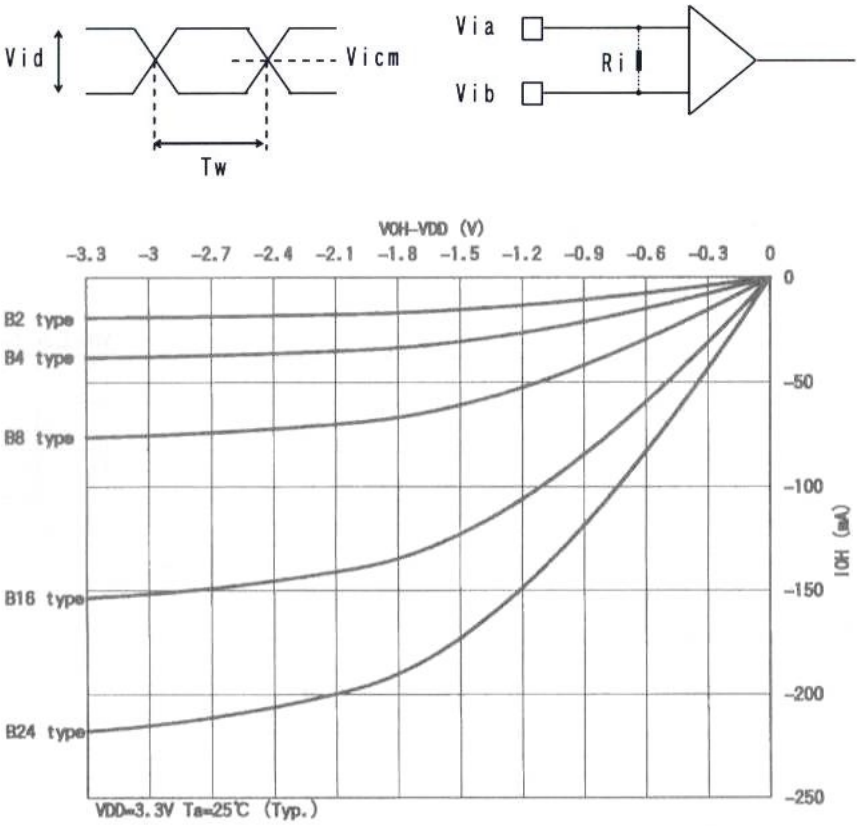


Fig. 3. Output Buffer VOH-IOH characteristics.

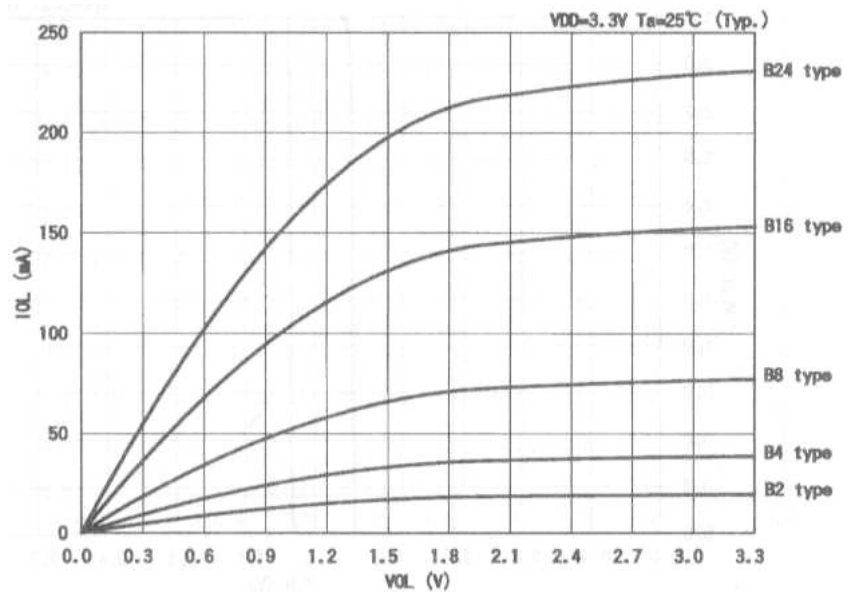


Fig. 4. Output Buffer VOL-IOL characteristics.

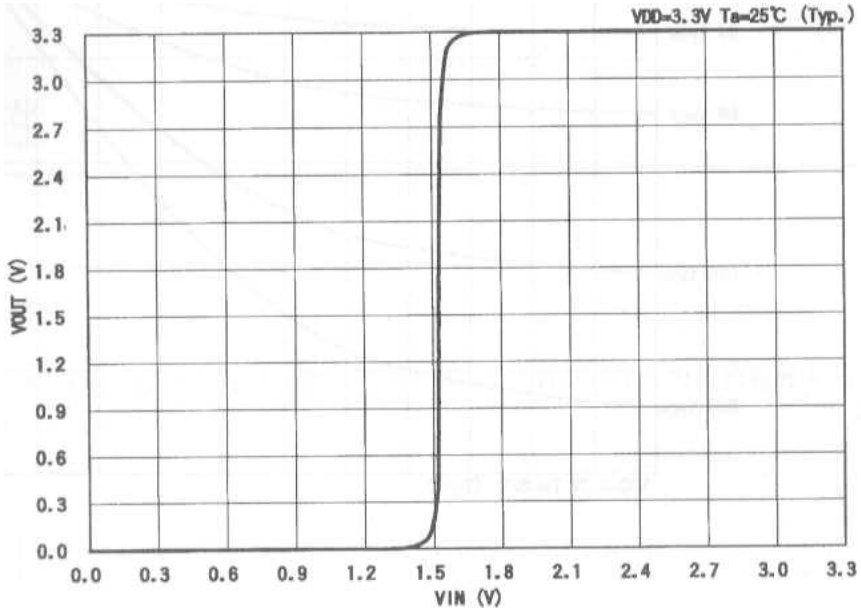


Fig. 5. CMOS Input Buffer (IBUF) characteristic.

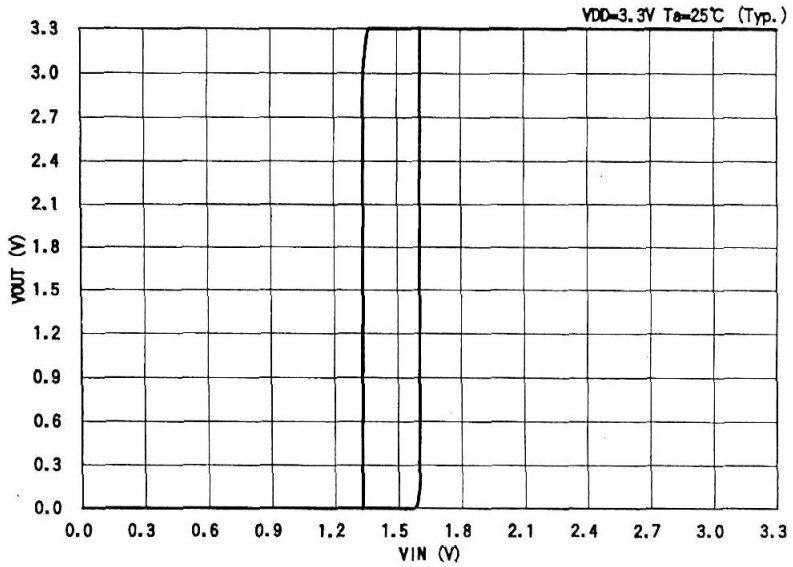


Fig. 6Schmitt Trigger Input Buffer (SMTC) characteristic.

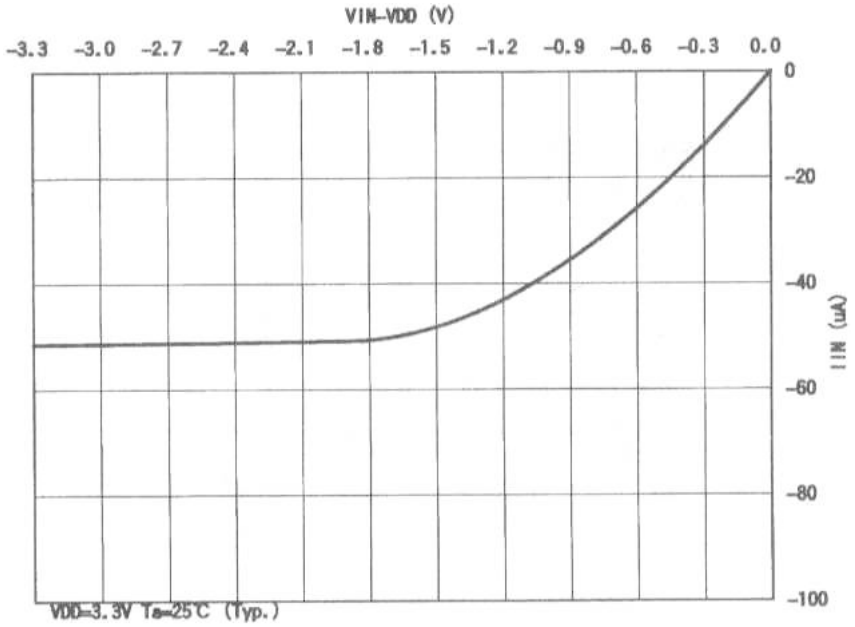


Fig. 7. Characteristic of Input buffer with Pull Up resistor (IBUFU).

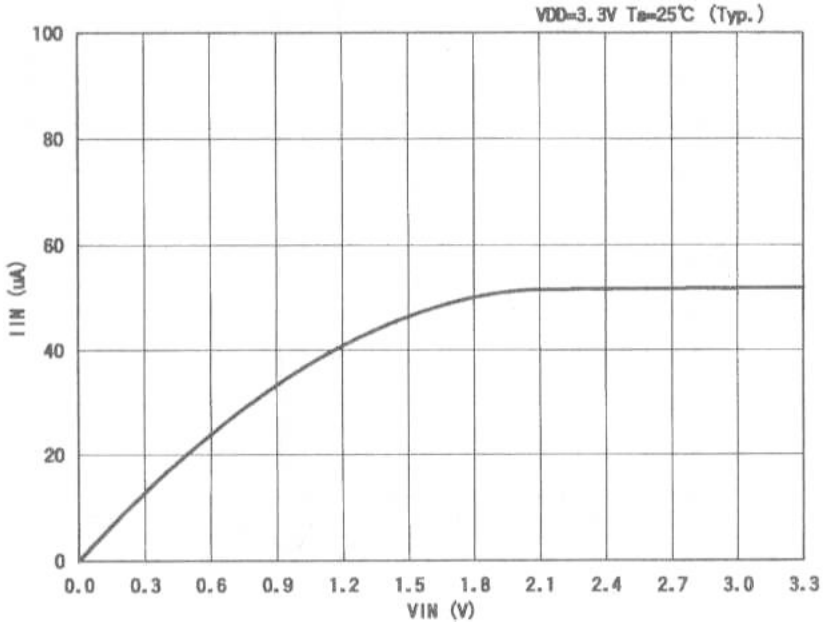


Fig. 8. Characteristic of Input Buffer with Pull Down resistor (IBUFD).

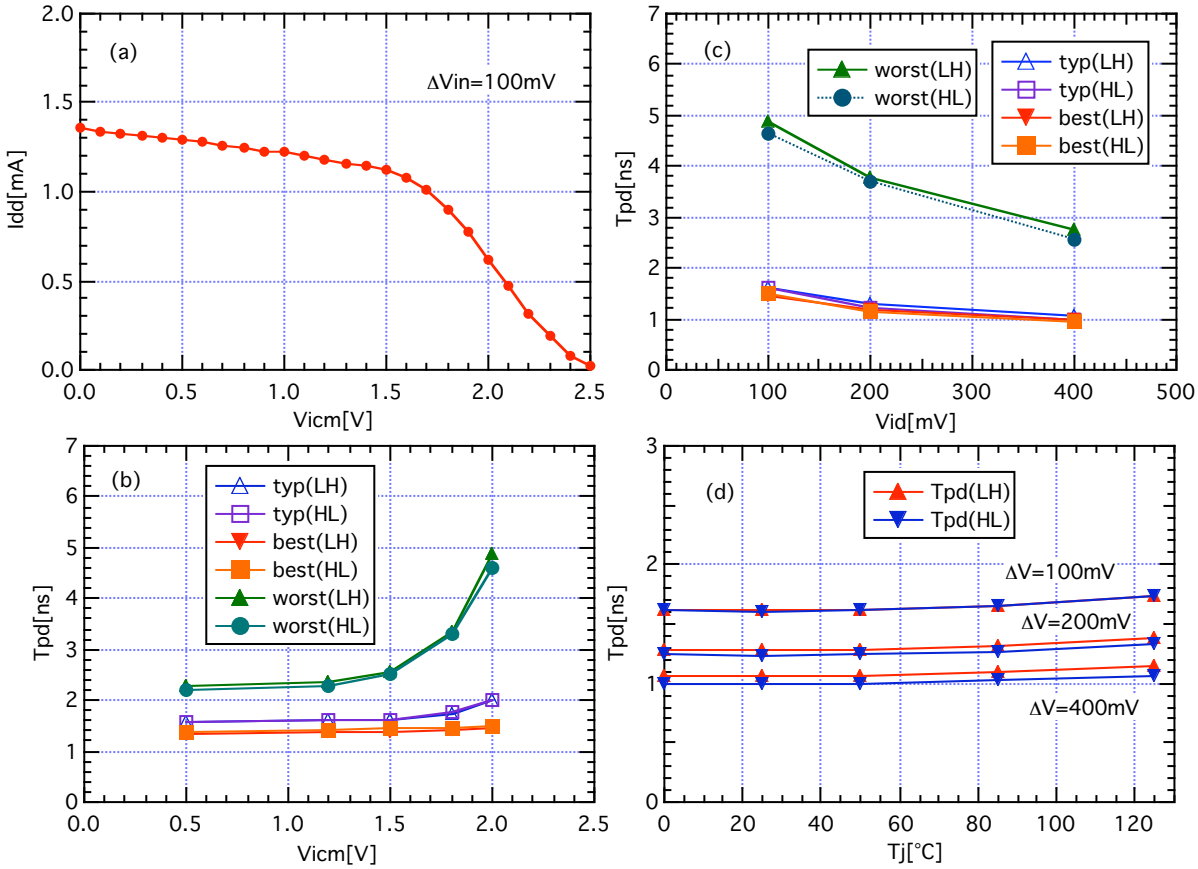


Fig. 9. LVDS receiver characteristics. (a) Static current (Idd) vs. input common mode voltage (Vicm), (b) Propagation delay (Tpd) vs. Vicm, (c) Tpd vs. input differential voltage (Vid), (d) Tpd vs. junction temperature (Tj).
[Typical condition --- 25 C, 3.3V, Best Condition --- 0 C, 3.6V, Worst Condition --- 85 C, 3.0V]

2.4.AC Characteristics

(VDD = 3.3 V, Ta = 25 °C, C_L = 30pF)

2.4.1.Clock Signal Characteristics

A simplified block diagram of clock signals is shown inFig. 10.External clock signals (CLKP and CLKN) are fed into PLL circuit. The PLL circuit generate multiplied frequency clock (x1 ~x8) CLK80. Nominal frequency of the CLK80 is 80 MHz. The CLK80 signal is used at front-end circuits of the time measurement. Most of the internal circuit uses 40 MHz clock (CLK40) which is created by dividing the CLK80 signal. Since I/O interfaces use the CLK40 signal as systemclock, it is natural to define timing relative to the CLK40.

However we can not see CLK40 timing directly, so here we define signal timings relative to the CLKOUT signal with clkout_mode=1. This CLKOUT signal represents the CLK40 signal delayed by buffers. It is important to know that the CLKOUT timings are measured with 30pF load. If the load is different, the timings will also change.

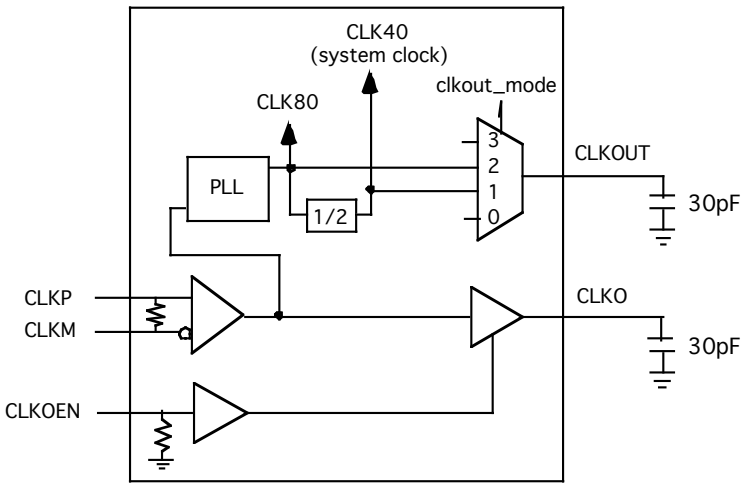


Fig. 10. Clock In/Out circuit.

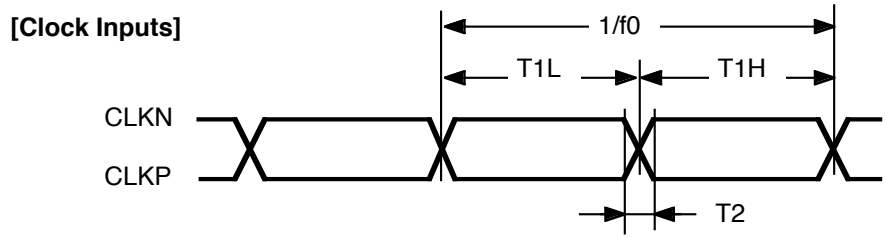


Fig. 11 Clock inputs signal characteristics.

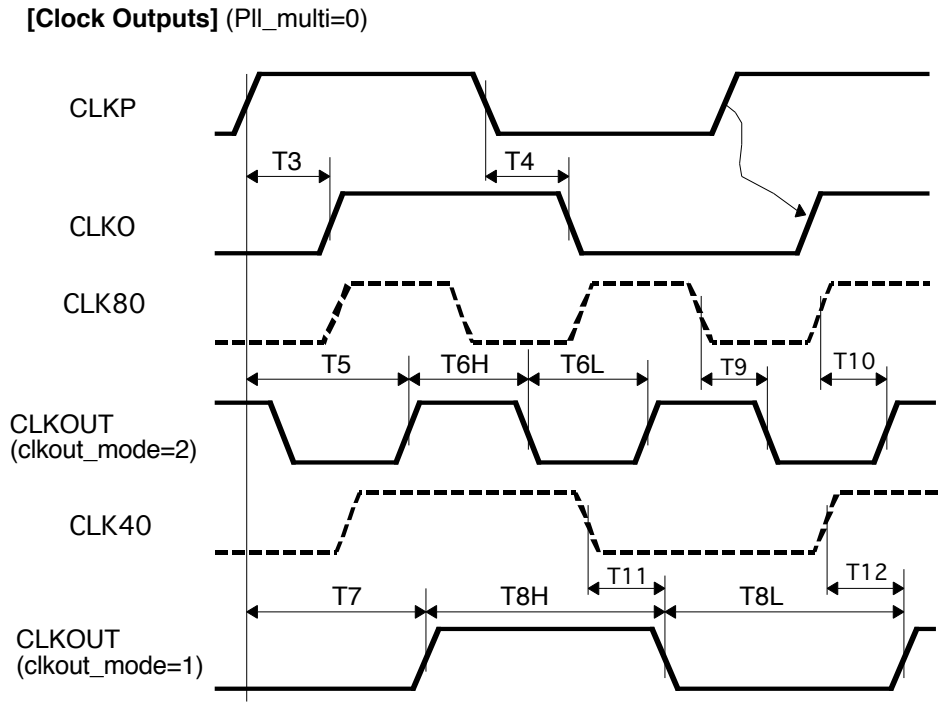


Fig. 12 Various clock timings. CLK40 and CLK80 are internal clock signals. Frequency of the CLK80 is 'pll_multi' x 'CLKP frequency'. Frequency of the CLK40 is half of the CLK80 frequency.

Table. 4

Symbol	Characteristics	Condition	Min	Typ	Max	Unit
f0	CLK frequency		10	40	60	MHz
T1L/T1H	CLK duty factor		0.8	1	1.25	
T3	CLKP Hi to CLKO Hi time	clkoen=1	6	7	8	ns
T4	CLKP Lo to CLKO Lo time	clkoen=1	6	7	8	ns
T5	CLKP Hi to CLKOUT Hi time	clkout_mode=2 pll_multi=0,1,3	11	12	13	ns
T6L/T6H	CLKOUT duty factor	clkout_mode=2	0.88	0.95	1.02	
T7	CLKP Hi to CLKOUT Hi time	clkout_mode=1	11	13	16	ns
T8L/T8H	CLKOUT duty factor	clkout_mode=1	0.81	0.88	0.95	
T9	CLK80 Lo to CLKOUT Lo time	clkout_mode=2		7.0		
T10	CLK80 Hi to CLKOUT Hi time	clkout_mode=2		7.9		
T11	CLK40 Lo to CLKOUT Lo time	clkout_mode=1		8.7		
T12	CLK40 Hi to CLKOUT Hi time	clkout_mode=1		9.1		

The generated clocks by the PLL has some jitter and shown in Fig. 13. Nominal value of the jitter is around 150 ps. However the jitter is affected by other activities. Fig. 14 shows the jitter dependence on trigger and hit rates.

Fig. 15 shows a result of time resolution measurement. Hit signal is delayed in 100 ps step from 1us to 13us to a clock synchronized start pulse. Timing resolution of 254 ps RMS is obtained.

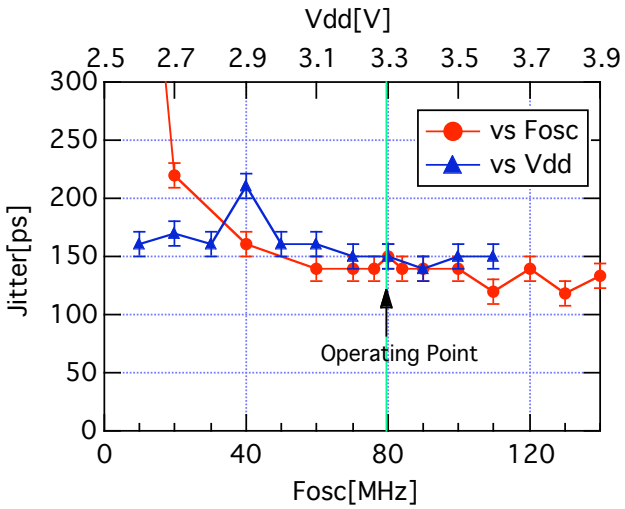


Fig. 13. PLL jitter vs. Oscillating frequency(Fosc) and supply voltage(Vdd) PLL mode is 1:2, so the input frequency is half of the Fosc. (No hit and no trigger signals).

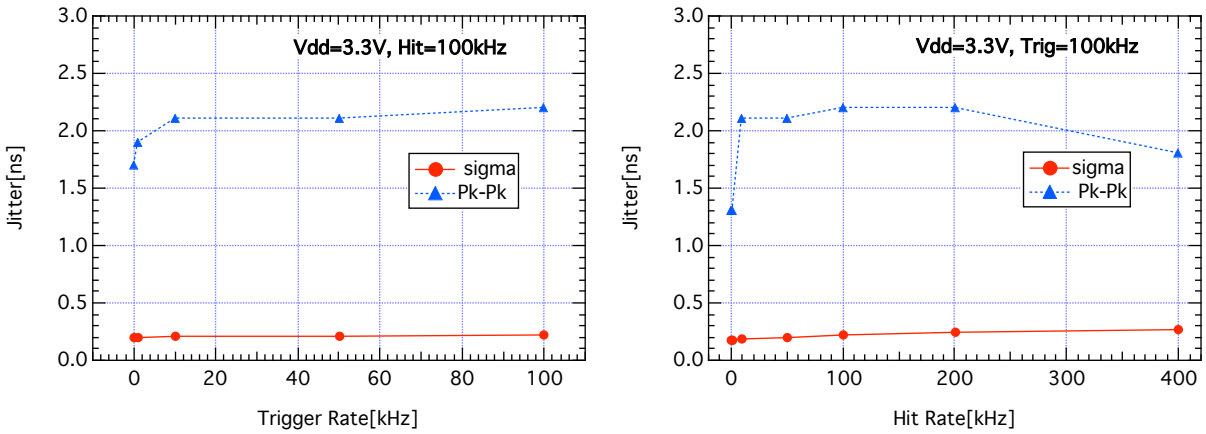


Fig. 14. Trigger rate and Hit rate dependence of the jitter.

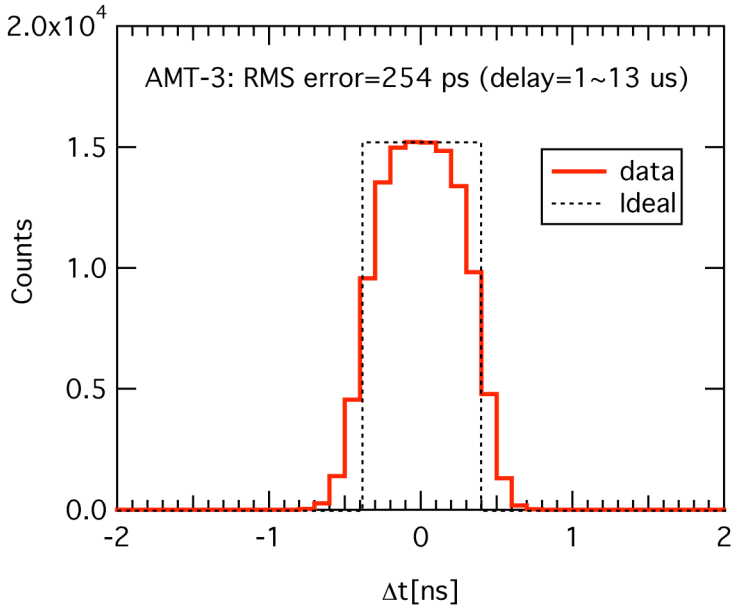
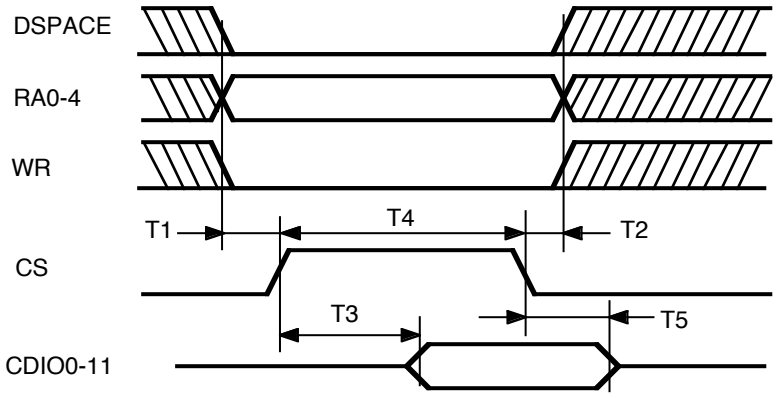


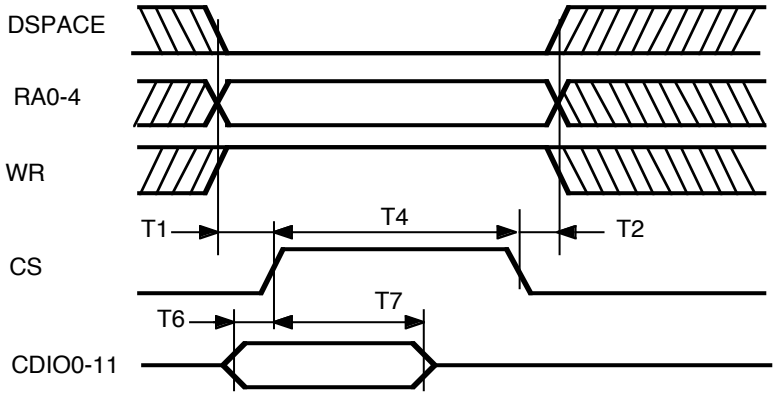
Fig. 15 Timing resolution of hit measurement for delay 1~13 us.

2.4.2.CSR Access Timing

[CSR Read Cycle Timing Diagram]



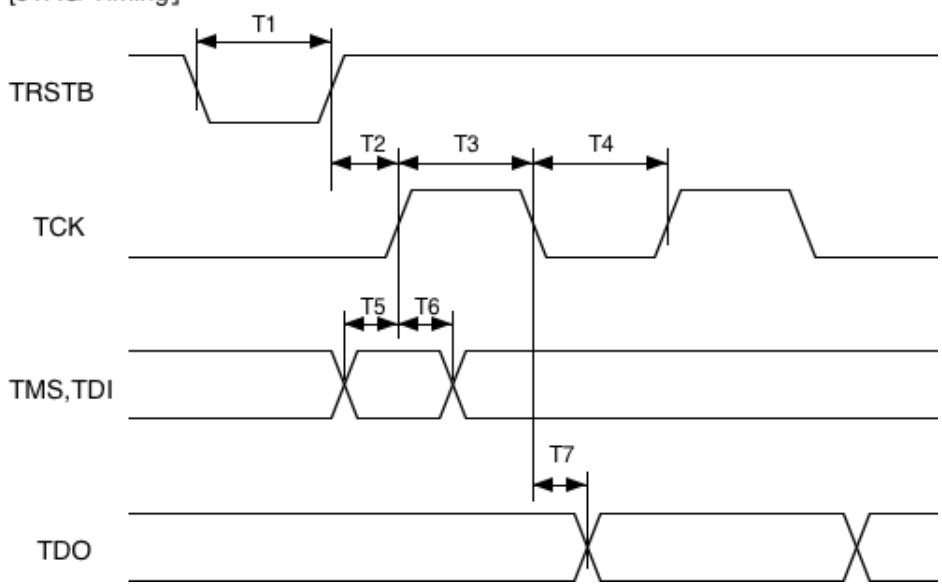
[CSR Write Cycle Timing Diagram]



Symbol	Characteristics	Min	Max	Unit
T1	RAx, WR setup time	1		ns
T2	CS negate to RAx, WR negate time	2		ns
T3	CS asserted to CDIOx asserted		18	ns
T4	CS pulse wiidth	8		ns
T5	CS negated to CDIOx negated		13	ns
T6	CDIO0-11 setup time	-1		ns
T7	CDIO0-11 hold time	9		ns

2.4.3.JTAG Signal Timings

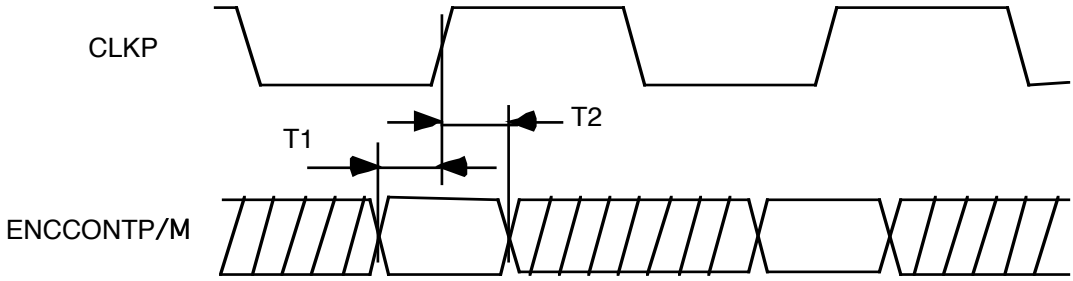
[JTAG Timing]



Symbol	Characteristics	Min	Max	Unit
T1	TRSTB width	4		ns
T2	TRSTB negate to TCK assert	3		ns
T3	TCK high width	6		ns
T4	TCK low width	6		ns
T5	TMS,TDI setup time	2		ns
T6	TMS,TDI hold time	2		ns
T7	TDO delay		8	ns

2.4.4.Encoded Control Signal Timing

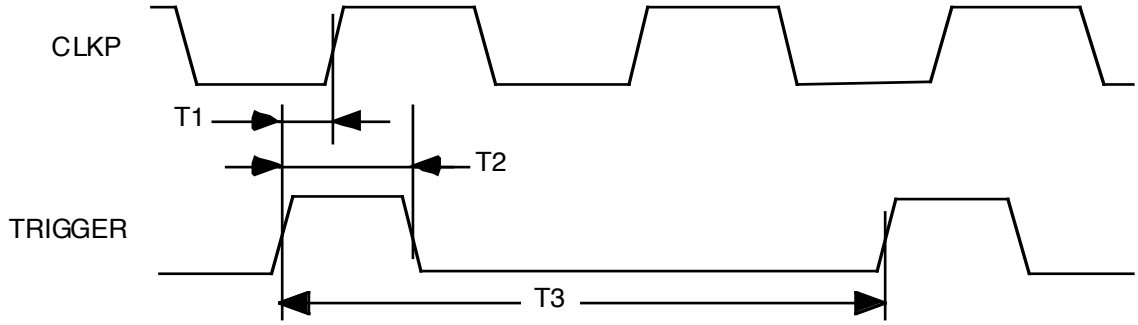
[Encoded Control Signal Timing]



Symbol	Characteristics	Condition	Min	Max	Unit
T1	CLKP Hi to ENCCONTP/M setup time		2	-	ns
T2	CLKP Hi to ENCCONTP/M hold time		5	-	ns

2.4.5.Trigger Signal Timing

[Triggerl Signal Timing (direct input, csr0[5]=1)]

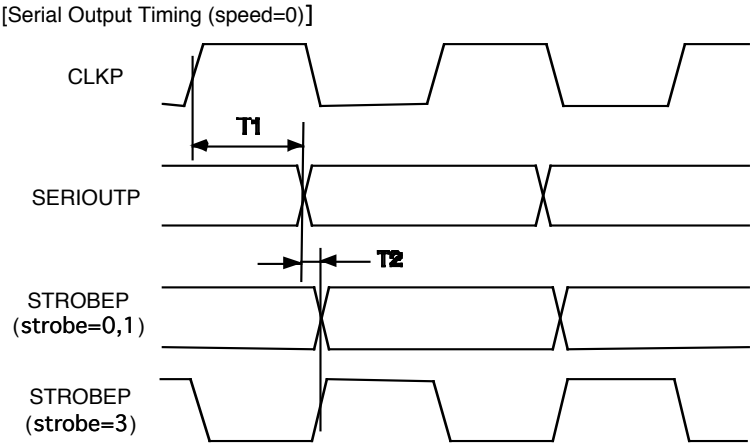


Symbol	Characteristics	Condition	Min	Max	Unit
T1	CLKP Hi to Trigger setup time		-3	CLK40 cycle - 4	ns
T2	Trigger signal width		CLK40 cycle	2 x (CLK40 cycle)	
T3	Trigger signal minimum separation		2 x (CLK40 cycle)	-	

(*) 'CLK40 cycle' nominal value is 25 ns.

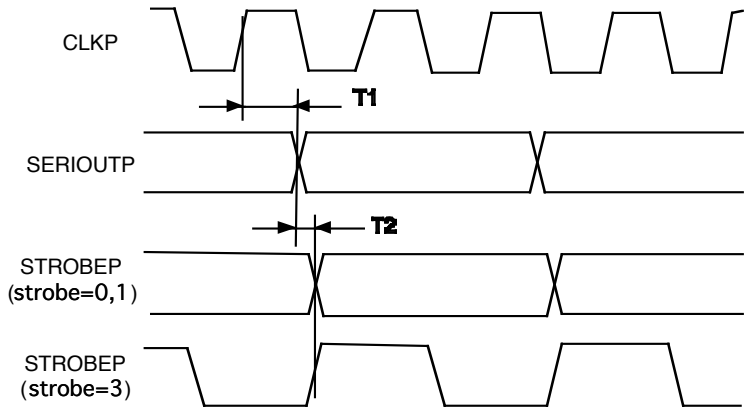
2.4.6.Serial Output Timing

[Serial Output Timing (speed=0)]



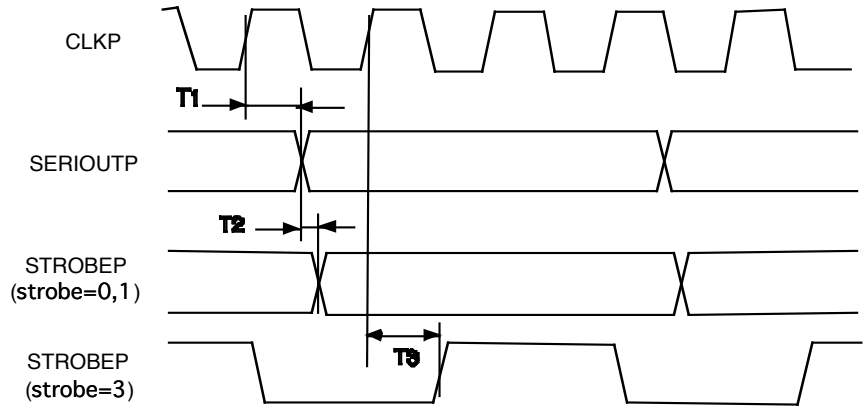
Symbol	Characteristics	Condition	Min	Typ	Max	Unit
T1	CLKP Hi to SERIOUTP change timing	readout_speed=0(40Mbps)	9	11	13	ns
T2	SERIOUT-STROBE timing	readout_speed=0(40Mbps) strobe_select=0,1,3	1	2	3	ns

[Serial Output Timing (readout_speed=1)]



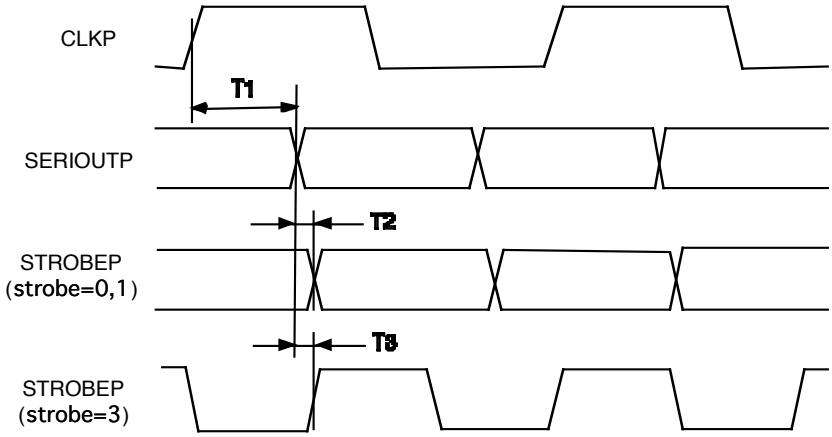
Symbol	Characteristics	Condition	Min	Typ	Max	Unit
T1	CLKP Hi to SERIOUTP change timing	readout_speed=1(20Mbps)	9	11	13	ns
T2	SERIOUT-STROBE timing	readout_speed=1(20Mbps) strobe_select=0,1,3	1	2	3	ns

[Serial Output Timing (readout_speed=2)]



Symbol	Characteristics	Condition	Min	Typ	Max	Unit
T1	CLKP Hi to SERIOUTP change timing	readout_speed=2(10Mbps)	9	11	13	ns
T2	SERIOUT - STROBE timing	readout_speed=2(10Mbps) strobe_select=0,1	1	2	3	ns
T3	CLKP Hi - STROBE timing	readout_speed=2(10Mbps) strobe_select=3	11	13	15	ns

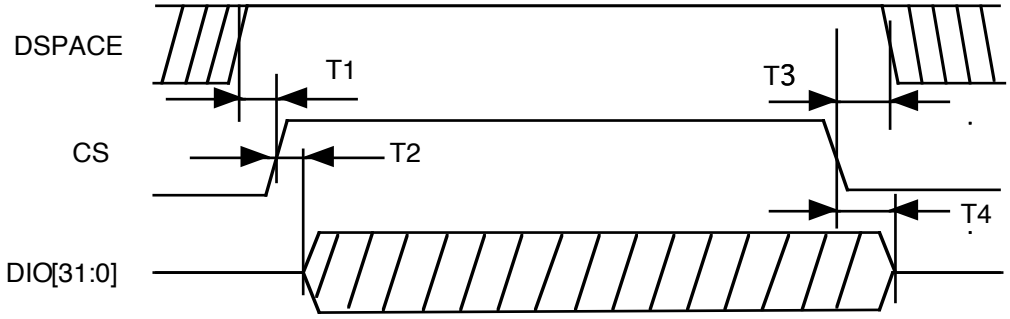
[Serial Output Timing (speed=3)]



Symbol	Characteristics	Condition	Min	Typ	Max	Unit
T1	CLKP Hi to SERIOUTP change timing	readout_speed=2(10Mbps)	7	9	11	ns
T2	SERIOUT-STROBE timing	readout_speed=2(10Mbps) strobe_select=0,1	0	1	2	ns
T3	SERIOUT-STROBE timing	readout_speed=2(10Mbps) strobe_select=3	0	1	2	ns

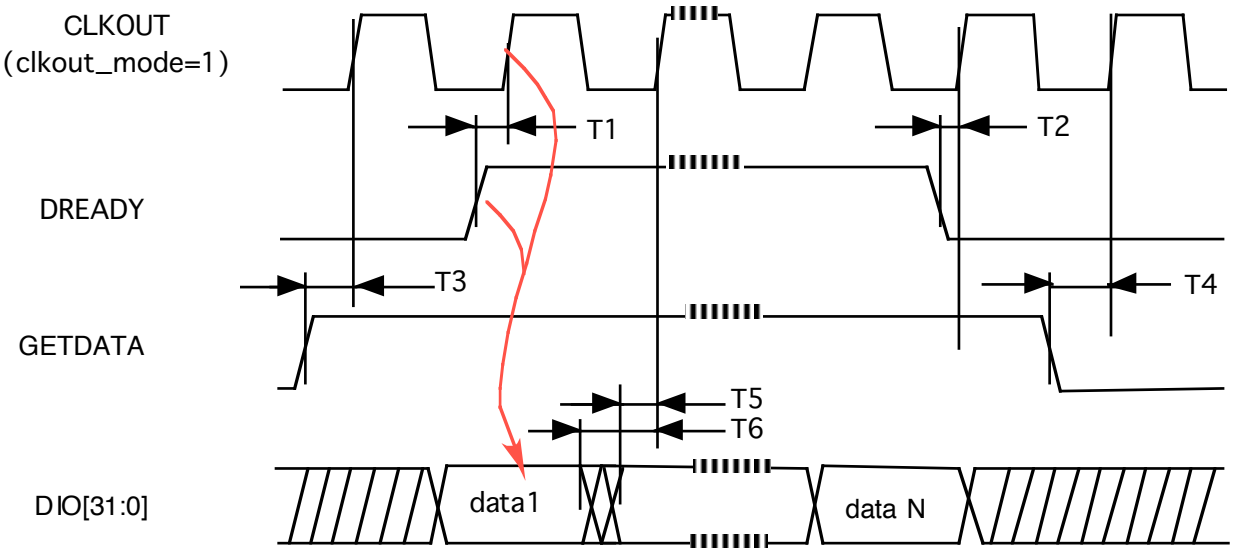
2.4.7.Parallel Output Timing

[DIO Enable Timing]



Symbol	Characteristics	Condition	Min	Max	Unit
T1	DSPACE to CS setup time		1		ns
T2	CS negate to DSPACE hold time		2		ns
T3	CS assert to DIO enable time			17	ns
T4	CS assert to DIO disable time			10	ns

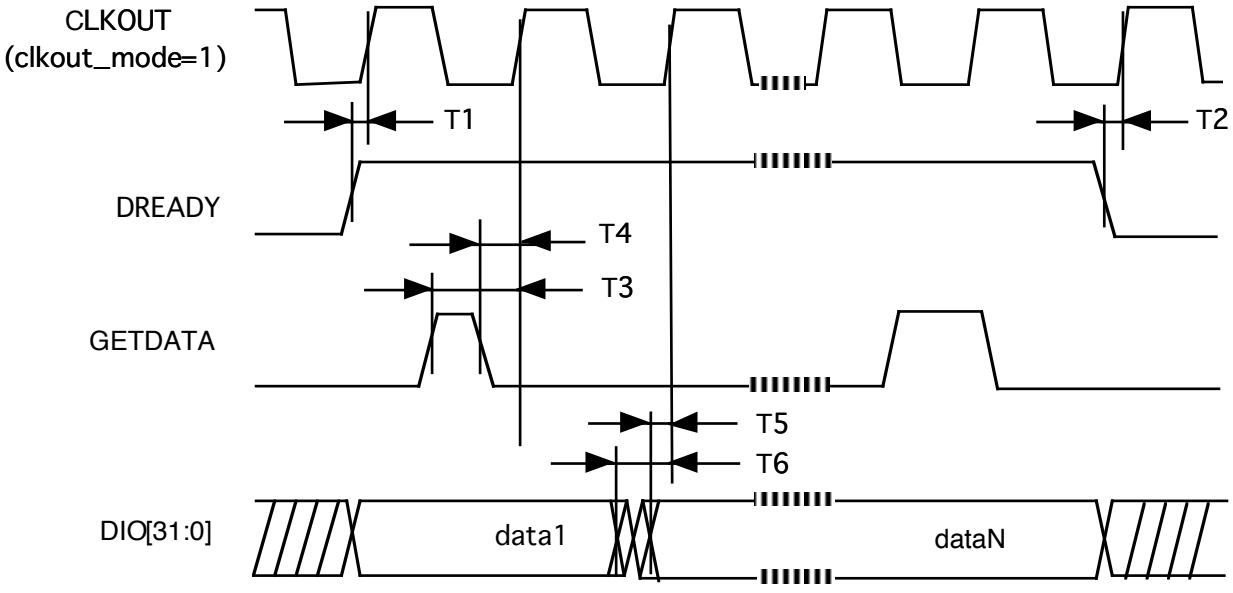
[Parallel Output Timing (synchronous mode : strobe_select[0]=0)]



Data are synchronous with the CLK40 signal. You can read valid data when DREADY & CLKOUT is asserted. GETDATA can be fixed to high level or used to pause the data stream.

Symbol	Characteristics	Condition	Min	Typ	Max	Unit
T1	DREADY assert to CLKOUT time	clkout_mode=1	0.5	1	1.5	ns
T2	DREADY negate to CLKOUT time	clkout_mode=1	1	1.5	2	ns
T3	GETDATA assert time		13			ns
T4	GETDATA negate time		9			ns
T5	DIO stable to CLKOUT time	clkout_mode=1	0			ns
T6	DIO unstable to CLKOUT time	clkout_mode=1			5	ns

[Parallel Output Timing (handshake mode : strobe_select[0]=1)]

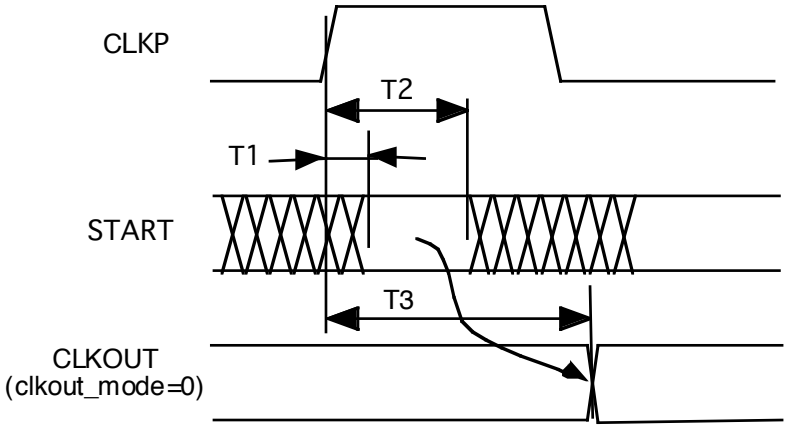


CLKOUT signal is shown only for timing reference purpose and not necessarily required.

Symbol	Characteristics	Condition	Min	Typ	Max	Unit
T1	DREADY assert to CLKOUT time	clkout_mode=1		1		ns
T2	DREADY negate to CLKOUT time	clkout_mode=1		1		ns
T3	GETDATA setup time		9			ns
T4	GETDATA hold time				6	ns
T5	DIO stable to CLKOUT time		0			ns
T6	DIO unstable to CLKOUT time				5	ns

2.4.8.START signal Timing

[START signal timing]



Symbol	Characteristics	Condition	Min	Typ	Max	Unit
T1	START setup time				1.0	ns
T2	START hold time		3.5			ns
T3	CLKP to CLKOUT (Start_Sync) change time	clkout_mode=0		13.5		