SIS3500
VME Discriminator

User Manual

SIS GmbH
Moorhof 2d
22399 Hamburg
Germany

Phone: ++49 (0) 40 60 87 305 0
Fax: ++49 (0) 40 60 87 305 20

email: info@struck.de
http://www.struck.de

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2 Introduction

The SIS3500 is a 16 channel VME discriminator.. The unit is based on the SIS350x printed circuit board. The analog section is implemented on a piggy pack card for better analog behaviour and increased flexibility to implement different front end cards, like a CFD or an updating leading edge version. The first implementation of the daughter card is of non updating leading edge type.
The unit is a single width (4 TE) 6U standard VME card requiring a CERN JAUX backplane with –5.2 V power.
Although the first series of the SIS350x is equipped with the JAUX connector, the basic design of the card is made in a fashion, that minimum layout changes are required to go to a VIPA card with J0 connector. The 160-pin 5 row connectors and the circuitry for the first mate first break pins for hot swap are already implemented to give an example.

As we are aware, that no manual is perfect, we appreciate your feedback and will try to incorporate proposed changes and corrections as quickly as possible. The most recent version of this manual can be obtained by email from info@struck.de, the revision dates are online under http://www.struck.de/manuals.htm.

3 Technical Properties/Features

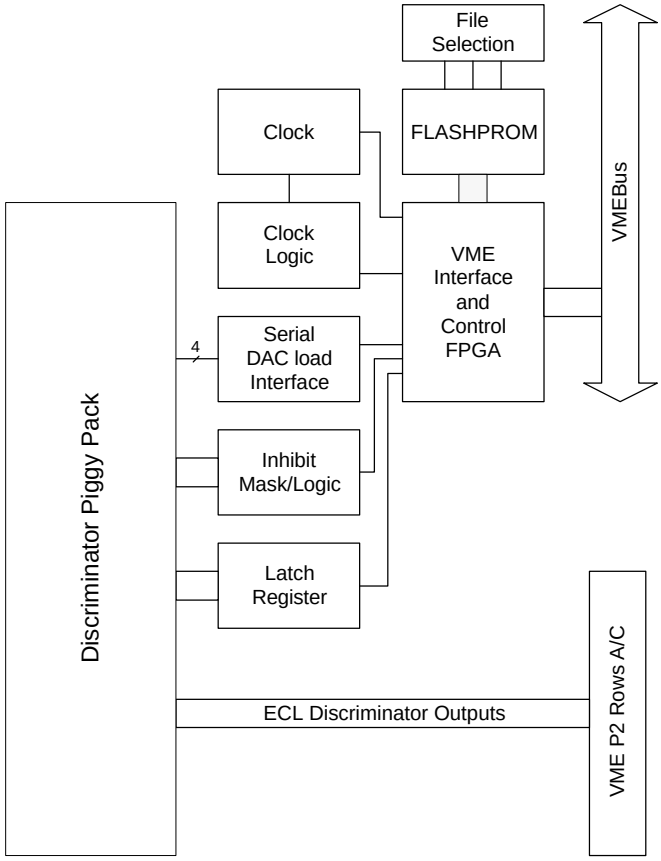
The SIS3500 is the combination of a VME carrier board and a non updating leading edge discriminator piggy pack. All inputs are fed to the unit via front panel input connectors, trigger (multiplicity, sum and fast OR) and active split outputs are located on the front panel also. The discriminated ECL output pulses can be accessed via the P2 connector with a standard DIN AC 64-pin connector.

Find below a list of key features/properties of the SIS3500.

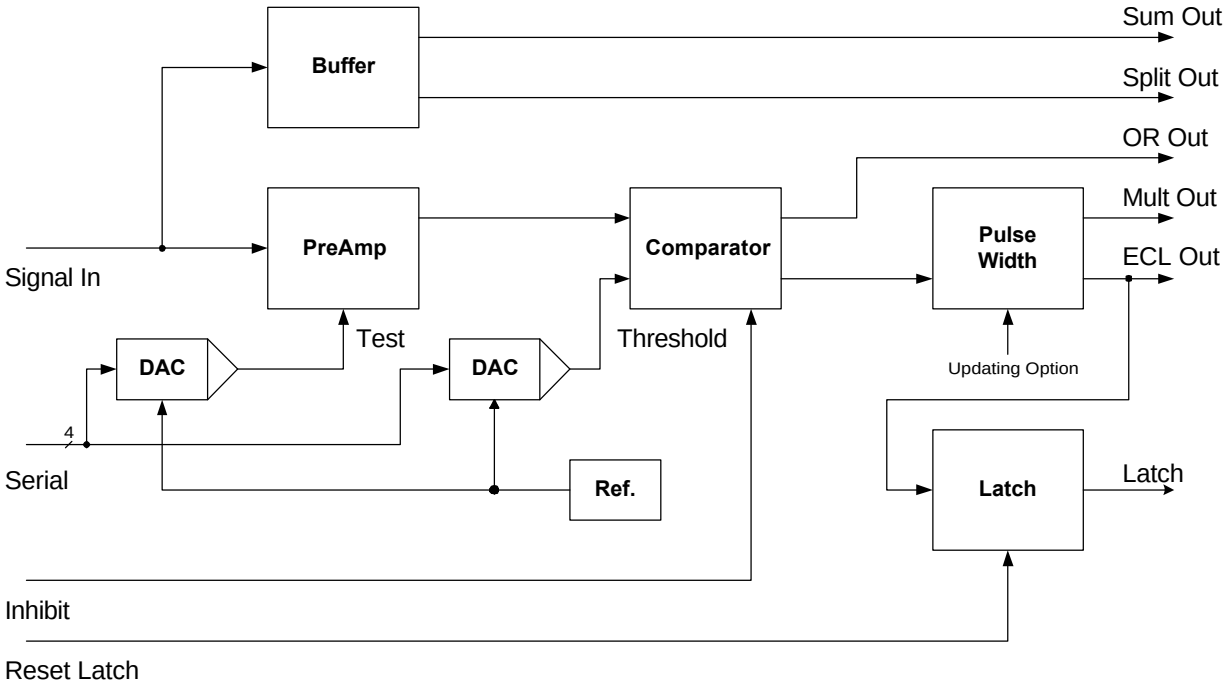
- 16 channels
- 12-bit threshold DACs
- 12-bit offset/test DAC
- individual threshold per channel
- 10 mV minimum threshold
- leading edge
- non updating
- LEMO input connectors
- active split on front panel
- sum output
- fast OR output
- multiplicity output
- common front panel inhibit
- software inhibit mask
- OR LED

3.1 Board Layout and theory of operation

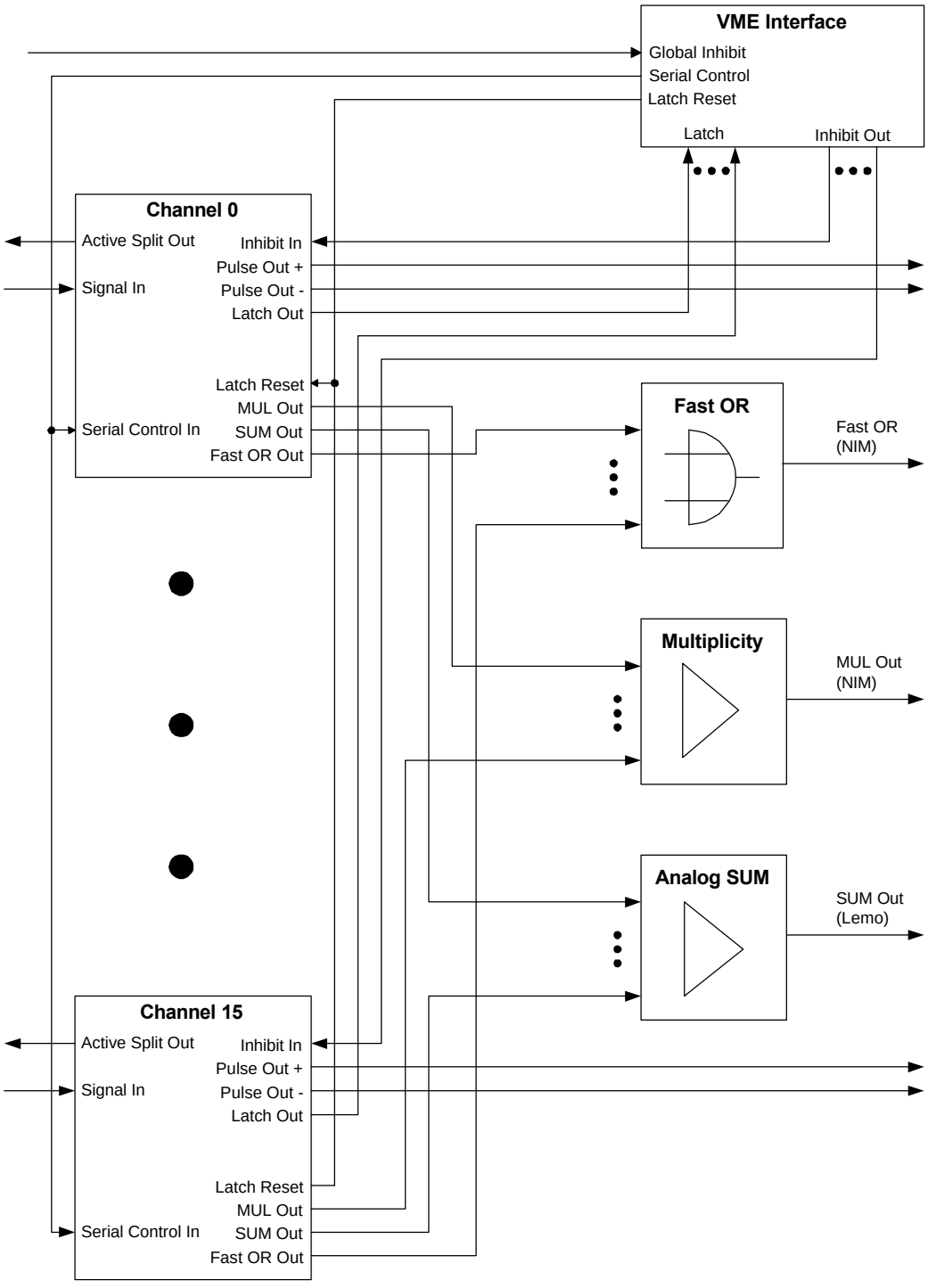
The SIS3500 consists of a VME baseboard with the VME interface and the control logic implemented in a Xilinx FPGA. The FPGA is loaded from a FLASHPROM upon power up. The user has the possibility to select among different boot files, for the time being the SIS3500 Version 1 is the only implementation. The individual thresholds are loaded to the DACs of the discriminator via a serial interface, hence all DACs have to be loaded sequentially. Two DACs (i.e. a LTC1446 dual DAC) are implemented per discriminator channel, one for the generation of the actual threshold setting and one to generate a test level (this DAC is typically set to zero during standard operation). New thresholds are set by writing the 32 DAC values to the DAC register. The old DAC setting is shifted to the DAC register and can be read back. This implies, that a readout of the actual threshold setting consists of a 32 fold alternate write read cycles to the DAC register.
It is recommended not to access the discriminator via VME during standard data taking operation, as VME bus activity may interfere with the analog portion of the board. In addition the user has the possibility to switch off the on board 50 MHz oscillator to reduce interference. With the clock switched off the card will react to accesses to the key address for clock enable only, access to other addresses on board will result in a bus error in this state.
The overall VME board layout is shown in the block diagram below, the setup of the individual channel and the logic for the generation of the different output signals is given in the following diagrams.



SIS3500 Block Diagram



SIS3500 Single Channel Layout



SIS3500 Overall Layout

4 Getting Started

The minimum setup to operate the SIS3500 requires the following steps:

- Check the proper firmware design is selected (should be design zero, i.e. all jumpers of jumper array J40 set.
- Select the VME base address for the desired addressing mode
- Select the VME SYSRESET behaviour via J520
- turn the VME crate power off
- install the discriminator in the VME crate
- connect your signals
- turn crate power back on
- issue a key reset by writing to 0x10
- set freeze
- write the threshold values to the 32 DACs via the DAC register (at 0x6)
- remove freeze (to activate new DAC settings)
- write inhibit mask if desired
- clear internal inhibit by writing 0x100 to the control register (at 0x0)

A good way of checking first time communication with the SIS3500 (besides the VME access LED) consists of switching off the inhibit LED (with no LEMO front panel inhibit active).

4.1 Factory Default Settings

4.1.1 Adressing

SIS3500 boards are shipped with the En_A24 and the En_A16 jumpers installed and the rotary switches set to:

Switch	SW_A24U	SW_A24L	SW_A16	J A_11	Bits 7-4	Bits 3-0
Setting	3	5	3	0	0	0

Jumper A_11 is set (bit 11 cleared).
Hence the unit will respond to the following base addresses:

Mode	Base address
A24	0x353000
A16	0x3000

Firmware Design
Design 0 (SIS3500, Version 1) of the FLASHPROM is selected (all jumpers of jumper array J40 set).

4.1.2 System Reset Behaviour

The system reset behaviour of the SIS3500 can be defined via jumper J50. With a jumper between Pins 1 and 2 (upper two contacts) the SIS3500 is reset upon VME Sysreset. With pins 3 and 4 connected reset is driven by the onboard reset logic (i.e. upon power up).

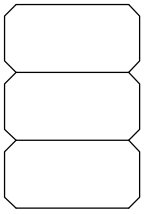
5 Firmware Selection

The FLASH PROM of a SIS350x board can contain several boot files. A list of available FLASHPROM versions can be found on our web site http://www.struck.de in the manuals page. If your FLASHPROM has more than one firmware design, you can select the desired firmware via the firmware selection jumper array J40 . The array is located near the FLASHPROM.

5.1 Examples

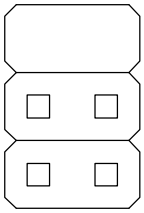
The figures below show jumper array 40 with the soldering side of the board facing the user and the VME connectors pointing to the right hand side.

Bootfile 0 selected



With all jumpers closed boot file 0 is selected

Bootfile 3 selected



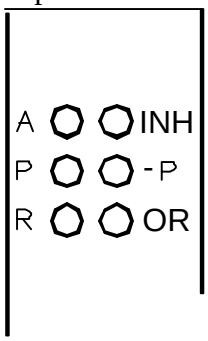
With the lowest two jumpers open bit 0 and bit 1 are set to 1 and hence boot file 3 is selected

Front Panel LEDs

The SIS3500 has 6 front panel LEDs to visualise part of the units status. Three LEDs according to the VME64xP standard (Power, Access and Ready) plus 3 additional LEDs (Inhibit, -5.2 V and OR).

Designation	LED	Color	Function
A	Access	yellow	Signals VME access to the unit
P	+5 V Power	red	Flags presence of +5V VME crate power
R	Ready	green	Signals configured logic
INH	Inhibit	yellow	External or internal inhibit set
-P	-5.2 V Power	red	Flags presence of –5.2 V VME crate power
OR	LED channel 2	green	

The LED locations are shown in the portion of the front panel drawing below.



The VME Access, the INH and the OR LEDS are monostable (i.e. the duration of the on phase is stretched for better visibility), the other LEDs reflect the current status.
An LED test cycle is performed upon power up (refer to the chapter 10).

6 VME addressing

6.1 Address Space

As bit 11 is the lowest settable bit on the 350x board, an address space of 2 Kbytes (Offset plus 0x000 to 0x7ff) is occupied by the module.

6.2 VME Base Address

The VME addressing mode (A16/A24) is selected via the jumpers EN_A16 and EN_A24.The mode is selected by closing the corresponding jumper, it is possible to enable two or all three addressing modes simultaneously.
The base address is set via the three rotary switches SW_A24U, SW_A24L and SW_A16 and the jumper J_A11. The table below lists the switches and jumpers and their corresponding address bits.

Switch/Jumper	Affected Bits
SW_A24U	23-20
SW_A24L	19-16
SW_A16	15-12
J_A11	11

In the table below you can see, which jumpers and switches are used for address decoding in the three different addressing modes (fields marked with an x are used).

	SW_A24U	SW_A24L	SW_A16	J_A11
A24	x	x	x	x
A16			x	x

Note: J_A11 closed represents a 0, J_A11 open a one

6.3 Address Map

The SIS350x boards are operated via VME registers and VME key addresses. The following table gives an overview on all SIS3500 addresses and their offset from the base address, a closer description of the registers and their function is given in the following subsections.

Offset	Key	Access	Type	Function
0x00		R/W	D16	Control and Status register
0x02		R/W	D16	Inhibit mask register
0x04		R/W	D16	Module Identification register
0x06		R/W	D16	DAC register
0x08		R/W	D16	ECL Latch register
0x10	KA	W	D16	Key reset
0x12	KA	W	D16	Key clear latch
0x20	KA	W	D16	Key enable clock
0x22	KA	W	D16	Key disable clock

Note: D32 and D08 is not supported by the SIS350x boards

The shorthand KA stands for key address. Write access with arbitrary data to a key address initiates the specified function

7 Register Description

7.1 Status Register (0x0)

The status register reflects the current settings of most of the SIS3500 parameters in read access, in write access it functions as the control register.

Bit	Function
15	Version Bit 3
14	Version Bit 2
13	Version Bit 1
12	Version Bit 0
11	0
10	0
9	0
8	Status external inhibit
7	0
6	0
5	0
4	0
3	
2	
1	Status freeze DAC
0	Status internal inhibit

The reading of the status register after power up or key reset is 0x1001 (see default settings of control register).

7.2 Control Register (0x0)

The control register is in charge of the control of most of the basic properties of the SIS3500 board in write access. It is implemented via a selective J/K register, a specific function is enabled by writing a 1 into the set/enable bit, the function is disabled by writing a 1 into the clear/disable bit (which has a different location within the register). An undefined toggle status will result from setting both the enable and disable bits for a specific function at the same time.
On read access the same register represents the status register.

Bit	Function
15	
14	
13	
12	
11	
10	
9	clear DAC freeze bit (*)
8	clear internal inhibit
7	
6	
5	
4	
3	
2	
1	set DAC freeze bit
0	set internal inhibit (*)

(*) denotes the default power up or key reset state

7.3 Inhibit register (0x2)

The output of individual channels or a group of channels can be masked by setting the bit of the corresponding channel in the inhibit register. Masked channels to not contribute to the fast OR and the multiplicity. The actual inhibit status can be read back.
Example: to mask channels 9 and 12 you would write 0x 1200 to the mask register.

7.4 Module Identification register (0x4)

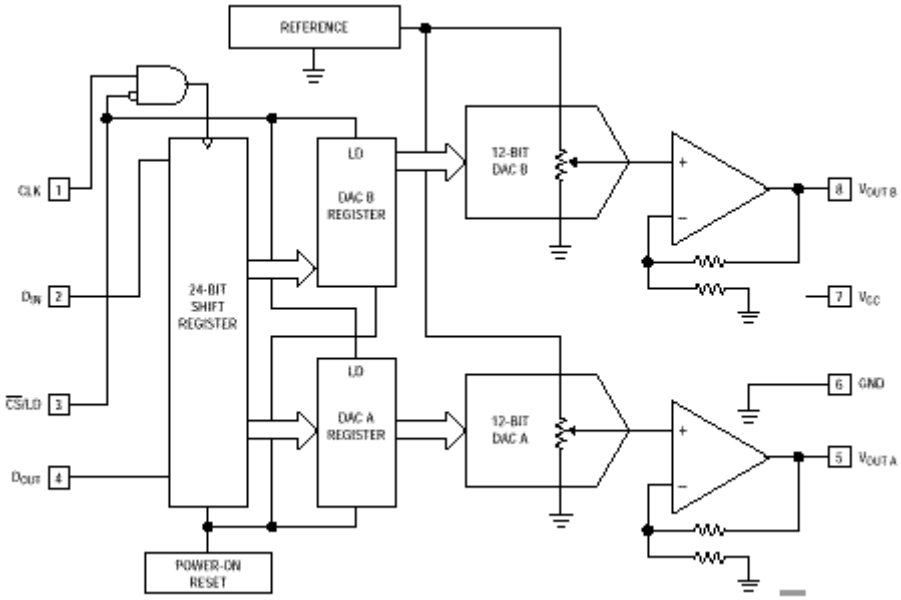
This register has the function to give information on the active firmware design. It is implemented via the read only upper 20 bits of the register. Bits 16-31 hold the four digits of the SIS module number (like 3807 or 3600 e.g.), bits 12-15 hold the version number. The version number allows a distinction between different implementations of the same module number, the SIS3806 for example has the 24-bit mode with user bits and the straight 32-bit mode as versions.

Bit	Read/Write access	Function	
15	read only	Module Identification Bit 15	Module Id Digit 3
14	read only	Module Identification Bit 14	
13	read only	Module Identification Bit 13	
12	read only	Module Identification Bit 12	
11	Read only	Module Identification Bit 11	Module Id Digit 2
10	read only	Module Identification Bit 10	
9	read only	Module Identification Bit 9	
8	read only	Module Identification Bit 8	
7	read only	Module Identification Bit 7	Module Id Digit 1
6	read only	Module Identification Bit 6	
5	read only	Module Identification Bit 5	
4	read only	Module Identification Bit 4	
3	read only	Module Identification Bit 3	Module Id Digit 0
2	read only	Module Identification Bit 2	
1	read only	Module Identification Bit 1	
0	read only	Module Identification Bit 0	

Module identification and version example:
The register for a SIS3500 reads 0x3500, the loaded firmware version can be obtained from bits 12-15 of the status register.

7.5 DAC register (0x6)

All thresholds are set through the DAC register. As the 32 DACs of the board are daisy chained, the user has to write data to all DACs if the value of an individual DAC is to be changed. The second DAC per channel is installed for test purposes and can be used to shift the input signal, in standard operation this DAC will be set to zero in most applications. By 32 alternate write read cycles to and from the DAC register the previous DAC settings can be read back. The data are read back from the DACs shift register, it is not possible to read them back from the DAC register directly, as shown in the DAC block diagram (from the LTC1446 data sheet).



Note: It is recommended to freeze all DACs via the freeze DAC bit in the control register, to download the new values and to unfreeze the DACs via the clear freeze DAC bit for the new threshold values to come into effect.

The DACs are set in the order:

1	Test/Offset DAC channel 0
2	Threshold DAC channel 0
31	Test/Offset DAC channel 15
32	Threshold DAC channel 15

The dual DACs have 12 bits, which are used to generate a threshold setting between 0 and 2 V, hence one bit corresponds to about 0.5 mV. The actual DAC offset is a channel parameter and has to be determined in a calibration measurement. The minimum threshold is specified to be 10 mV (offset corrected), lower settings may be possible in the given application. The test or offset DAC can be used to shift the input signals to higher values what allows the user to work with a higher threshold setting, what may result in a lower noise contribution.

7.6 Latch register (0x8)

The output status of the individual channels is latched into the 16 bits of the latch register as soon as a channel exceeds his threshold. The status of the latch register can be cleared via the key address 0x12 (key clear latch). The latch register can be used to test the input level of a channel or to test the threshold DAC against the latch DAC.

8 Connector Specification

The three different types of front panel and VME connectors used on the SIS3500 boards are:

Connector	Purpose	Part Number
96 pin abc	VME P1/P2	ERNI e.g.
30 pin abc	JAUX	ERNI e.g.
LEMO	All front panel connectors	LEMO ERN.00.250.CTL

8.1 Discriminator Output Pinning

The discriminated ECL output signals are routed to rows A and C of the P2 VME bus connector. This is done in a fashion, that cabling to the digitising electronics like TDCs or scalers is straightforward with the use of a DIN 64-pin A-C crimp connector (Schuricht part number xx.xx.xx e.g.) twisted pair ribbon cable and standard 34-pin header connectors. Find below the pinout on the P2 connector like seen when viewed from behind of the VME crate:

	Connector Row		
Pin	C	B	A
1	CH0 +		CH0 -
2	CH1 +		CH1 -
3	CH2 +		CH2 -
4	CH3 +		CH3 -
5	CH4 +		CH4 -
6	CH5 +		CH5 -
7	CH6 +		CH6 -
8	CH7 +		CH7 -
9	CH8 +		CH8 -
10	CH9 +		CH9 -
11	CH10 +		CH10 -
12	CH11 +		CH11 -
13	CH12 +		CH12 -
14	CH13 +		CH13 -
15	CH14 +		CH14 -
16	CH15 +		CH15 -
17	GND		GND
18			
•			
•			
•			
32			

9 Operating conditions

9.1 Power Consumption/Voltage requirement

The power consumption is lower than +5 V xx A, -5.2V 3A (i.e. the power consumption is < xx W). An accurate measurement is yet to be done.

9.2 Cooling

Forced air flow is required for the operation of the SIS3500 board.

9.3 Insertion/Removal

Please note, that the VME standard does not support live insertion (hot swap). Hence crate power has to be turned off for installation and removal of SIS3500 discriminators.

9.4 Warm Upl

It is recommended to operate the discriminator after a “warm up” phase of 10 to 15 minutes to ensure minimum impact from thermal effects of the individual components.

10 LED (selftest)

During power up self test and LCA configuration all LEDs except the Ready (R) LED are on. After the initialisation phase is completed, the Ready (R) LED, the positive Power (P), the negative Power (-P) and the Inhibit LED will stay on. Differing behaviour indicates either a problem with the download of the firmware boot file or one or more LCA and/or the download logic (the reason may be a defective FLASHPROM or a wrong boot file selection).

11 Software Support

VME discriminator boards are tested at SIS with an OR VP6 VME CPU (Pentium II based) under Windows NT and a National Instruments CVI user interface. The actual VME C code makes use of the OR Windows NT driver, which has straightforward to read and understand routines like:

```
VMEA24StdWriteWord(a24address + KEY_RESET, 0x0);
rdata = VMEA24StdReadWord(a24address + STAT_REG);
```

In most cases the user setup will be using different hardware, a full fleshed real time operating system like VxWorks, and a different user interface. We still believe, that it is helpful to have a look at the code which is used to test the units and to take it as an example for the implementation of the actual scaler readout application. A floppy with our test software is enclosed with SIS3500 shipments.
Depending on the user feedback and co-operation we expect, that we will have drivers or at least example routines for the commonly used VME CPU operating systems at hand in the mid term.

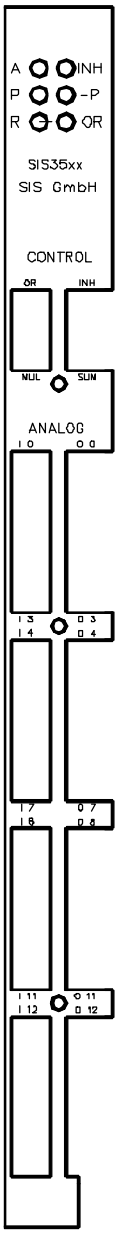
11.1 Contents of the included Floppy

The Floppy contains a readme.txt file with the most up to date information, the CVI project file and all home made files from the project. The important part of the code for the implementation of your own program is sitting in the CVI call back routines.
As an example for the minimum needed steps to use the card the FORTRAN code for the initialisation for the tests done at one of the HERMES DESY test DAQ systems is also on the floppy.

11.2 Front Panel Layout

The front panel of the SIS3500 is equipped with 6 LEDs and 4 LEMO control in- and outputs. The 16 inputs and the 16 active split outputs are of LEMO type also.

Note: Only the aluminium portion without the extractor handle mounting fixtures is shown



11.3 List of Jumpers

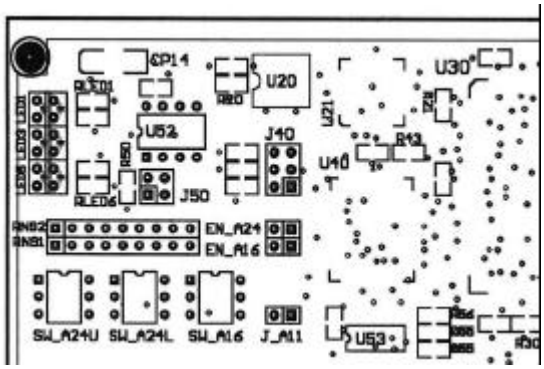
Find below a list of the jumpers and jumper arrays.

Jumper Name	Array/Single	Function
J40	Array	Boot File Selection
EN_A16	Single	Enable A16 addressing
EN_A24	Single	Enable A24 addressing
J_A11	Single	Address Bit 11 Selection

11.4 Jumper and rotary switch locations

11.4.1 Addressing mode and base address selection

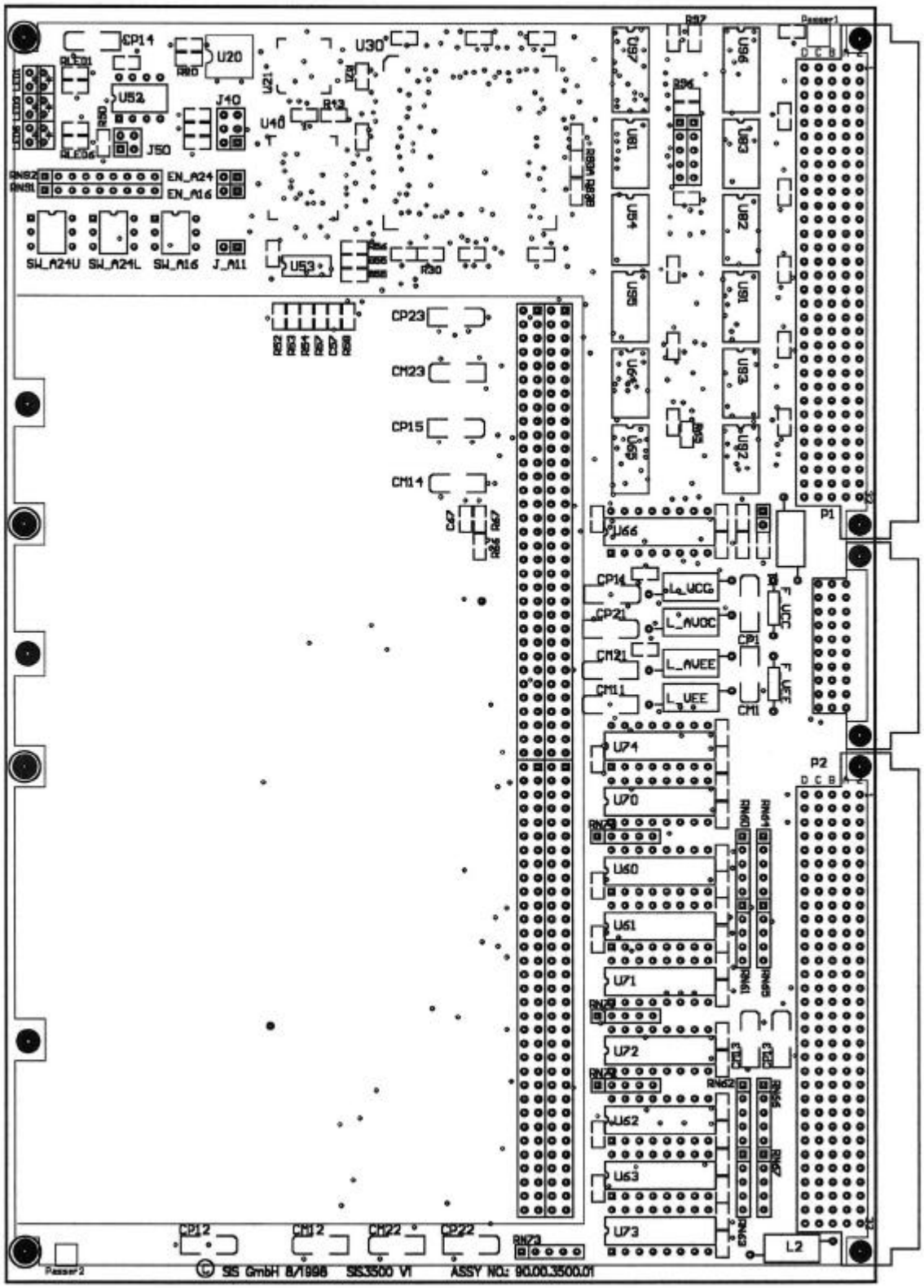
The EN_A24, EN_A16, A_11 and the 5 rotary switches are located to the left of the top section of the board, the corresponding section of the PCB is shown below.



11.4.2 J40 (Bootfile Selection)

The jumper array J40 is located next to the FLASHPROM and above the EN_A16 and EN_A24 as shown above. J50 is located to the left hand side of J40.

11.5 Motherboard Layout



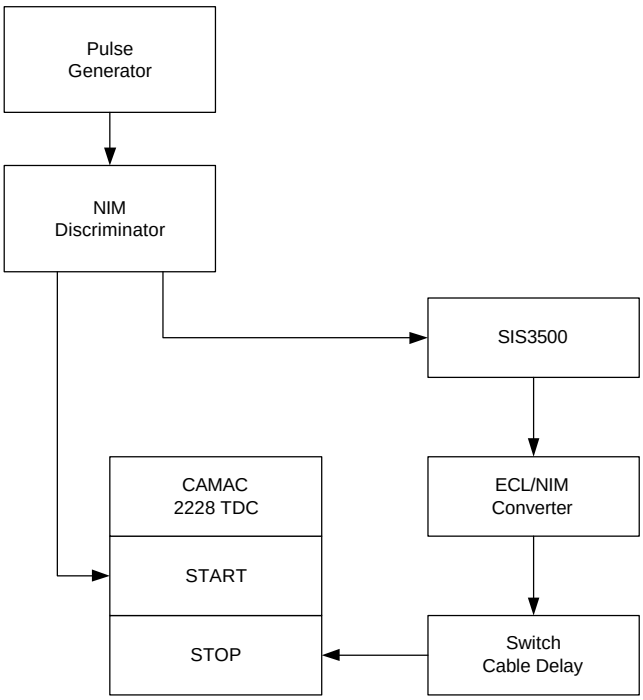
11.6 Signal Transition Times

Following signal transition times were measured with an oscilloscope with 5ns time divisions to an accuracy in the order of one ns. 50% level timings are used, more accurate data on the channel to channel deviations can be readily obtained during the calibration phase in the final DAQ environment:

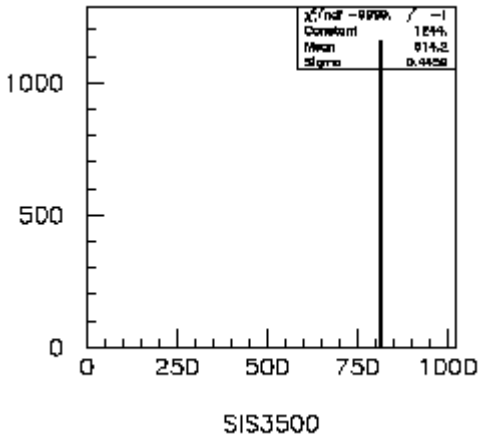
Signal In	Signal Out	Transition Time in ns	Variation in ns
Analog In	Active Split Out	< 2	< 1
Analog In	Discriminator Out	< 6	< 1
Analog In	Sum Out	< 12	< 1
Analog In	FAST OR Out	< 9	< 1
Analog In	Mult Out	< 18	< 1

11.7 Time resolution

A TDC measurement was performed to get a feeling for the contribution to the time resolution from the SIS3500 discriminator. The output signal of a pulser was fanned out through a NIM discriminator. One discriminator output was used as TDC start. The second discriminator output was used as analog input signal for a channel of the SIS3500 VME discriminator. The discriminated output was used as TDC stop after ECL to NIM level conversion and delay through a cable switch delay. The length of the flat cable between the VME discriminator P2 output and the level converter was in the order of 1.5 m. A Le Croy model 2228 CAMAC TDC was used to acquire the time spectrum. The data were histogrammed with PAW and a Minuit gaussian fit was applied. The overall setup resulted in a FWHM of 100 ps. With the intrinsic time resolution of all components of the setup taken into account the contribution of the SIS3500 will be negligible in most applications. In a second measurement the analog signal of the active split output of channel 0 was used as input for channel 1 and the channel 1 active split output was used as input for channel 2. The cable length in between of the channels was 5 ns. No significant broadening of the TDC spectrum of channel 1 could be seen. The overall setup was scattered over 3 NIM crates, the discriminator was plugged into a standard VME crate with –5.2 V supplied from a FASTBUS crate and the CAMAC TDC readout was done through FASTBUS. No VME transactions were executed during the acquisition of the TDC spectrum, the offset DACs were set to 0, the threshold DACs to 0x100 (i.e. some 125 mV). A sketch of the electronics setup is shown below:



Electronics Test Setup



TDC Spectrum

11.8 FLASHPROM Versions

A list of available FLASHPROMs can be obtained from http://www.struck.de/sis35firm.htm. Please note, that a special hardware configuration may be necessary for the firmware design of interest.
The table on the web is of the format shown below:

SIS350x FLASHPROM table

Design Name	Design	Boot File (s)
SIS3500_170998	0	SIS3500 Version 1

11.9 Additional Information on VME

The VME bus has become a popular platform for many realtime applications over the last decade. Information on VME can be obtained in printed form, via the web or from newsgroups. Among the sources are the VMEbus handbook, http://www.vita.com (the home page of the VME international trade association (VITA)) and comp.bus.arch.vmebus. In addition you will find useful links on many high energy physics labs like CERN or FNAL

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