SIS3305
5 GS/s, 2.5 GS/s, 1.25 GS/s 10-bit VME Digitizer

User Manual

SIS GmbH
Harksheider Str. 102A
22399 Hamburg
Germany

Phone: ++49 (0) 40 60 87 305 0
Fax: ++49 (0) 40 60 87 305 20

email: info@struck.de
http://www.struck.de

Version: sis3305-M-0x1009-1-v120.doc as of 06.06.2011

Revision Table:

Revision	Date	Modification
0.01	26.01.10	Generation
0.07	29.06.10	EV10EQ190 block diagram
1.00	16.08.10	0x1005 firmware Veto length logic
1.01	23.08.10	Mention bandwidth in SPI section
1.02	02.12.10	Change in SW80 default setting
1.10	08.03.11	0x1007 firmware - modified Veto Delay/Length logic - add Direct Memory Start Mode - add Direct Memory Wrap (Stop) Mode
1.20	06.06.11	0x1008/0x1009 firmware - add ADC-FPGA Individual Select/Set Veto logic - add Memory Overrun Veto logic

- Table of contents

1 Introduction

The SIS3305 is our first digitizer card with GS/s sampling speed. It's resolution of 10-bit in combination with the high channel count in 1.25 GS/s mode of operation makes it perfectly suited for many mid channel count applications in Particle Physics, Synchrotron Radiation, accelerator controls and related applications.
Two digitizer chips from e2v Technologies with 4 ADC cores each are used on the SIS3305. The flexible architecture of the digitizers with an analog cross bar, on chip clock logic and adjustable gain and offset allow for interleaved operation at 2.5 GS/s and 5 GS/s.

Applications comprise but are not limited to:

- MCP readout
- Fast detector readout
- Accelerator/machine controls

SIS3305 with veto input option

As we are aware, that no manual is perfect, we appreciate your feedback and will try to incorporate proposed changes and corrections as quickly as possible. The most recent version of this manual can be obtained by email from info@struck.de, the revision dates are online under http://www.struck.de/manuals.html.

1.1 Related documents

A list of available firmware designs can be retrieved from http://www.struck.de/sis3305firm.html .

2 Technical Properties/Features

2.1 Benefits

- High speed digitization with good resolution
- Low noise fixed gain input stage
- High channel density
- Fast readout
- Minimal event to event deadtime
- Availability of turnkey systems with ready to run software

2.2 Key functionality

Find below a list of key features of the SIS3305 digitizer.

- 8/4/2 channels with
- 1.25 GS/s, 2.5 GS/s or 5 GS/s sampling speed
- 10-bit resolution
- 2 GByte memory
- ACAM GPX TDC
- external/internal clock
- multi event mode
- read on the fly (actual sample value)
- pre/post trigger option
- readout in parallel to acquisition
- trigger generation
- sparsification
- differential clock output (two SMA connectors)
- differential clock input (two SMA connectors)
- 4 channel input piggy back
- A32 D32/BLT32/MBLT64/2e/SSTVME
- VME64x Connectors (operation in standard crate supported)
- VME64x Front panel
- VME64x extractor handles
- +5 V, +12V and –12 V VME standard voltages
- Optical 4-Gigabit link connection option or
- Veto input option

2.3 Input Stage Options

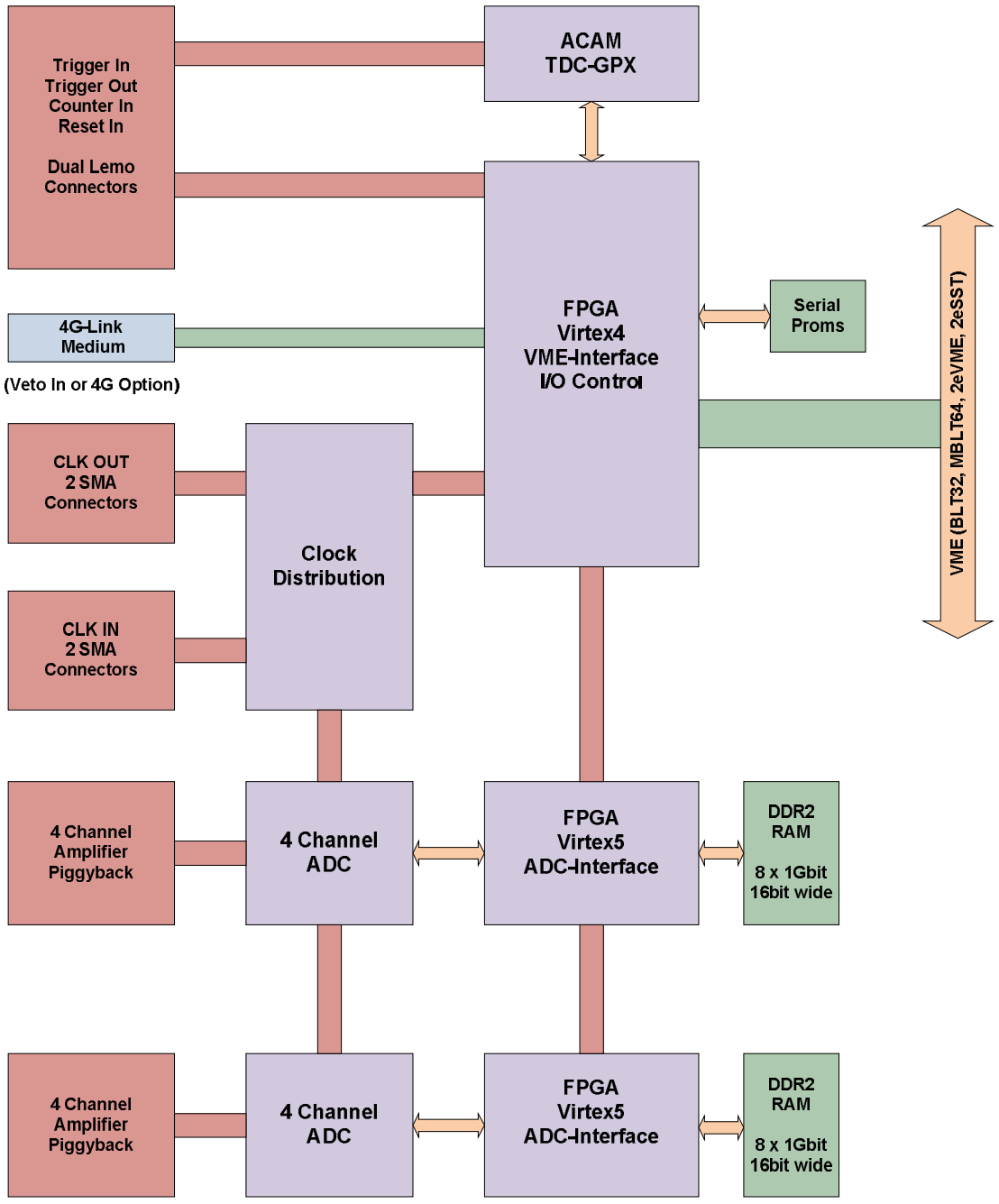
At this point in time the following input stage piggies are available

Card name	Coupling	Range	Bandwidth	Connectors
SIS3305_P4D_SMA	DC	-1 V, …,+1V	1,8 GHz	SMA
SIS3305_P4D_LEMO	DC	-1 V, …,+1V	400 MHz	LEMO

Feel free to inquire about custom input stage developments

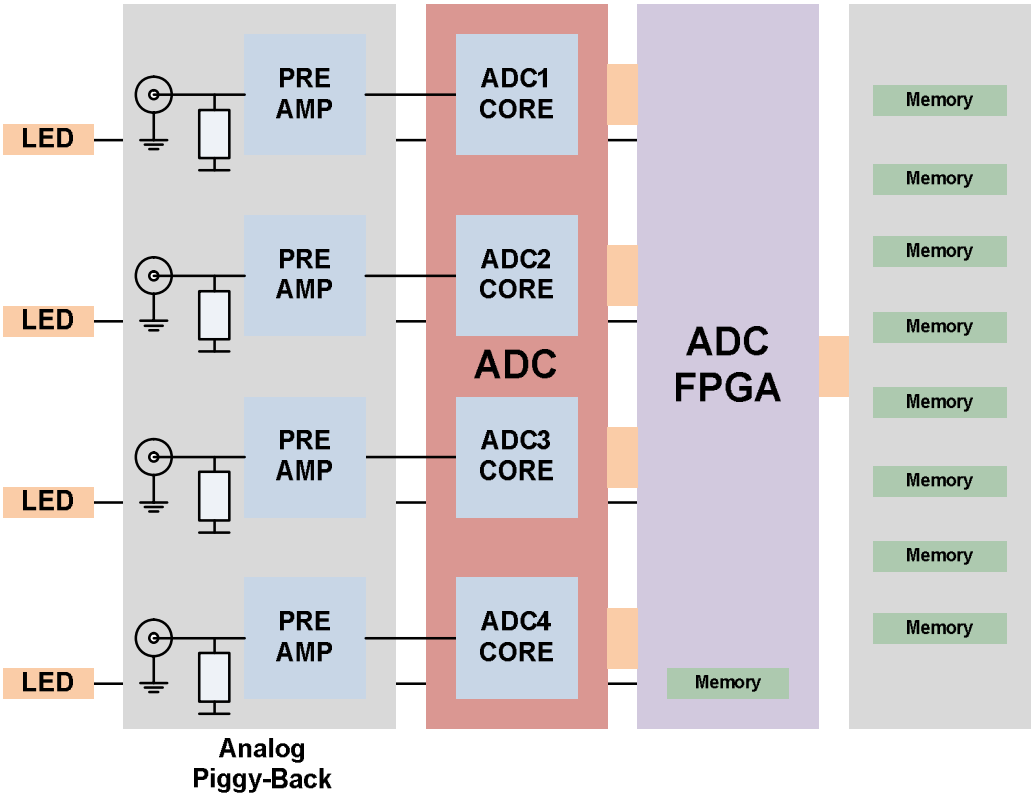
2.4 Module design

A simplified block diagram of the SIS3305 can be found below. The module is a dual four channel digitizer group design with control/interface section as illustrated in the simplified block diagram below..



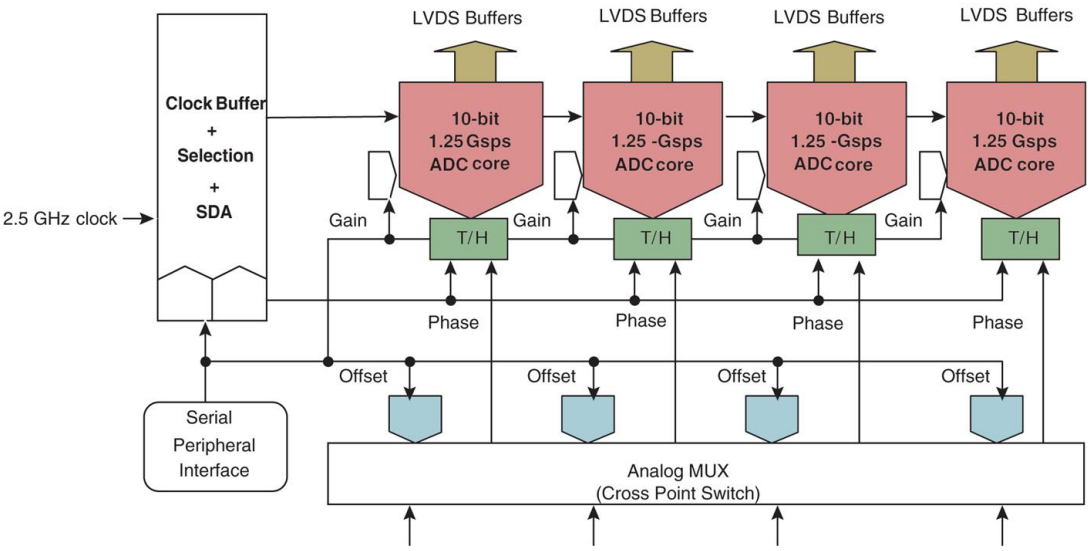
2.4.1 Four channel group

The structure of both four channel groups is identical. The ADC chip itself has four ADC cores and is connected to its peripherals as illustrated in the simplified scheme below.



2.4.2 EV10EQ190 Digitizer/ADC Chip

The EV10EQ190 chip from e2v Technologies is used as ADC chip on the SIS3305. It's architecture is illustrated below.



2.4.3 Memory handling

The SIS3305 has FPGA block memory and DDR2 memory resources.
The stream of digitized data from the ADC cores is recorded to the block memory of the FPGA continuously. Trigger handling, data processing, data formatting and storage to external DDR2 memory can be implemented in a flexible fashion in different firmware flavors.

2.4.4 Clock sources

The SIS3305 features following clock modes

- Internal fixed clock
- External differential clock

2.4.4.1 Internal clock

The internal clock is generated from an on board tunable quartz, the factory default configuration is 2.5 GHz.

2.4.4.2 External clock

A PECL symmetric differential clock can be supplied to the module through two SMA connectors. Typically this clock is coming from the clock output of another SIS3305 to operate two cards synchronously.

Min. sym. clock	Max sym. clock
400 MHz	2500 MHz

The duty cycle has to meet the criteria specified in the table below.

Mode	Min.	Max.
One channel	48%	52%
Two channel	40%	60%
Four channel	40%	60%

2.4.5 Trigger control (pre/post, start/stop and gate mode)

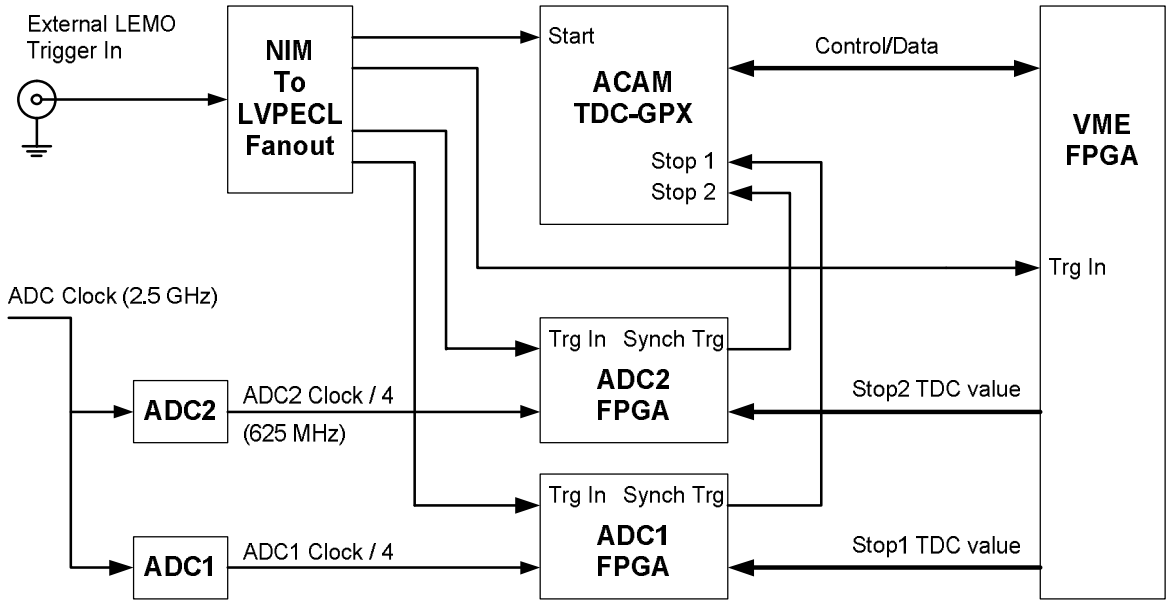
The modes of operation start, stop and gate in combination with the Ringbuffer delay and Pre Trigger Sample Length allow for the flexible implementation of acquisition schemes with and without pre- and post trigger samples.

2.4.6 Internal Trigger generation

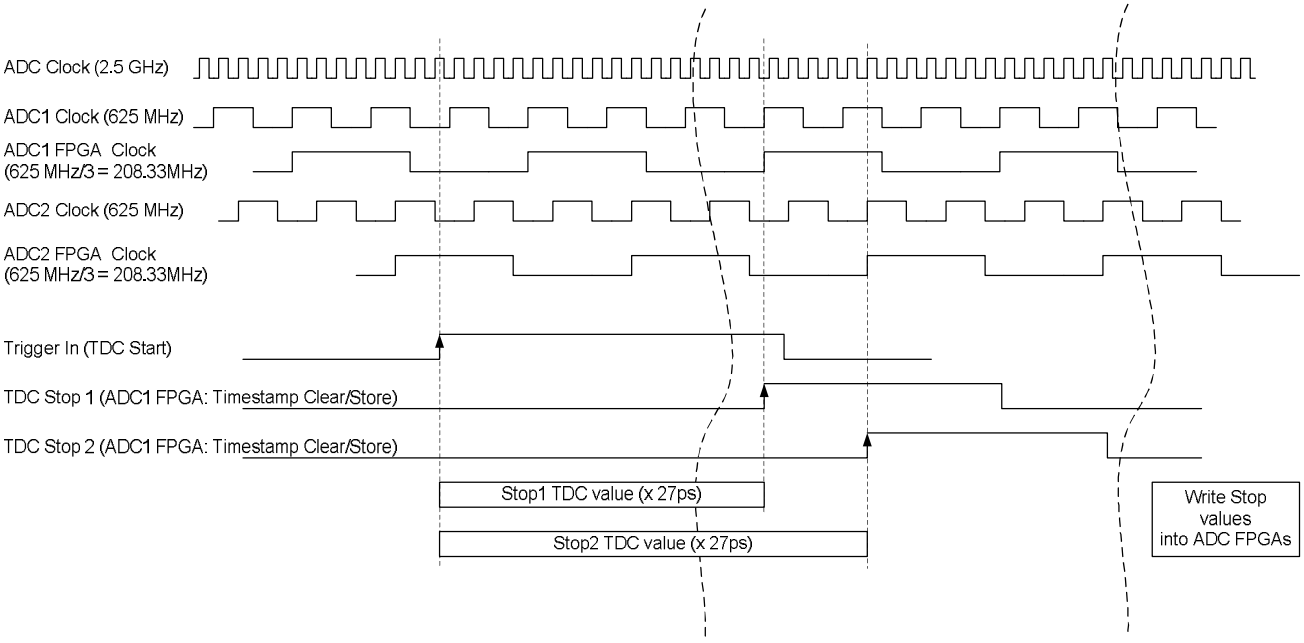
A set of 16 registers allows to set individual thresholds for the 8 channels with the two trigger conditions greater than (GT) and lower than (LT). Schmitt trigger like operation is supported via different values for the trigger on and trigger off conditions.

2.5 TDC

The TDC on the SIS3305 is used to measure the time between the external start signal and it's ADC-FPGA clock synchronized stop signal for the two ADC groups.
The TDC information (Stop 1 and Stop 2 values) is used in the process of ADC data (timing) rearrangement.



The TDC Measurement logic is implemented in the VME FPGA. If the Sample Logic and the TDC Measurement logic are enabled (Acquisition register bit 4 = 1) and the TDC is configured then it handles the timing measurement of the TDC. The stop values (in steps of 27ps) are written to the corresponding ADC FPGA to get the timing information relative to the internal timestamp for each TDC measurement (Start to Stop1/2).
The maximal trigger in rate is limited to 500kHz.



2.6 VME Interrupts

Eight interrupt sources are forseen, refer to sections 4.3 and 4.4 for details on the actual implementation. RORA or ROAK interrupter mode can be used.

3 VME Addressing

As the SIS3305 VME FADC has two times one GByte of memory (two times two GByte in V2), A32 addressing was implemented as the only option for the time being. The module occupies an address space of 0x00FF FFFF Bytes (i.e. 16 Mbyte).
The base address is defined by the selected addressing mode, which is selected by jumper array SW80 and SW1 and SW2 (in non geographical mode).

The table below summarises the possible base address settings.

SW80 Setting				Bits							
EN_A32	EN_ A16	EN_GEO	EN_RES	31	30	29	28	27	26	25	24
x				SW1				SW2			
	x			Not implemented in this design							
		x		Not implemented in this design							
			x	Not implemented in this design							

Shorthand	Explanation
SW1/SW2	Setting of rotary switch SW1 or SW2 respective

Notes:

- This concept allows the use of the SIS3305 in standard VME as well as in VME64x environments, i.e. the user does not need to use a VME64x backplane.
- The factory default setting is EN_A32 closed, SW1=4, SW2=1 (i.e. the module will react to A32 addressing under address 0x41000000). With more than one unit shipped in one batch a set of addresses (like 0x41000000, 0x42000000, 0x43000000,...) may be used also.
- The A16 jumper allows for a future changed addressing scheme with different resource allocation

3.1 Address Map Overview

The SIS3305 resources and their locations are listed in the tables below.

Note: Write access to a key address (KA) with arbitrary data invokes the respective action

Offset	BLT	Access	Function
0x000000 – 0x0000FC	-	W/R	VME FPGA registers
0x000400 – 0x00043C	-	W only	VME FPGA key addresses (with Broadcast functionality)
0x002000 – 0x002FFC	-	R/W	ADC1 ch1-ch4 FPGA registers
0x003000 – 0x003FFC	-	R/W	ADC2 ch5-ch8 FPGA registers
0x008000 – 0x00BFFC	-	R/W	ADC1 ch1-ch4 Memory Data FIFO
0x00C000 – 0x00FFFC	-	R/W	ADC2 ch5-ch8 Memory Data FIFO
or			
0x800000 – 0xBFFFFC	-	R/W	ADC1 ch1-ch4 Memory Data FIFO
0xC00000 – 0xFFFFFC	-	R/W	ADC2 ch5-ch8 Memory Data FIFO

3.1.1 VME FPGA registers

Offset	Size in Bytes	BLT	Access	Function
0x00000000	4	-	W/R	Control/Status Register (J-K register)
0x00000004	4	-	R only	Module Id. and Firmware Revision register
0x00000008	4	-	R/W	Interrupt configuration register
0x0000000C	4	-	R/W	Interrupt control register
0x00000010	4	-	R/W	Acquisition control/status register (J-K register)
0x00000014	4	-	R/W	Veto Length register
0x00000018	4	-	R/W	Veto Delay register
0x0000001C	4	-	R/W	reserved
0x00000020			R/W	TDC test register (only SIS internal use)
0x00000024			R/W	TDC test register (only SIS internal use)
0x00000028			R/W	EEprom 93C56 control register
0x0000002C			R/W	EEprom DS2430 onewire control register
0x00000030	4	-	R/W	CBLT/Broadcast Setup register
0x00000034	4	-	R/W	reserved
0x00000038	4	-	R/W	reserved
0x0000003C	4	-	R/W	reserved
0x00000040	4	-	R/W	LEMO Trigger Out Select register
0x00000044	4	-	R/W	reserved
0x00000048	4	-	R/W	reserved
0x0000004C	4	-	R	External Trigger In counter (TDC Event counter)
0x00000050	4	-	R/W	TDC Write Cmd register / TDC Status register
0x00000054	4	-	R/W	TDC Read Cmd register / TDC Read value register
0x00000058	4	-	R/W	TDC Start/Stop Enable register
0x0000005C	4	-	R/W	TDC FSM Reg4 value (used for TDC Master Reset) register

0x00000060			R/W	XILINX JTAG_TEST/JTAG_DATA_IN
0x00000070			R/W	Temperature and Temperature Supervisor Register
0x00000074			W only	ADC Serial Interface (SPI) register
0x000000C0			R/W	ADC1 ch1-ch4 FPGA Data Transfer Control register
0x000000C4			R/W	ADC2 ch5-ch8 FPGA Data Transfer Control register
0x000000C8			R only	ADC1 ch1-ch4 FPGA Data Transfer Status register
0x000000CC			R only	ADC2 ch5-ch8 FPGA Data Transfer Status register
0x000000D0			R only	Aurora Protocol Status
0x000000D4			R only	Aurora Data Status
0x000000D8			R only	Aurora Data Pending Request Counter Status

3.1.2 Key address registers

Offset	Size in Bytes	BLT	Access	Function
0x00000400	4	-	KA	General Reset
0x00000410	4	-	KA	Arm Sample Logic
0x00000414	4	-	KA	Disarm/Disable Sample Logic
0x00000418	4	-	KA	Trigger
0x0000041C	4	-	KA	Enable Sample Logic
0x00000420	4	-	KA	Set Veto
0x00000424	4	-	KA	Clear Veto
0x00000430	4	-	KA	ADC Clock Synchronisation
0x00000434	4	-	KA	Reset ADC-FPGA-Logic (DDR2-Memory, Aurora Interface)
0x0000043C	4	-	KA	Trigger Out pulse

3.1.3 ADC group 1 registers

Event information ADC group 1 (channel 1 - 4)				
0x02000	4	-	R/W	Event configuration register ADC1 ch1-ch4
0x02004	4		R/W	Sample Memory Start address register ADC1 ch1-ch4
0x02008	4		R/W	Sample/Extended Block Length register ADC1 ch1-ch4
0x0200C	4	-	R/W	Direct Memory Pretrigger Block Length register ADC1 ch1-ch4
0x02010	4	-	R/W	Ringbuffer Pretrigger Delay (ADC1 ch1-ch2)
0x02014	4	-	R/W	Ringbuffer Pretrigger Delay (ADC1 ch3-ch4)
0x02018	4	-	R/W	Direct Memory Max Nof Events register ADC1 ch1-ch4
0x0201C	4	-	R/W	End Address Threshold
0x02020	4	-	R/W	Trigger/Gate GT Threshold register ADC1 ch1
0x02024	4	-	R/W	Trigger/Gate LT Threshold register ADC1 ch1
0x02028	4	-	R/W	Trigger/Gate GT Threshold register ADC1 ch2
0x0202C	4	-	R/W	Trigger/Gate LT Threshold register ADC1 ch2
0x02030	4	-	R/W	Trigger/Gate GT Threshold register ADC1 ch3
0x02034	4	-	R/W	Trigger/Gate LT Threshold register ADC1 ch3
0x02038	4	-	R/W	Trigger/Gate GT Threshold register ADC1 ch4
0x0203C	4	-	R/W	Trigger/Gate LT Threshold register ADC1 ch4
0x02040	4	-	R	Sampling Status ADC1 ch1-ch4
0x02044	4	-	R	Actual Sample address register ADC1 ch1-ch4
0x02048	4	-	R	Direct Memory Event Counter ADC1 ch1-ch4
0x0204C	4	-	R	Direct Memory Actual Event Start address register ADC1 ch1-ch4
0x02050	4	-	R	Actual Sample Value ADC1 ch1-ch2
0x02054	4	-	R	Actual Sample Value ADC1 ch3-ch4
0x02058	4	-	R	Aurora Protocol/Data Status register ADC1
0x0205C	4	-	R	Internal Status register ADC1
0x02060	4	-	R	Aurora Protocol TX Live counter ADC1
0x02070	4	-	R /W	Individual Channel Select/Set Veto register ADC1 ch1-ch4
0x02074	4	-	R /W	reserved
0x02078	4	-	R /W	reserved
0x0207C	4	-	R /W	reserved
0x02400	4		R/W	Input Tap Delay register ADC1 ch1-ch4

3.1.4 ADC group 2 registers

Event information ADC group 2 (channel 5 - 8)				
0x03000	4	-	R/W	Event configuration register ADC2 ch5-ch8
0x03004	4		R/W	Sample Memory Start address register ADC2 ch5-ch8
0x03008	4		R/W	Sample/Extended Block Length register ADC2 ch5-ch8
0x0300C	4	-	R/W	Direct Memory Pretrigger Block Length register ADC2 ch5-ch8
0x03010	4	-	R/W	Ringbuffer Pretrigger Delay ADC2 ch5-ch6
0x03014	4	-	R/W	Ringbuffer Pretrigger Delay ADC2 ch7-ch8
0x03018	4	-	R/W	Direct Memory Max Nof Events register ADC2 ch5-ch8
0x0301C	4	-	R/W	End Address Threshold
0x03020	4	-	R/W	Trigger/Gate GT Threshold register ADC2 ch5
0x03024	4	-	R/W	Trigger/Gate LT Threshold register ADC2 ch5
0x03028	4	-	R/W	Trigger/Gate GT Threshold register ADC2 ch6
0x0302C	4	-	R/W	Trigger/Gate LT Threshold register ADC2 ch6
0x03030	4	-	R/W	Trigger/Gate GT Threshold register ADC2 ch7
0x03034	4	-	R/W	Trigger/Gate LT Threshold register ADC2 ch7
0x03038	4	-	R/W	Trigger/Gate GT Threshold register ADC2 ch8
0x0303C	4	-	R/W	Trigger/Gate LT Threshold register ADC2 ch8
0x03040	4	-	R	Sampling Status ADC2 ch5-ch8
0x03044	4	-	R	Next Sample address register ADC2 ch5-ch8
0x03048	4	-	R	Direct Memory Event Counter ADC2 ch5-ch8
0x0304C	4	-	R	Direct Memory Actual Event Start address register ADC2 ch5-ch8
0x03050	4	-	R	Actual Sample Value ADC2 ch5-ch6
0x03054	4	-	R	Actual Sample Value ADC2 ch7-ch8
0x03058	4	-	R	Aurora Protocol Status register ADC2
0x0305C	4	-	R	Internal Status register ADC2
0x03060	4	-	R	Aurora Protocol TX Live counter ADC2
0x03070	4	-	R /W	Individual Channel Select/Set Veto register ADC2 ch5-ch8
0x03074	4	-	R /W	reserved
0x03078	4	-	R /W	reserved
0x0307C	4	-	R /W	reserved
0x03400	4		R/W	Input Tap Delay register ADC2 ch5-ch8

4 Register Description

The function of the individual registers is described in detail in this section.
The first line after the subsection header (in Courier font) like:

```
#define SIS3305_CONTROL_STATUS          0x0         /* read/write; D32 */
```

refers to the SIS3305.h header file

4.1 Control/Status Register(0x0, write/read)

```
#define SIS3305_CONTROL_STATUS          0x0         /* read/write; D32 */
```

The control register is implemented as a selective J/K register, a specific function is enabled by writing a 1 into the set/enable bit, the function is disabled by writing a 1 into the clear/disable bit (which location is 16-bit higher in the register). An undefined toggle status will result from setting both the enable and disable bits for a specific function at the same time. The same register represents the status register on read access.

Bit	write Function	read Function
31	Clear Control LEMO Trigger Out (*)	0
30	Clear reserved 14 (*)	0
29	Clear Enable Memory Overrun Veto (*)	0
28	Clear Gate Mode External Veto In Delay/Length Logic (*)	0
27	Clear Invert External Veto In Delay/Length Logic (*)	0
26	Clear Edge sensitive External Veto Delay/Length Logic (*)	0
25	Clear Enable External LEMO Veto Delay/Length Logic (*)	0
24	Clear Invert External LEMO Direct Veto In (*)	0
23	Clear Enable External LEMO Trigger In (*)	0
22	Clear Enable External LEMO Count In (*)	0
21	Clear Enable External LEMO Reset In (*)	0
20	Clear Enable External LEMO Direct Veto In (*)	0
19	Clear Led-Application Mode (*)	0
18	Switch off user 3 LED (*)	0
17	Switch off user 2 LED (*)	0
16	Switch off user 1 LED (*)	0
15	Set Control LEMO Trigger Out (**)	Status Control LEMO Trigger Out
14	Set reserved 14	Status reserved 14
13	Set Enable Memory Overrun Veto	Status Enable Memory Overrun Veto
12	Set Gate Mode External Veto In Delay/Length Logic	Status Gate Mode External Veto In Delay/Length Logic
11	Set Invert External Veto In Delay/Length Logic	Status Invert External Veto In Delay/Length Logic
10	Set Edge sensitive External Veto Delay/Length Logic	Status Edge sensitivity External Veto Delay/Length Logic
9	Set Enable External LEMO Veto Delay/Length Logic	Status Enable External Veto Delay/Length Logic
8	Set Invert External LEMO Direct Veto In	Status Invert External LEMO Direct Veto In
7	Set Enable External LEMO Trigger In	Status Enable External LEMO Trigger In
6	Set Enable External LEMO Count In	Status Enable External LEMO Count In
5	Set Enable External LEMO Reset In	Status Enable External LEMO Reset In
4	Set Enable External LEMO Direct Veto In	Status Enable External LEMO Direct Veto In
3	Set Led-Application Mode	Status Led-Application Mode
2	Switch on user 3 LED	Status User 3 LED
1	Switch on user 2 LED	Status User 2 LED
0	Switch on user 1 LED	Status User 1 LED (1=LED on, 0=LED off)

(*) denotes power up default setting
(**) if enabled, see LEMO Trigger Out Select register

If Led-Application Mode = 0:

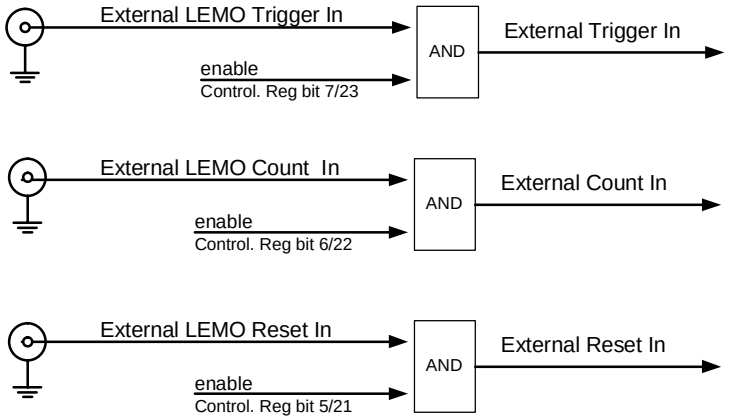
Led	Led On if
U1	Status User 1 LED = 1
U2	Status User 2 LED = 1
U3	Status User 3 LED = 1

If Led-Application Mode = 1:

Led	Led On if
U1	Status User 1 LED = 1
U2	Data sampling (ADC data transfer to Memory acitve)
U3	Data sample logic enabled

4.1.1 Enable for the External LEMO Inputs

The logic of the four LEMO inputs is illustrated in the diagram below



Note 1: The external inputs are disabled at power up
Note 2: The external trigger input is routed to the TDC independent of the status of the enable bit

Note 3: The Veto input is not present on cards with Optical Link Medium option

4.2 Module Id. and Firmware Revision Register (0x4, read)

```
#define SIS3305_MODID                    0x4        /* read only; D32 */
```

This register reflects the module identification of the SIS3305 and its minor and major firmware revision levels. The major revision level will be used to distinguish between substantial design differences and experiment specific designs, while the minor revision level will be used to mark user specific adaptations.

Bit	Function	Reading
31	Module Id. Bit 15	3
30	Module Id. Bit 14	
29	Module Id. Bit 13	
28	Module Id. Bit 12	
27	Module Id. Bit 11	3
26	Module Id. Bit 10	
25	Module Id. Bit 9	
24	Module Id. Bit 8	
23	Module Id. Bit 7	0
22	Module Id. Bit 6	
21	Module Id. Bit 5	
20	Module Id. Bit 4	
19	Module Id. Bit 3	5
18	Module Id. Bit 2	
17	Module Id. Bit 1	
16	Module Id. Bit 0	
15	Major Revision Bit 7	
14	Major Revision Bit 6	
13	Major Revision Bit 5	
12	Major Revision Bit 4	
11	Major Revision Bit 3	
10	Major Revision Bit 2	
9	Major Revision Bit 1	
8	Major Revision Bit 0	
7	Minor Revision Bit 7	
6	Minor Revision Bit 6	
5	Minor Revision Bit 5	
4	Minor Revision Bit 4	
3	Minor Revision Bit 3	
2	Minor Revision Bit 2	
1	Minor Revision Bit 1	
0	Minor Revision Bit 0	

4.2.1 Major revision numbers

Find below a table with major revision numbers used to date

Major revision number	Application/user
0x10	RoentDec designs

4.3 Interrupt configuration register (0x8)

```
#define SIS3305_IRQ_CONFIG                0x8         /* read/write; D32 */
```

This read/write register controls the VME interrupt behaviour of the SIS3305 ADC. Eight interrupt sources are foreseen, for the time being two of them are associated with an interrupt condition, the other condition is reserved for future use.
The interrupter type is DO8 .

4.3.1 IRQ mode

In RORA (release on register access) mode the interrupt will be pending until the IRQ source is cleared by specific access to the corresponding disable VME IRQ source bit. After the interrupt is serviced the source has to be activated with the enable VME IRQ source bit again.
In ROAK (release on acknowledge) mode , the interrupt condition will be cleared (and the IRQ source disabled) as soon as the interrupt is acknowledged by the CPU. After the interrupt is serviced the source has to be activated with the enable VME IRQ source bit again.

Bit	Function	Default
31		0
...		0
16		0
15		0
14		0
13		0
12	RORA/ROAK Mode (0: RORA; 1: ROAK)	0
11	VME IRQ Enable (0=IRQ disabled, 1=IRQ enabled)	0
10	VME IRQ Level Bit 2	0
9	VME IRQ Level Bit 1	0
8	VME IRQ Level Bit 0	0
7	IRQ Vector Bit 7; placed on D7 during VME IRQ ACK cycle	0
6	IRQ Vector Bit 6; placed on D6 during VME IRQ ACK cycle	0
5	IRQ Vector Bit 5; placed on D5 during VME IRQ ACK cycle	0
4	IRQ Vector Bit 4; placed on D4 during VME IRQ ACK cycle	0
3	IRQ Vector Bit 3; placed on D3 during VME IRQ ACK cycle	0
2	IRQ Vector Bit 2; placed on D2 during VME IRQ ACK cycle	0
1	IRQ Vector Bit 1; placed on D1 during VME IRQ ACK cycle	0
0	IRQ Vector Bit 0; placed on D0 during VME IRQ ACK cycle	0

The power up default value reads 0x 00000000

4.4 Interrupt control register (0xC)

```
#define SIS3305_IRQ_CONTROL                0xC          /* read/write; D32 */
```

This register controls the VME interrupt behaviour of the SIS3305 ADC. Eight interrupt sources are foreseen, for the time being two of them are associated with an interrupt condition, the others are reserved for future use.

Bit	Function (w)	(r)	Default
31	Update IRQ Pulse	Status IRQ source 7 (reserved)	0
30	unused	Status IRQ source 6 (reserved)	0
29	unused	Status IRQ source 5 (reserved)	0
28	unused	Status IRQ source 4 (reserved)	0
27	unused	Status IRQ source 3 (End Address Threshold Flag; level sensitive)	0
26	unused	Status IRQ source 2 (End Address Threshold Flag; edge sensitive)	0
25	unused	Status IRQ source 1 (Direct Memory Stopped Flag; level sensitive)	0
24	unused	Status IRQ source 0 (Direct Memory Stopped; edge sensitive)	0
23	Disable/Clear IRQ source 7	Status flag source 7	0
22	Disable/Clear IRQ source 6	Status flag source 6	0
21	Disable/Clear IRQ source 5	Status flag source 5	0
20	Disable/Clear IRQ source 4	Status flag source 4	0
19	Disable/Clear IRQ source 3	Status flag source 3	0
18	Disable/Clear IRQ source 2	Status flag source 2	0
17	Disable/Clear IRQ source 1	Status flag source 1	0
16	Disable/Clear IRQ source 0	Status flag source 0	0
15	unused	Status VME IRQ	0
14	unused	Status internal IRQ	0
13	unused	0	0
12	unused	0	0
11	unused	0	0
10	unused	0	0
9	unused	0	0
8	unused	0	0
7	Enable IRQ source 7	Status enable source 7 (read as 1 if enabled, 0 if disabled)	0
6	Enable IRQ source 6	Status enable source 6 (read as 1 if enabled, 0 if disabled)	0
5	Enable IRQ source 5	Status enable source 5 (read as 1 if enabled, 0 if disabled)	0
4	Enable IRQ source 4	Status enable source 4 (read as 1 if enabled, 0 if disabled)	0
3	Enable IRQ source 3	Status enable source 3 (read as 1 if enabled, 0 if disabled)	0
2	Enable IRQ source 2	Status enable source 2 (read as 1 if enabled, 0 if disabled)	0
1	Enable IRQ source 1	Status enable source 1 (read as 1 if enabled, 0 if disabled)	0
0	Enable IRQ source 0	Status enable source 0 (read as 1 if enabled, 0 if disabled)	0

The power up default value reads 0x 00000000

IRQ source 3: reached Address Threshold (level sensitive)
IRQ source 2: reached Address Threshold (edge sensitive)

IRQ source 1: Direct Memory Stopped Flag (level sensitive)
IRQ source 0: Direct Memory Stopped Flag (edge sensitive)

4.5 *Acquisition control register (0x10, read/write)*

```
#define SIS3305_ACQUISITION_CONTROL      0x10        /* read/write; D32 */
```

The acquisition control register is in charge of most of the settings related to the actual configuration of the digitization process.
Like the control register it is implemented in a J/K fashion.

Bit	Write Function	Read
31	Clear reserved 15 (*)	Status of ADC2 Memory Overrun Veto Flag
30	Clear reserved 14 (*)	Status of ADC1 Memory Overrun Veto Flag
29	Clear Clock Source Bit1	Status of Direct Memory Stopped Flag
28	Clear Clock Source Bit0	Status of Direct Memory Busy Flag
27	Clear reserved 11 (*)	Status of "Enabled Memory Overrun Veto Flag"
26	Clear reserved 10 (*)	Status of External Veto Delay/Length Logic
25	Clear reserved 9 (*)	Status of Internal Veto (Key Veto Flag)
24	Clear reserved 8 (*)	Status of External Direct Veto
23	Clear reserved 7 (*)	Status of ADC2 Memory End Address Threshold Flag
22	Clear reserved 6 (*)	Status of ADC1 Memory End Address Threshold Flag
21	Clear reserved 5 (*)	Status of ADC2 Events to Memory Logic Busy Flag
20	Disable Trigger-In TDC Measurement Logic (*)	Status of ADC1 Events to Memory Logic Busy Flag
19	Clear reserved 3 (*)	Status of Memory End Address Threshold Flag
18	Clear reserved 2 (*)	Status of Events to Memory Logic Busy Flag
17	Clear reserved 1 (*)	Status of ADC Sample Logic Enabled
16	Clear reserved 0 (*)	Status of ADC Sample Logic Armed
15	Set reserved 15	Status reserved 15
14	Set reserved 14	Status reserved 14
13	Set clock source Bit 1	Status clock source Bit 1
12	Set clock source Bit 0	Status clock source Bit 0
11	Set reserved 11	Status reserved 11
10	Set reserved 10	Status reserved 10
9	Set reserved 9	Status reserved 9
8	Set reserved 8	Status reserved 8
7	Set reserved 7	Status reserved 7
6	Set reserved 6	Status reserved 6
5	Set reserved 5	Status reserved 5
4	Enable Trigger-In TDC Measurement Logic	Status Enable Trigger-In TDC Measurement Logic
3	Set reserved 3	Status reserved 3
2	Set reserved 2	Status reserved 2
1	Set reserved 1	Status reserved 1
0	Set reserved 0	Status reserved 0

The power up default value reads 0x0

Direct Memory Event Mode Flag table:

Direct Memory Busy Flag	Direct Memory Stopped Flag	Clock Source
0	0	Not Busy
0	1	Not possible
1	0	Busy
1	1	Stopped

Clock source bit setting table:

Clock Source Bit1	Clock Source Bit0	Clock Source
0	0	Internal 2.5 GHz
0	1	External Clock
1	0	No clock
1	1	No clock

Enable Trigger-In TDC Measurement Logic:

Enable Trigger-In TDC Measurement Logic bit	
0	Disables the TDC Measurement Logic in the VME FPGA
1	Enables the TDC Measurement Logic in the VME FPGA

4.1 Veto Length register (0x14, read/write))

```
#define SIS3305_VETO_LENGTH              0x14
```

This registers defines the veto length setting. It is used if the External LEMO Veto Delay/Length logic is enabled in the control register.

Refer to sections 4.1.1 and 5.4.1 for an illustration of the External LEMO Veto Delay/Length logic.

Bit	31-0
Function	32-bit Veto Length value - Veto Length = (Veto Length value + 1) * 20ns

The power up default value is 0

4.2 Veto Delay register (0x18, read/write))

```
#define SIS3305_DELAY_LENGTH             0x18
```

This registers defines the veto delay setting. It is used if the External LEMO Veto Delay/Length logic is enabled in the control register.

Refer to sections 4.1.1 and 5.4.1 for an illustration of the External LEMO Veto Delay/Length logic.

Bit	31-0
Function	32-bit Veto Delay value - Veto Delay = (Veto Delay value + 1) * 20ns

The power up default value is 0

4.3 *EEprom 93C56 Control Register*

```
#define SIS3305_EEPROM_CONTROL_REG       0x28      /* read/write; D32 */
```

Provides access to the 2kbit onboard eeprom. The EEprom is organized as 128 words * 16bit.

Bit	Write Function	Read
31	reserved	EEprom Busy
30	reserved	0
29	reserved	0
28	EEprom Command: WRITE DISABLE	0
27	EEprom Command: WRITE ENABLE	0
26	EEprom Command: ERASE	0
25	EEprom Command: WRITE	0
24	EEprom Command: READ	0
23	reserved	0
22	EEprom Address bit 6	0
21	EEprom Address bit 5	0
20	EEprom Address bit 4	0
19	EEprom Address bit 3	0
18	EEprom Address bit 2	0
17	EEprom Address bit 1	0
16	EEprom Address bit 0	0
15	EEprom Write data bit 15	EEprom Read data bit 15
14	EEprom Write data bit 14	EEprom Read data bit 14
13	EEprom Write data bit 13	EEprom Read data bit 13
12	EEprom Write data bit 12	EEprom Read data bit 12
11	EEprom Write data bit 11	EEprom Read data bit 11
10	EEprom Write data bit 10	EEprom Read data bit 10
9	EEprom Write data bit 9	EEprom Read data bit 9
8	EEprom Write data bit 8	EEprom Read data bit 8
7	EEprom Write data bit 7	EEprom Read data bit 7
6	EEprom Write data bit 6	EEprom Read data bit 6
5	EEprom Write data bit 5	EEprom Read data bit 5
4	EEprom Write data bit 4	EEprom Read data bit 4
3	EEprom Write data bit 3	EEprom Read data bit 3
2	EEprom Write data bit 2	EEprom Read data bit 2
1	EEprom Write data bit 1	EEprom Read data bit 1
0	EEprom Write data bit 0	EEprom Read data bit 0

The power up default value reads 0x0

Programming: see in sis3305_configuration_readout_lib.c

```
// read access
int ee_93c56_read_word(unsigned int moduleAdr,
                       unsigned char adr,
                       unsigned short *data);

int ee_93c56_read_block(unsigned int moduleAdr,
                        unsigned char startAdr,
                        unsigned short *data,
                        unsigned char len);
```

```
// write access
int ee_93c56_write_word(unsigned int moduleAdr,
                        unsigned char adr,
                        unsigned short data);

int ee_93c56_write_block(unsigned int moduleAdr,
                         unsigned char startAdr,
                         unsigned short *data,
                         unsigned char len);


// erase to 0xFFFF access
int ee_93c56_erase_word(unsigned int moduleAdr,
                        unsigned char adr);

int ee_93c56_erase_block(unsigned int moduleAdr,
                         unsigned char startAdr,
                         unsigned char len);


// write and erase accesses need to 'write-enable' the device first
int ee_93c56_write_enable(unsigned int moduleAdr);
int ee_93c56_write_disable( unsigned int moduleAdr);
```

The EEprom information and the offsets as used by the SIS3305 base software are listed in the table below:

16-bit address offset	ADC mode	ADC channel 1		ADC channel 8
0	-	IOB Tap Delay		IOB Tap Delay
8	-	Phase adjust		Phase adjust
16	4-channel	Gain adjust		Gain adjust
24	4-channel	Offset adjust		Offset Gain adjust
32	2-channel (A,C)	Gain adjust		Gain adjust
40	2-channel (A,C)	Offset adjust		Offset Gain adjust
48	2-channel (B,D)	Gain adjust		Gain adjust
56	2-channel (B,D)	Offset adjust		Offset Gain adjust
64	1-channel (A)	Gain adjust		Gain adjust
72	1-channel (A)	Offset adjust		Offset Gain adjust
80	1-channel (B)	Gain adjust		Gain adjust
88	1-channel (B)	Offset adjust		Offset Gain adjust
96	1-channel (C)	Gain adjust		Gain adjust
104	1-channel (C)	Offset adjust		Offset Gain adjust
112	1-channel (D)	Gain adjust		Gain adjust
120	1-channel (D)	Offset adjust		Offset Gain adjust

EEprom DS2430 Onewire Control Register

```
#define SIS3305_ONE_WIRE_CONTROL_REG     0x2C      /* read/write; D32 */
```

Provides access to the 256-bit onboard EEprom. The EEprom is organized as 32 words * 8bit.

Bit	Write Function	Read
31	reserved	EEprom Busy
30	reserved	0
29	reserved	0
28	reserved	0
27	reserved	0
26	reserved	0
25	reserved	0
24	reserved	0
23	reserved	0
22	reserved	0
21	reserved	0
20	reserved	0
19	reserved	0
18	reserved	0
17	reserved	0
16	reserved	0
15	reserved	0
14	reserved	0
13	reserved	0
12	reserved	0
11	reserved	0
10	Onewire Command: RESET BUS	0
9	Onewire Command: WRITE BYTE	0
8	Onewire Command: READ BYTE	0
7	EEprom Write data bit 7	EEprom Read data bit 7
6	EEprom Write data bit 6	EEprom Read data bit 6
5	EEprom Write data bit 5	EEprom Read data bit 5
4	EEprom Write data bit 4	EEprom Read data bit 4
3	EEprom Write data bit 3	EEprom Read data bit 3
2	EEprom Write data bit 2	EEprom Read data bit 2
1	EEprom Write data bit 1	EEprom Read data bit 1
0	EEprom Write data bit 0	EEprom Read data bit 0

The Device Presence bit can be found in ‘EEprom Read data bit 0’ after executing a ‘RESET BUS’ command.
A value of ‘0’ indicates that at least 1 device is present on the Onewire bus.

The power up default value reads 0x0

Programming: refer to sis3305_configuration_readout_lib.c

```
// bus reset + presence bit
int ee_ds2430_reset(unsigned int moduleAdr);

int ee_ds2430_read_rom(unsigned int moduleAdr,
                       unsigned char *data) ;


// read access
int ee_ds2430_read_byte(unsigned int moduleAdr,
                        unsigned char adr,
                        unsigned char *data);

int ee_ds2430_read_block(unsigned int moduleAdr,
                         unsigned char startAdr,
                         unsigned char *data,
                         unsigned char len);


// write access
int ee_ds2430_write_byte(unsigned int moduleAdr,
                         unsigned char adr,
                         unsigned char data);

int ee_ds2430_write_block(unsigned int moduleAdr,
                          unsigned char startAdr,
                          unsigned char *data,
                          unsigned char len);


// erase to 0xFFFF access
int ee_ds2430_erase_byte(unsigned int moduleAdr,
                         unsigned char adr);

int ee_ds2430_erase_block(unsigned int moduleAdr,
                          unsigned char startAdr,
                          unsigned char len);
```

Struck definition of the DS2430 contents:

8-bit address offset	
0	Struck Serial Number (lower byte)
1	Struck Serial Number (upper byte)
2	User Serial Number (lower byte)
3	User Serial Number (upper byte)
4	TDC HSDiv value (High speed divider PLL)
.	free
31	free

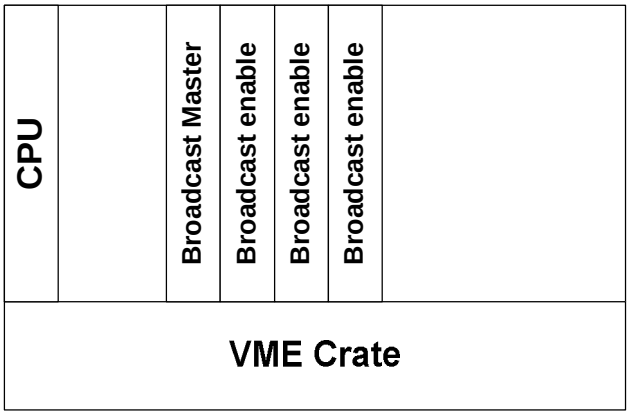
4.4 Broadcast setup register

```
#define SIS3305_CBLT_BROADCAST          0x30      /* read/write; D32 */
```

This read/write register defines, whether the SIS3305 will participate in a Broadcast. The configuration of this register and the registers of other participating modules is essential for proper Broadcast behaviour.

Bit	Function
31	Broadcast address bit 31
30	Broadcast address bit 30
29	Broadcast address bit 29
28	Broadcast address bit 28
27	Broadcast address bit 27
26	Broadcast address bit 26
25	Broadcast address bit 25
24	Broadcast address bit 24
23	reserved
22	reserved
21	reserved
20	reserved
19	reserved
18	reserved
17	reserved
16	reserved
15	reserved
14	reserved
13	reserved
12	reserved
11	reserved
10	0
9	0
8	0
7	0
6	0
5	Enable Broadcast Master
4	Enable Broadcast
3	0
2	reserved
1	reserved
0	reserved

Broadcast functionality is implemented for all Key address cycles.
Modules which are supposed to participate in a broadcast have to get the same broadcast address. The broadcast address is defined by the upper 8 bits of the broadcast setup register. One module has to be configured as broadcast master, the enable broadcast bit has to be set for all modules as illustrated below.



Broadcast setup example (broadcast address 0x30000000):

Module	Broadcast Setup Register	Comment
1	0x30000030	Broadcast Master + Broadcast enable
2	0x30000010	Broadcast enable
3	0x30000010	Broadcast enable
4	0x30000010	Broadcast enable

All 4 modules will participate in a key reset (A32/D32 write) to address 0x30000400.

Note: Do not use a broadcast address that is an existing VME address of a VME card in the crate.

4.5 *LEMO Trigger Out Select register (0x40, read/write)*

```
#define SIS3305_TRIGGER_OUT_SELECT_REG   0x40      /* read/write; D32 */
```

The selected conditions are ored to the LEMO Trigger Out connector.

Bit	Write Function
31	reserved
30	reserved
29	reserved
28	reserved
27	reserved
26	reserved
25	reserved
24	reserved
23	reserved
22	reserved
21	reserved
20	reserved
19	Select Memory Overrun Veto
18	Select External Veto Length Logic
17	Select Internal Veto (Key Veto Flag)
16	Select External Veto
15	Select Control LEMO Trigger Out (Control register bit 15)
14	Select Key Output Pulse
13	Select Sample Logic Enabled
12	Select Sample Logic Armed
11	Select Trigger In pulse (if Sample Logic and TDC Measurement Logic is enabled)
10	Select Trigger In pulse (if LEMO IN is enabled)
9	Select Trigger In (if LEMO IN is enabled)
8	Select Trigger In (direct)
7	Select Trigger ADC2 ch8
6	Select Trigger ADC2 ch7
5	Select Trigger ADC2 ch6
4	Select Trigger ADC2 ch5
3	Select Trigger ADC1 ch4
2	Select Trigger ADC1 ch3
1	Select Trigger ADC1 ch2
0	Select Trigger ADC1 ch1

4.6 *External Trigger In Counter*

```
#define SIS3305_EXTERNAL_TRIGGER_COUNTER 0x4C      /* read only; D32 */
```

This 32-bit Counter will be cleared if “the Sample Logic or the TDC Measurement Logic” is disabled.
It will be incremented with each External Trigger In Signal if “the Sample Logic and the TDC Measurement Logic” are enabled.

The TDC Measurement Logic writes the lower 4 counter bits with the TDC Stop values to the ADC FPGAs.

4.7 *TDC registers*

The SIS3305 is equipped with a ACAM TDC-GPX chip
Four TDC registers are implemented to control the TDC-GPX.

```
#define SIS3305_TDC_WRITE_CMD_REG               0x50  /* read/write; D32 */
#define SIS3305_TDC_READ_CMD_REG                0x54  /* read/write; D32 */
#define SIS3305_TDC_START_STOP_ENABLE_REG       0x58  /* read/write; D32 */
#define SIS3305_TDC_FSM_REG4_VALUE_REG          0x5C  /* read/write; D32 */
```

Programming: refer to sis3305_configuration_readout_lib.c

```
int SIS3305_TDC_Event_Mode_Setup(unsigned int module_addr,
                                 unsigned int uint_HSDiv)   ;
```

4.7.1 TDC Write Cmd / Read Status register (0x50, read/write)

Bit	Write Function	Read
31	TDC Write Address bit 3	0
30	TDC Write Address bit 2	0
29	TDC Write Address bit 1	0
28	TDC Write Address bit 0	0
27	TDC Write Data bit 27	0
26	TDC Write Data bit 26	0
25		0
24		0
23		0
22		0
21		0
20		0
19		0
18		0
17		0
16		0
15		0
14		0
13		0
12		0
11		0
10		0
9		0
8		0
7		0
6		0
5		TDC IRQ Flag
4		TDC Error Flag
3		TDC FIFO2 Load Flag
2		TDC FIFO1 Load Flag
1	TDC Write data bit 1	TDC FIFO2 Empty Flag
0	TDC Write data bit 0	TDC FIFO1 Empty Flag

The power up default value reads 0x0

4.7.2 TDC Read Cmd / Read Data register (0x54, read/write)

Bit	Write Function	Read
31	TDC Read Address bit 3	0
30	TDC Read Address bit 2	0
29	TDC Read Address bit 1	0
28	TDC Read Address bit 0	0
27	Reserved	TDC Read Data bit 27
26	Reserved	TDC Read Data bit 26
25		
24		
23		
22		
21		
20		
19		
18		
17		
16		
15		
14		
13		
12		
11		
10		
9		
8		
7		
6		
5		
4		
3		
2		
1	Reserved	TDC Read Data bit 1
0	Reserved	TDC Read Data bit 0

The power up default value reads 0x0

4.7.3 TDC Start/Stop Enable register (0x58, read/write)

Bit	Write Function
31	Reserved
30	Reserved
29	Reserved
28	Reserved
27	Reserved
26	Reserved
25	
24	
23	
22	
21	
20	
19	
18	
17	
16	
15	
14	
13	
12	
11	
10	
9	
8	
7	
6	
5	
4	
3	
2	TDC Stop2 Enable
1	TDC Stop1 Enable
0	TDC Start Enable

Note: Data are ored with TDC FSM data. To be used in test mode only (TDC test in software Loop)

4.7.4 XILINX JTAG_TEST register

#define SIS3305_XILINX_JTAG_TEST 0x60 /* write only; D32 */

This register is used in the firmware upgrade process over VME. A TCK is generated upon a write cycle to the register.

Bit	write Function
31	none
...	...
4	none
3	none
2	none
1	TMS
0	TDI

4.7.5 XILINX JTAG_DATA_IN register

#define SIS3305_XILINX_JTAG_DATA_IN 0x60 /* read only; D32 */

This register is used in the firmware upgrade process over VME. It is at the same address as the JTAG_TEST register and is used in read access. It operates as a shift register for TDO. The contents of the register is shifted to the right by one bit with every positive edge of TCK and the status of TDO is transferred to Bit 30. Bit 31 reflects the current value of TDO during a read access.

4.8 Temperature and Temperature Supervisor register (0x70, read/write))

```
#define SIS3305_INTERNAL_TEMPERATURE_REG       0x70   /* read/write; D32 */
```

The SIS3305 is equipped with a serial 10-bit Analog Devices AD7314 temperature sensor. The temperature reading is stored in twos complement format.

Refer to the AD7314 data sheet for more detailed information.

Bit	write	
31	Enable Temperature Supervisor	Enable Temperature Supervisor
...		0
28		Temperature Supervisor Threshold Flag
27		0
26		0
25	Temperature Threshold Bit 9 (MSB)	Temperature Threshold Bit 9 (MSB)
..		
17	Temperature Threshold Bit 1	Temperature Threshold Bit 1
16	Temperature Threshold Bit 0 (LSB)	Temperature Threshold Bit 0 (LSB)
15		0
…		
10		0
9		Temperature Data Bit 9 (MSB)
..		
1		Temperature Data Bit 1
0		Temperature Data Bit 0 (LSB)

The power up default value reads 0x80F00nnn

The default temperature threshold setting at power up or after a Key Reset command is 0x0F0 (60^{O} C).

The Temperature Supervisor Threshold Flag will be set if the value of the Temperature Data is higher than 0^{O} C and higher than the Temperature Threshold value. It will be cleared with a power on reset or with clear the “Enable Temperature Supervisor” bit.

If the Temperature Supervisor Threshold Flag is set then the Supervisor logic sets the both ADC chips to standby mode (under that condition it is no longer possible to write/read to/from the ADC chips via the SPI interface !), the logic of the ADC FPGAs are set to the reset state and the ADC clock is turned off.

The three USER Leds (U1,U2,U3) are flashing with 4 Hz to indicate the over temperature state (U2 is inverted to U1,U3).

The operating temperature ranges from -35 ^{O}C to +85 ^{O}C and is covered by the table below

Temperature	Data Bit 9 . . . Bit 0
–50 ^{O}C	11 0011 1000
–25 ^{O}C	11 1001 1100
–0.25 ^{O}C	11 1111 1111
0 ^{O}C	00 0000 0000
+0.25 ^{O}C	00 0000 0001
+10 ^{O}C	00 0010 1000
+25 ^{O}C	00 0110 0100
+50 ^{O}C	00 1100 1000
+75 ^{O}C	01 0010 1100
+100 ^{O}C	01 1001 0000

Note: The Celsius temperature reading is obtained by casting the read data to signed short and dividing the obtained value by 4.0 after float conversion.

4.9 ADC Serial Interface (SPI) register (0x74, read/write)

```
#define SIS3305_ADC_SERIAL_INTERFACE_REG       0x74   /* read/write; D32 */
```

Several parameters of the 10-bit 5 GS/s ADC e2V EV10AQ190 chip (like gain, 1 GHz/full bandwidth, offset, phase calibration e.g.) can be configured with the SPI (serial Peripheral Interface). The SPI register is the interface between the SIS3305 VME FPGA and the ADC SPIs.
Please refer to the documentation of the EV10AQ190 ADC chip for details.

Bit	write	read
31	SPI	Write/Read Logic BUSY Flag
...		“Set ADC Standby” Logic Busy Flag
...		“Force ADC Standby” Flag
24	ADC Select Bit	
23	Write Cmd	
22	Address Bit 6	
21	Address Bit 5	
20	Address Bit 4	
19	Address Bit 3	
18	Address Bit 2	
17	Address Bit 1	
16	Address Bit 0	
15	Write Data Bit 15 (MSB)	Read Data Bit 15 (MSB)
14	Write Data Bit 14	Read Data Bit 14
..		
1	Write Data Bit 1	Read Data Bit 1
0	Write Data Bit 0 (LSB)	Read Data Bit 0 (LSB)

The power up default value is 0x0

Programming: see in sis3305_configuration_readout_lib.c

```
int SIS3305_ADC_SPI_Setup(unsigned int module_addr,
                          struct SIS3305_ADC_SPI_Config_Struct*
                                 sis3305_ADC_SPI_configuration_struct)   ;
```

4.10 ADC1 ch1-ch4/ADC2 ch5-8 FPGA Data Transfer Control register (0xC0, 0xC4)

```
#define SIS3305_DATA_TRANSFER_ADC1_4_CTRL_REG   0xC0  /* read/write; D32 */
#define SIS3305_DATA_TRANSFER_ADC5_8_CTRL_REG   0xC4  /* read/write; D32 */
```

With a write to this (these) register(s) the fast data transfer logic (5GBit serial interface, between the ADC FPGA and VME FPGA) will execute the written "Command".

A "Reset Transfer FSM" command stops the fast data transfer logic and resets the FIFOs (ADC1 ch1-ch4 Memory Data FIFO, ADC2 ch5-ch8 Memory Data FIFO).

A "Start Read Transfer" command resets the FIFOs (ADC1 ch1-ch4 Memory Data FIFO, ADC2 ch5-ch8 Memory Data FIFO) and starts the fast data transfer "Read". The logic transfers the memory data from the written Start Address to the VME FPGA data FIFO controlled by the FIFO Halffull flag.

A "Start Write Transfer" command resets the FIFOs (ADC1 ch1-ch4 Memory Data FIFO, ADC2 ch5-ch8 Memory Data FIFO) and starts the fast data transfer "Write". The logic transfers the VME FPGA Data FIFO data to memory at the written Start Address controlled by the FIFO Empty flag (only possible if "ADC Memory Write via VME Test" is enabled; Event Configuration registers bit 15).

Bit	31-30	29-24	23-0
Function	Cmd	reserved	Memory Start 512-bit Block Address

default after Reset: 0x0

Command bit table:

Command Bit1	Command Bit0	function
0	-	Reset Transfer FSM
1	0	Start Read Transfer
1	1	Start Write Transfer

4.11 ADC1 ch1-ch4/ADC2 ch5-8 FPGA Data Transfer Status register (0xC8, 0xCC)

```
#define SIS3305_DATA_TRANSFER_ADC1_4_STATUS_REG      0xC8  /* read ; D32 */
#define SIS3305_DATA_TRANSFER_ADC5_8_STATUS_REG      0xCC  /* read ; D32 */
```

This set of two registers holds the status of the VME-ADC FPGA data transfer.

Bit	Function
31	Data Transfer Logic busy
30	Data Transfer Direction (Write-Flag; 0: Memory -> VME FPGA; 1: VME FPGA -> Memory)
29	FIFO (read VME FIFO) Data valid Flag
28	FIFO (read VME FIFO) Data AlmostFull Flag
27	“max_nof_pending_read_requests”
26	“no_pending_read_requests”
25	0
24	0
23	Data Transfer internal 512-block Address counter bit 23
	..
	..
0	Data Transfer internal 512-block Address counter bit 0

4.12 Aurora Protocol Status register (0xD0, read/write)

```
#define SIS3305_VME_FPGA_AURORA_PROT_STATUS    0xD0   /* read/write; D32 */
```

This register holds the VME FPGA Status of the Aurora Protocol Link between the VME FPGA and the ADC FPGAs (U11 and U21).

Bit	write	read
31		Prot_U21_error counter bit 7
24		Prot_U21_error counter bit 0
23	Clear Prot_U21_Frame_error_latch	Prot_U21_Frame_error_latch
22	Clear Prot_U21_Soft_error_latch	Prot_U21_Soft_error_latch
21	Clear Prot_U21_Hard_error_latch	Prot_U21_Hard_error_latch
20	no	Prot_U21_Lane_up_flag
19	no	Prot_U21_Channel_up_flag
18	no	Prot_U21_Frame_error_flag
17	no	Prot_U21_Soft_error_flag
16	no	Prot_U21_Hard_error_flag
15		Prot_U11_error counter bit 7
8		Prot_U11_error counter bit 0
7	Clear Prot_U11_Frame_error_latch	Prot_U11_Frame_error_latch
6	Clear Prot_U11_Soft_error_latch	Prot_U11_Soft_error_latch
5	Clear Prot_U11_Hard_error_latch	Prot_U11_Hard_error_latch
4	no	Prot_U11_Lane_up_flag
3	no	Prot_U11_Channel_up_flag
2	no	Prot_U11_Frame_error_flag
1	no	Prot_U11_Soft_error_flag
0	no	Prot_U11_Hard_error_flag

4.13 Aurora Data Status register (0xD4, read/write)

```
#define SIS3305_VME_FPGA_AURORA_DATA_STATUS    0xD4   /* read/write; D32 */
```

This register holds the VME FPGA Status of the Aurora Data Link between the VME FPGA and the ADC FPGAs (U11 and U21).

Bit	write	read
31		Data_U21_Lane_up_flag (1)
30		Data_U21_Lane_up_flag (0)
29		Data_U21_Tx_Lock_flag
28		Data_U21_error counter bit 7 to 4 (or)
27		Data_U21_error counter bit 3
24		Data_U21_error counter bit 0
23	Clear Prot_U21_Frame_error_latch	Data_U21_Frame_error_latch
22	Clear Prot_U21_Soft_error_latch	Data_U21_Soft_error_latch
21	Clear Prot_U21_Hard_error_latch	Data_U21_Hard_error_latch
20	no	Data_U21_Lane_up_flag (both)
19	no	Data_U21_Channel_up_flag
18	no	Data_U21_Frame_error_flag
17	no	Data_U21_Soft_error_flag
16	no	Data_U21_Hard_error_flag
15		Data_U11_Lane_up_flag (1)
14		Data_U11_Lane_up_flag (0)
13		Data_U11_Tx_Lock_flag
12		Data_U11_error counter bit 7 to 4 (or)
11		Data_U11_error counter bit 3
8		Data_U11_error counter bit 0
7	Clear Prot_U11_Frame_error_latch	Data_U11_Frame_error_latch
6	Clear Prot_U11_Soft_error_latch	Data_U11_Soft_error_latch
5	Clear Prot_U11_Hard_error_latch	Data_U11_Hard_error_latch
4	no	Data_U11_Lane_up_flag (both)
3	no	Data_U11_Channel_up_flag
2	no	Data_U11_Frame_error_flag
1	no	Data_U11_Soft_error_flag
0	no	Data_U11_Hard_error_flag

Note: Data_Ux1_Lane_up_flag (1) = Data_Ux1_Lane_up_flag (0)

4.14 Key addresses (0x400 – 0x43C write only)

Write access (with Broadcast functionality) to a key address (KA) with arbitrary data invokes a respective action.

4.14.1 Key address general reset (0x400 write only)

```
#define SIS3305_KEY_RESET                0x400   /* write only; D32 */
```

A write with arbitrary data to this register (key address) resets the SIS3305 to it's power up state.

4.14.2 Key address Arm sample logic (0x410 write only)

```
#define SIS3305_KEY_ARM                  0x410   /* write only; D32 */
```

A write with arbitrary data to this register (key address) will arm the sample logic.

4.14.3 Key address Disarm sampe logic (0x414 write only)

```
#define SIS3305_KEY_DISARM               0x414   /* write only; D32 */
```

A write with arbitrary data to this register (key address) will disarm the sample logic.

4.14.4 Key address Trigger

```
#define SIS3305_KEY_TRIGGER              0x418   /* write only; D32 */
```

A write with arbitrary data to this register (key address) will generate a trigger.

4.14.5 Key address Enable sample logic

```
#define SIS3305_KEY_ENABLE               0x41C   /* write only; D32 */
```

A write with arbitrary data to this register (key address) will enable the sample logic.

4.14.6 Key address Set Veto

```
#define SIS3305_KEY_SET_VETO             0x420   /* write only; D32 */
```

A write with arbitrary data to this register (key address) will set the Veto function.

4.14.7 Key address Clear Veto

```
#define SIS3305_KEY_CLR_VETO             0x424   /* write only; D32 */
```

A write with arbitrary data to this register (key address) will clear the Veto function.

4.14.8 Key address ADC Clock Synchronization

```
#define SIS3305_ADC_SYNCH_PULSE                 0x430  /* write only; D32 */
```

A write with arbitrary data to this register (key address) makes the ADC out clock signals go low and resets the ISERDES Logic in the FPGA for the ADC data.
The ADC out clock signals restart after TDR + pipeline delay + a certain number of input clock cycles which is programmed via the SPI in the SYNCH register.
This command is necessary to synchronize the four ADC channels within the ADC chips.

4.14.9 Key address Reset ADC-FPGA-Logic

```
#define SIS3305_ADC_FPGA_RESET                  0x434  /* write only; D32 */
```

A write with arbitrary data to this register (key address) reset the ADC-FPGA logic (including the DDR2-memory controller). Used for test purposes only.

4.14.10 Key address Trigger Out Pulse

```
#define SIS3305_ADCEXTERNAL_TRIGGER_OUT_PULSE  0x43C  /* write only; D32 */
```

A write with arbitrary data to this register (key address) generates a pulse on the External Trigger Out (if enabled, see LEMO Trigger Out Select register bit 15).

4.15 Event configuration registers(0x2000, 0x3000 read/write)

```
#define SIS3305_EVENT_CONFIG_ADC1_4                    0x2000
#define SIS3305_EVENT_CONFIG_ADC5_8                    0x3000
```

This register is implemented for each channel group.

Bit	Function
31	ADC Event Header programmable ID bit 7
…	…
…	…
24	ADC Event Header programmable ID bit 0
23	ADC Event Header programmable Info bit 3
...	...
20	ADC Event Header programmable Info bit 0
19	Unused; read 0
18	Enable “Direct Memory Stop Arm for Trigger after PreTriggerDelay” bit
17	Unused; (Enable “Direct Memory TDC Measurement” bit)
16	Disable “Direct Memory Header” bit
15	ADC Memory Write via VME Test Enable
14	Unused; read 0
13	Unused; read 0
12	Gray code enable
11	Unused; read 0
10	Disable Timestamp Clear
9	Enable “Timestamp Clear with Sample Enable” bit
8	Enable “ADC Event sampling with next external Trigger” (TDC) (else with “Enable”)
7	Unused; read 0
6	Enable internal Trigger/Gate (asynchronous Mode)
5	Enable global Trigger/Gate (synchronous Mode)
4	ADC Gate Mode (else Trigger Mode)
3	Unused; read 0
2	ADC Event Saving Mode bit 2
1	ADC Event Saving Mode bit 1
0	ADC Event Saving Mode bit 0

The 8-bit ADC Event Header programmable ID is used to program an Event Header ID.
The example software writes a part of the selected SIS3305 VME base address and the ADC group number to this register.

Bits	7-1	0
assignement	VME Base Address bits 30 – 24	0 : ADC chip 1 (channel 1-4) 1 : ADC chip 2 (channel 5-8)

The 4-bit ADC Event Header programmable information is used to add additional information to the ADC event header.
The Struck example software writes the selected ADC chip channel mode to this register.

ADC Event Header programmable information	ADC chip channel mode (software defined)
0	4-channel (4 x 1.25Gsps)
1	2-channel (2 x 2.5Gsps)
2	1-channel (1 x 5Gsps)
3	reserved

“Enable Direct Memory Stop Arm for Trigger after PreTriggerDelay” bit

Enable Direct Memory Stop Arm for Trigger after PreDelay bit	
0	Arms the logic for an external trigger immediately after the sampling is started in Event Direct Memory Stop (Wrap) Mode
1	Arms the logic for an external trigger after the sampling is started and “PreTrigger” samples are stored in Event Direct Memory Stop (Wrap) Mode

“Disable Direct Memory Header “ bit

Disable Direct Memory Header bit	
0	Direct Memory Event Data Buffer has a Header
1	Direct Memory Event Data Buffer has no Header

“Disable Timestamp Clear” bit

Disable Timestamp Clear bit	Timestamp Clear with
0	Enable Timestamp clear function (see “Timestamp Clear with Sample Enable” bit)
1	Disable Timestamp clear function

“Timestamp Clear with Sample Enable” bit

Timestamp Clear with Sample Enable bit	Timestamp Clear with
0	Sample Enabled and first TDC Event (external Trigger)
1	Sample Enabled

"ADC Event sampling with next external Trigger"

ADC Event sampling with next external Trigger bit	ADC Event sampling with
0	Ready for ADC Events after Sample Enabled
1	Ready for ADC Events after Sample Enabled and first TDC Event (external Trigger)

"Enable internal Trigger/Gate (asynchronous Mode)"

Enable internal Trigger/Gate bit	
0	No internal individual trigger /gate
1	internal individual trigger/gate

"Enable global Trigger/Gate (synchronous Mode)"

Enable global Trigger/Gate bit	
0	No global trigger
1	global trigger, all channels are trigger with global trigger/gate: external trigger (if enabled) or KeyTrigger

ADC Event Saving Modes

ADC Event Saving Mode bits	ADC Event building
0	4-channel **Event FIFO Mode**: Save ADC values of 4 channels in one Data Block - asynchronous Mode 1 x 5Gsps - synchronous Mode 5Gsps / 2.5Gsps / 1.25Gsps
1	2-channel **Event FIFO Mode**: Save ADC values of 2 channels in one Data Block - asynchronous Mode 2 x 2.5Gsps
2 - 3	reserved
4	1-channel **Event FIFO Mode**: Save ADC values of 1 channel in one Data Block - asynchronous Mode 4 x 1.25Gsps
5	reserved
6	4-channel **Event Direct Memory Start Mode** - synchronous Mode 5Gsps / 2.5Gsps / 1.25Gsps
7	4-channel **Event Direct Memory Stop (Wrap) Mode** - synchronous Mode 5Gsps / 2.5Gsps / 1.25Gsps

synchronous Mode: external trigger/gate, all channels record data at the same time
asynchronous Mode: internal trigger/gate, each channel (group) records data individually

4.16 Sample Memory Start Address registers (0x2004, 0x3004)

```
#define SIS3305_SAMPLE_START_ADDRESS_ADC1_4                0x2004
#define SIS3305_SAMPLE_START_ADDRESS_ADC5_8                0x3004
```

These registers define the memory start address.
The value is given in 512-bit blocks (16 32-bit words) .

Bit	31-24	23-0
Function	reserved	Sample Memory Start Address (512-bit blocks) (32-bit word address x 16)

The power up default value is 0

Explanation (sample memory start address)
The contents of the **sample memory start address** register is assigned as memory data storage address with the arm command (key address arm sample logic) or with the enable command (key address enable sample logic).

4.17 Sample/Extended Block Length registers (0x2008, 0x3008)

```
#define SIS3305_SAMPLE_LENGTH_ADC1_4                    0x2008
#define SIS3305_SAMPLE_LENGTH_ADC5_8                    0x3008
```

This register set defines the number of sample blocks of each ADC Event or the number of extended sample blocks depending on the Trigger/Gate mode.

The size of one sample block for each ADC channel is 128-bit (i.e. 4 x 32-bit word, 12 samples).

The maximum number of "Sample/Extended Block Length" depends on the "ADC Event Saving Mode".

Valid for "ADC Event Saving Modes" 0, 1 and 4 (Event FIFO Mode):

Bit	31-8	7-0
Function	reserved	Sample/Extended Block Length

default after Reset: 0x0

Note: the maximum ADC Event size for one ADC channel is 3072 samples !
The logic stops the ADC event sampling after 3072 samples in gate mode!

Valid for "ADC Event Saving Modes" 6 and 7 (Event Direct Memory Mode):

Bit	31-24	23-0
Function	reserved	Sample/Extended Block Length

default after Reset: 0x0

Sample/Extended Block Length	Number of 128-bit blocks	Number of samples		
		1.25 Gsps	2.5 Gsps	5 Gsps
0x0	1	12	24	48
0x1	2	24	48	96
..	..	..	..	..
N	N+1	(N+1) x 12	(N+1) x 24	(N+1) x 48
..	..	..	..	..
0xff	**256**	**3072**	**6144**	**12288**

Valid for "ADC Event Saving Modes" 6 and 7 (Direct Memory Mode):

..	..	..	..	..
0xff ffff	**16.777.216**	**201.326.592**	**402.653.184**	**805.306.368**

4.18 Direct Memory Stop Pretrigger Block Length registers (0x200C, 0x300C)

```
#define SIS3305_SAMPLE_PRE_TRIGGER_LENGTH_ADC1_4          0x200C
#define SIS3305_SAMPLE_PRE_TRIGGER_LENGTH_ADC5_8          0x300C
```

These registers define the pretrigger number of sample blocks of each Event in Direct Memory Stop (Wrap) Mode (”ADC Event Saving Mode” 7) .

The size of one sample block for each ADC channel is 128-bit (4 x 32-bit word, 12 samples).

Valid for ”ADC Event Saving Mode” 7 (Direct Memory Stop (Wrap) Mode):

Bit	31-24	23-0
Function	reserved	Sample Pretrigger Block Length

default after Reset: 0x0

4.19 Ringbuffer Pretrigger Delay register

```
#define SIS3305_RINGBUFFER_PRE_DELAY_ADC12                0x2010
#define SIS3305_RINGBUFFER_PRE_DELAY_ADC34                0x2014
#define SIS3305_RINGBUFFER_PRE_DELAY_ADC56                0x3010
#define SIS3305_RINGBUFFER_PRE_DELAY_ADC78                0x3014
```

These registers define the number of pre trigger delay for each channel !
The maximum Ringbuffer pretrigger delay value is 1023.

Bit	31-26	25-16	15-10	9-0
Function	reserved	ADC 1/3/5/7 Pretrigger Delay value	reserved	ADC 2/4/6/8 Pretrigger Delay value

Ringbuffer Pretrigger Delay value	Number of delayed samples		
	1.25 Gsps	2.5 Gsps	5 Gsps
0x0	0	0	0
0x1	6	12	24
..	..	..	..
N	N x 6	N x 12	N x 24
..	..	..	..
0x3ff	1023 x 6 = 6138	1023 x 12 = 12276	1023 x 24 = 24552

4.20 Direct Memory Max Nof Events registers (0x2018, 0x3018)

```
#define SIS3305_MAX_NOF_EVENTS_ADC1_4                     0x2018
```

```
#define SIS3305_MAX_NOF_EVENTS_ADC5_8                0x3018
```

The Sample Logic stops as soon as the Event counter reaches the value of the Direct_Memory_Max_Nof_Events register in Event Direct Memory Mode.
The Event sample logic runs continuous with Max Nof Events = 0

Bit	31-16	15-0
Function	reserved	Max Nof Events

The power up default value is 0

4.21 End Address Threshold registers

```
#define SIS3305_END_ADDRESS_THRESHOLD_ADC1_4              0x201C
#define SIS3305_END_ADDRESS_THRESHOLD_ADC5_8              0x301C
```

These registers define the “End Address Threshold” values for each ADC channel group.

The value of the Actual Next Sample address counter will be compared with the value of the End Address Threshold register.
The value is given in 512-bit Blocks (i.e. 32-bit word address x 16)

Bit	31-24	23-0
Function	reserved	Sample Memory End Address Threshold (in 512-bit Blocks) (32-bit word address x 16)

The power up default value is 0

4.22 Trigger/Gate Threshold registers

```
#define SIS3305_TRIGGER_GATE_GT_THRESHOLDS_ADC1          0x2020
#define SIS3305_TRIGGER_GATE_LT_THRESHOLDS_ADC1          0x2024
#define SIS3305_TRIGGER_GATE_GT_THRESHOLDS_ADC2          0x2028
#define SIS3305_TRIGGER_GATE_LT_THRESHOLDS_ADC2          0x202C
#define SIS3305_TRIGGER_GATE_GT_THRESHOLDS_ADC3          0x2030
#define SIS3305_TRIGGER_GATE_LT_THRESHOLDS_ADC3          0x2034
#define SIS3305_TRIGGER_GATE_GT_THRESHOLDS_ADC4          0x2038
#define SIS3305_TRIGGER_GATE_LT_THRESHOLDS_ADC4          0x203C

#define SIS3305_TRIGGER_GATE_GT_THRESHOLDS_ADC5          0x3020
#define SIS3305_TRIGGER_GATE_LT_THRESHOLDS_ADC5          0x3024
#define SIS3305_TRIGGER_GATE_GT_THRESHOLDS_ADC6          0x3028
#define SIS3305_TRIGGER_GATE_LT_THRESHOLDS_ADC6          0x302C
#define SIS3305_TRIGGER_GATE_GT_THRESHOLDS_ADC7          0x3030
#define SIS3305_TRIGGER_GATE_LT_THRESHOLDS_ADC7          0x3034
#define SIS3305_TRIGGER_GATE_GT_THRESHOLDS_ADC8          0x3038
#define SIS3305_TRIGGER_GATE_LT_THRESHOLDS_ADC8          0x303C
```

4.22.1 Threshold Trigger/Gate GT

Bit	31	30-26	25-16	15-10	9-0
Function	GT Enable	None	Threshold value OFF	None	Threshold value ON

default after Reset: 0x0

A valid gate output is generated on the conditions:

- GT is set (GT):
  the Gate output signal will be set if the actual ADC value **goes** above the programmable threshold value ON **and** OFF and it is valid until the actual ADC value goes below the threshold value OFF .

4.22.2 Threshold Trigger/Gate LT

Bit	31	30-26	25-16	15-10	9-0
Function	LT Enable	None	Threshold value OFF	None	Threshold value ON

default after Reset: 0x0

A valid gate output is generated on the condition:

- LT is set (LT):
  the Gate output signal will be set if the actual ADC value **goes** below the programmable threshold value ON **and** OFF and it is valid until the actual ADC value goes above the threshold value OFF .

4.23 Sampling Status (0x2040, 0x3040)

```
#define SIS3305_SAMPLING_STATUS_REG_ADC1_4                0x2040
#define SIS3305_SAMPLING_STATUS_REG_ADC5_8                0x3040
```

This register holds the sampling status and an event builder FSM (Finite State Machine) error counter. The Finite State Machine (FSM) error counter is reserved for internal use.

Bit	
31	reserved
...	
24	reserved
23	Event Builder FSM Mode-Error Counter bit 7
...	
16	Event Builder FSM Mode-Error Counter bit 0
15	reserved
..	
6	Direct Memory Wrap Flag
5	Direct Memory Stopped Flag
4	Direct Memory Busy Flag
3	0 (reserved)
2	0 (reserved)
1	End Address Flag
0	Sampling Enable (BUSY)

4.24 Actual Sample address register

```
#define SIS3305_ACTUAL_SAMPLE_ADDRESS_ADC1_4                0x2044
#define SIS3305_ACTUAL_SAMPLE_ADDRESS_ADC5_8                0x3044
```

These two read only registers hold the actual sampling address for the given ADC channel group.
The value is given in 512-bit Blocks (32-bit word address x 16).

Bit	31-24	23-0
Function	reserved	Actual Sample Memory Address (in 512-bit Blocks) (32-bit word address x 16)

4.25 Direct Memory Event Counter

```
#define SIS3305_DIRECT_MEMORY_EVENT_COUNTER_ADC1_4          0x2048
#define SIS3305_DIRECT_MEMORY_EVENT_COUNTER_ADC5_8          0x3048
```

These two read only registers hold the actual number of events in Direct Memory mode for the given ADC channel group.
The Event Counter will be cleared with “Sample enable” and will be incremented with each saved Event.

Bit	31-16	15-0
Function	reserved	Event Counter

4.26 Direct Memory Actual Next Event Start address register

```
#define SIS3305_DIRECT_MEMORY_ACTUAL_EVENT_START_ADDRESS_ADC1_4     0x204C
#define SIS3305_DIRECT_MEMORY_ACTUAL_EVENT_START_ADDRESS_ADC5_8     0x304C
```

These two read only registers hold the actual Next Event Start address in Direct Memory mode for the given ADC channel group.

The value is given in 512-bit Blocks (32-bit word address x 16).

Bit	31-24	23-0
Function	reserved	Actual Next Event Start Memory Address (in 512-bit Blocks) (32-bit word address x 16)

4.27 Actual Sample Value registers

```
#define SIS3305_ACTUAL_SAMPLE_VALUE_ADC12          0x2050 /* read */
#define SIS3305_ACTUAL_SAMPLE_VALUE_ADC34          0x2054 /* read */
#define SIS3305_ACTUAL_SAMPLE_VALUE_ADC56          0x3050 /* read */
#define SIS3305_ACTUAL_SAMPLE_VALUE_ADC78          0x3054 /* read */
```

Read “on the fly” of the actual converted ADC values.
The read only registers are updated with every ADC clock, unless a concurrent VME read access is pending.
The register contents is refreshed and can be read any time (i.e. they are updated independent of the unarmed, armed, sampling state) as long as a sampling clock is distributed on the ADC board (internal clock or active/clocking external clock)

Bit	31-26	25-16	15-10	9-0
Function	0	ADC 1/3/5/7 10-bit data	0	ADC 2/4/6/8 10-bit data

4.28 Aurora Protocol/Data Status register (0x2058,0x3058 read/write)

```
#define SIS3305_FPGA_AURORA_STATUS_ADC1_4       0x2058 /* read/write; D32 */
#define SIS3305_FPGA_AURORA_STATUS_ADC5_8       0x3058 /* read/write; D32 */

#define SIS3305_FPGA_AURORA_STATUS_KEY_CLEAR_ADC1_4  0x200C  /* wr; D32 */
#define SIS3305_FPGA_AURORA_STATUS_KEY_CLEAR_ADC5_8  0x300C  /* wr; D32 */
```

These registers hold the ADC FPGA Status of the Aurora Protocol and Data Links between the ADC FPGAs (U11 and U21) and the VME FPGA.

Note: Clear Error_Latch bits
With version 1006 and lower: write to addr. = 0x200c/0x300c
With version 1007 and higher: write to addr. = 0x2058/0x3058 with datum = 0x5555aaaa;

Bit	read
31	0
26	Data_Frame_Error_Latch bit
25	Data_Soft_ Error_Latch bit
24	Data_Hard_ Error_Latch bit
23	0
22	Data_gt_clk_locked
21	Data_Lane_up_flag(1)
20	Data_Lane_up_flag(1)
19	Data_Channel_up_flag
18	Data_Frame_error_flag
17	Data_Soft_error_flag
16	Data_Hard_error_flag
15	0
10	Prot_Frame_ Error_Latch bit
9	Prot_Soft_ Error_Latch bit
8	Prot_Hard_ Error_Latch bit
7	0
6	Prot_gt_clk_locked
5	0
4	Prot_ Lane_up_flag
3	Prot_Channel_up_flag
2	Prot_Frame_error_flag
1	Prot_Soft_error_flag
0	Prot_Hard_error_flag

Note: After power up and the links locked the reading will be 0x03780358, after a clear error latch bit cycle the reading should be 0x00780058

4.29 Individual Channel Select/Set Veto register (0x2070,0x3070 read/write)

```
#define SIS3305_INDIVIDUAL_SELECT_SET_VETO_ADC1_4     0x2070 /* rd/wr D32 */
#define SIS3305_INDIVIDUAL_SELECT_SET_VETO_ADC5_8     0x3070 /* rd/wr D32 */
```

These two registers are used to include/exclude channels from the external veto and to veto channels directly. Refer to the illustration in section 5.4 also.

Bit	read
31	reserved
16	reserved
15	reserved
10	reserved
9	reserved
8	Select Veto TDC Event
7	Select Veto ADC Channel 4/8
6	Select Veto ADC Channel 3/7
5	Select Veto ADC Channel 2/6
4	Select Veto ADC Channel 1/5
3	Set Veto ADC Channel 4/8
2	Set Veto ADC Channel 3/7
1	Set Veto ADC Channel 2/6
0	Set Veto ADC Channel 1/5

Note: the power up value is 0x0

4.30 ADC Input tap delay registers (0x2400, 0x3400)

```
#define SIS3305_ADC_INPUT_TAP_DELAY_ADC1_4                0x2400
#define SIS3305_ADC_INPUT_TAP_DELAY_ADC5_8                0x3400
```

The input tap delay registers are used to adjust the ADC - FPGA data strobe timing.

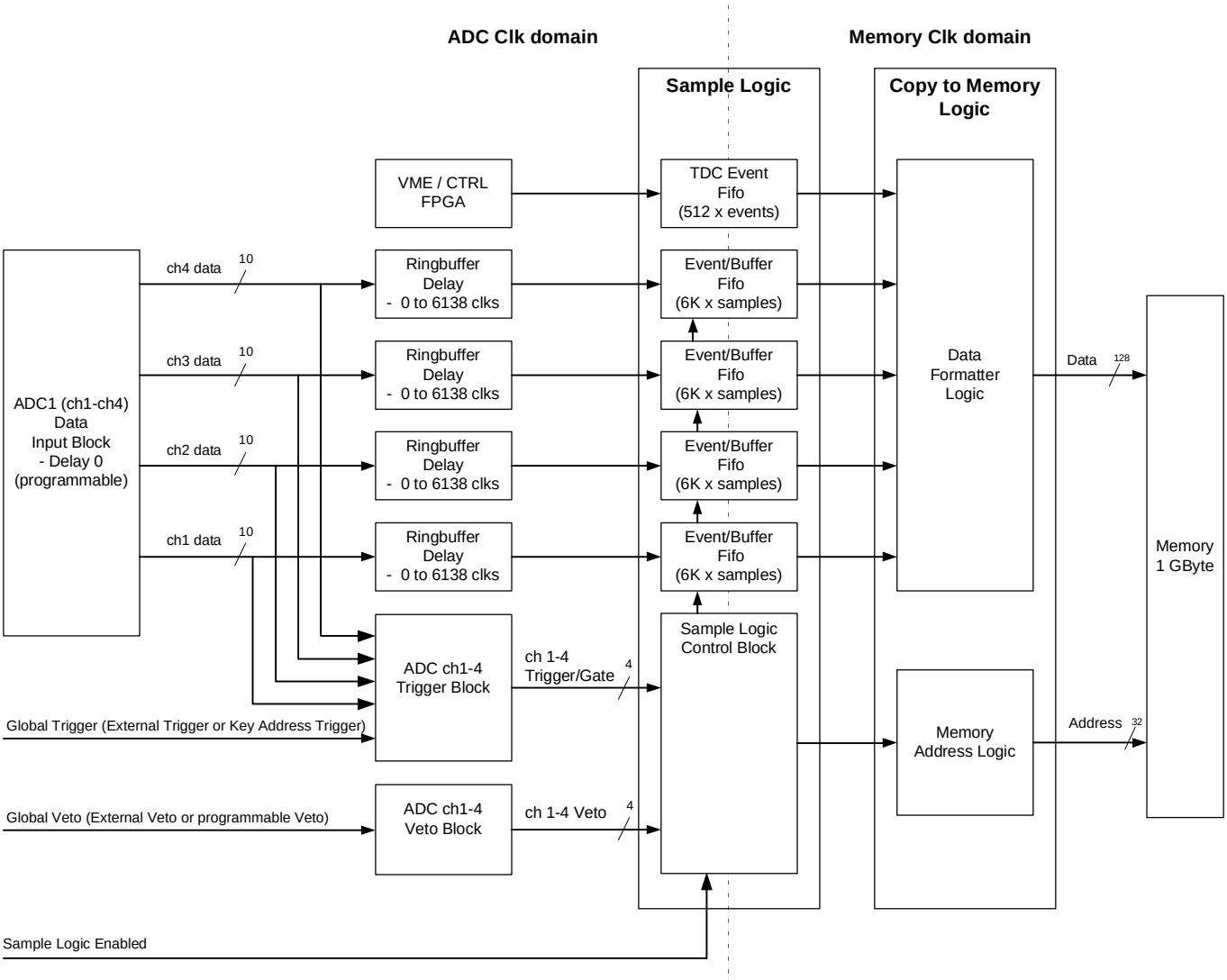
Bit	31-11	11	10	9	8	7-6	5-0
Function	None	ADC 4 Select	ADC 3 Select	ADC 2 Select	ADC 1 Select	None	Tap delay value (x 78ps)

Note: The tap delays can be retrieved fom the 93C56 EEprom and have to be written to the two input tap delay registers prior to acquisition of data

5 Aspects of Operation

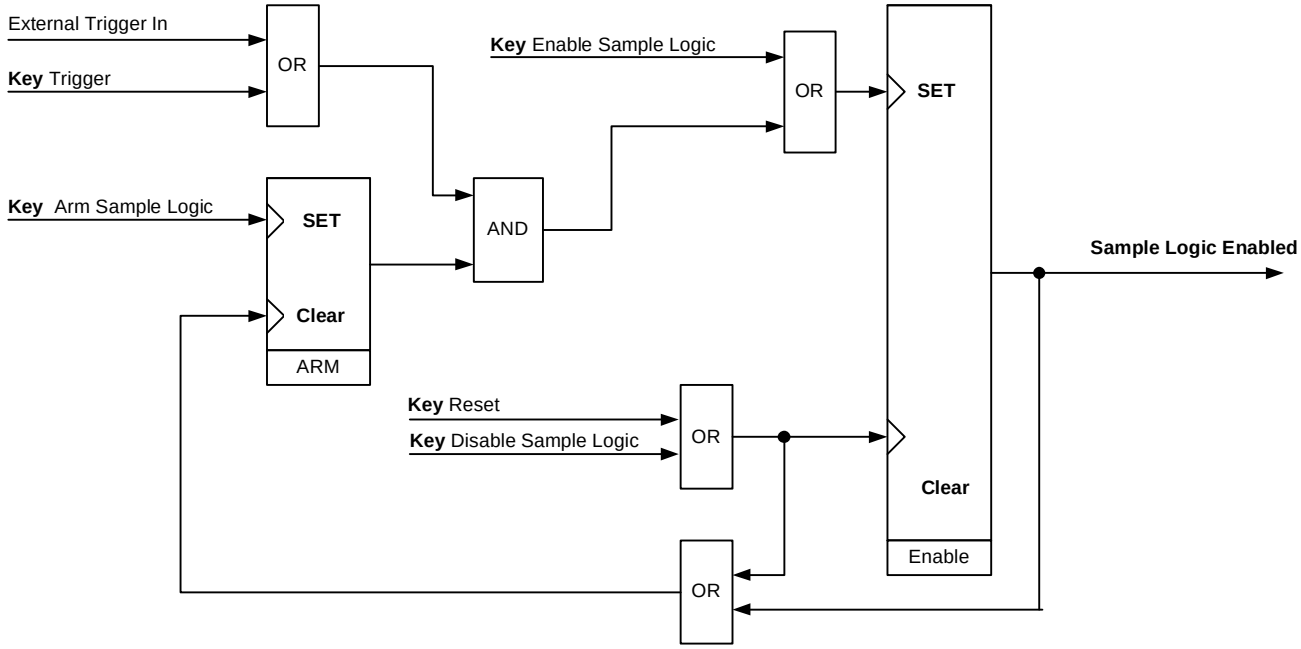
5.1 General block diagram of one ADC (channel 1-4)

The schematic of the ADC (channel 1-4) data flow and sample sample logic is shown below.



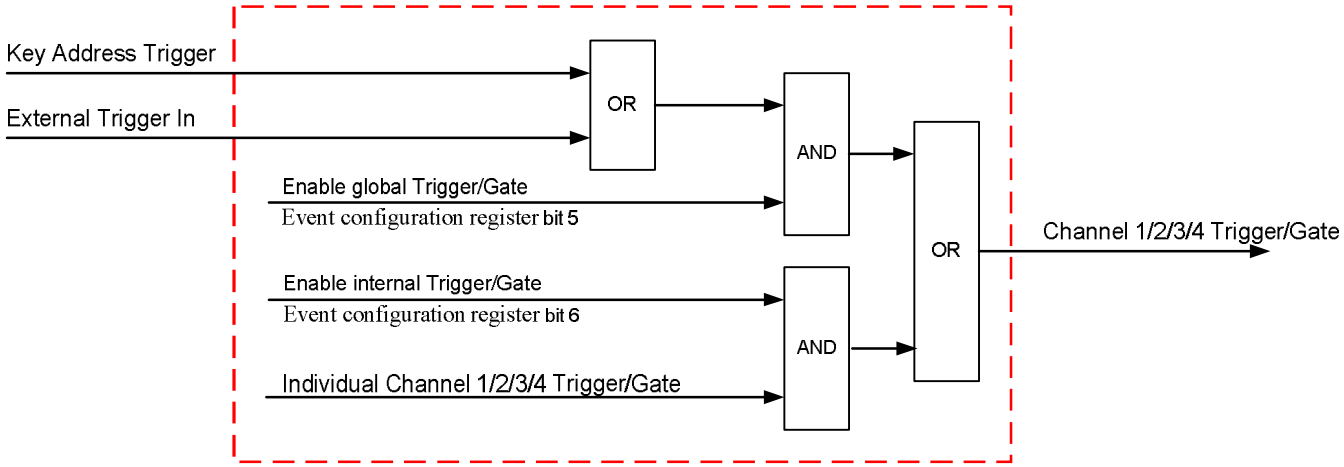
5.2 Enable Sample Logic

The schematic of the sample logic is shown below.



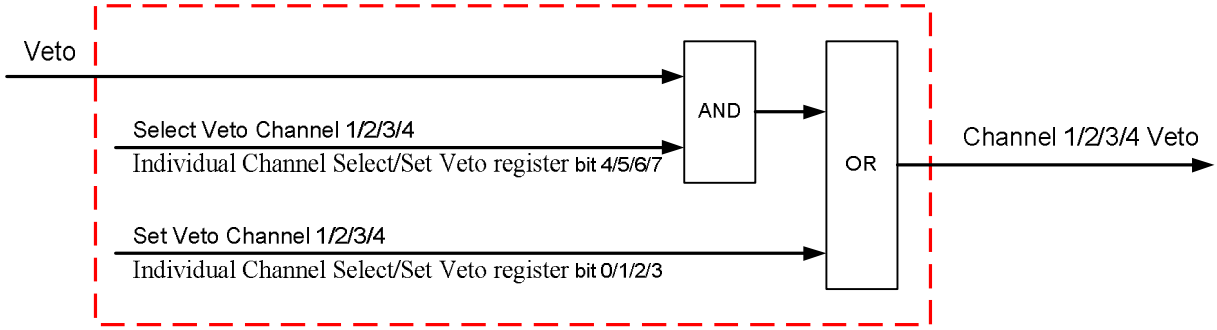
5.3 Triggering

The schematic of the trigger logic of the ADC1 (channel 1-4) is shown below.

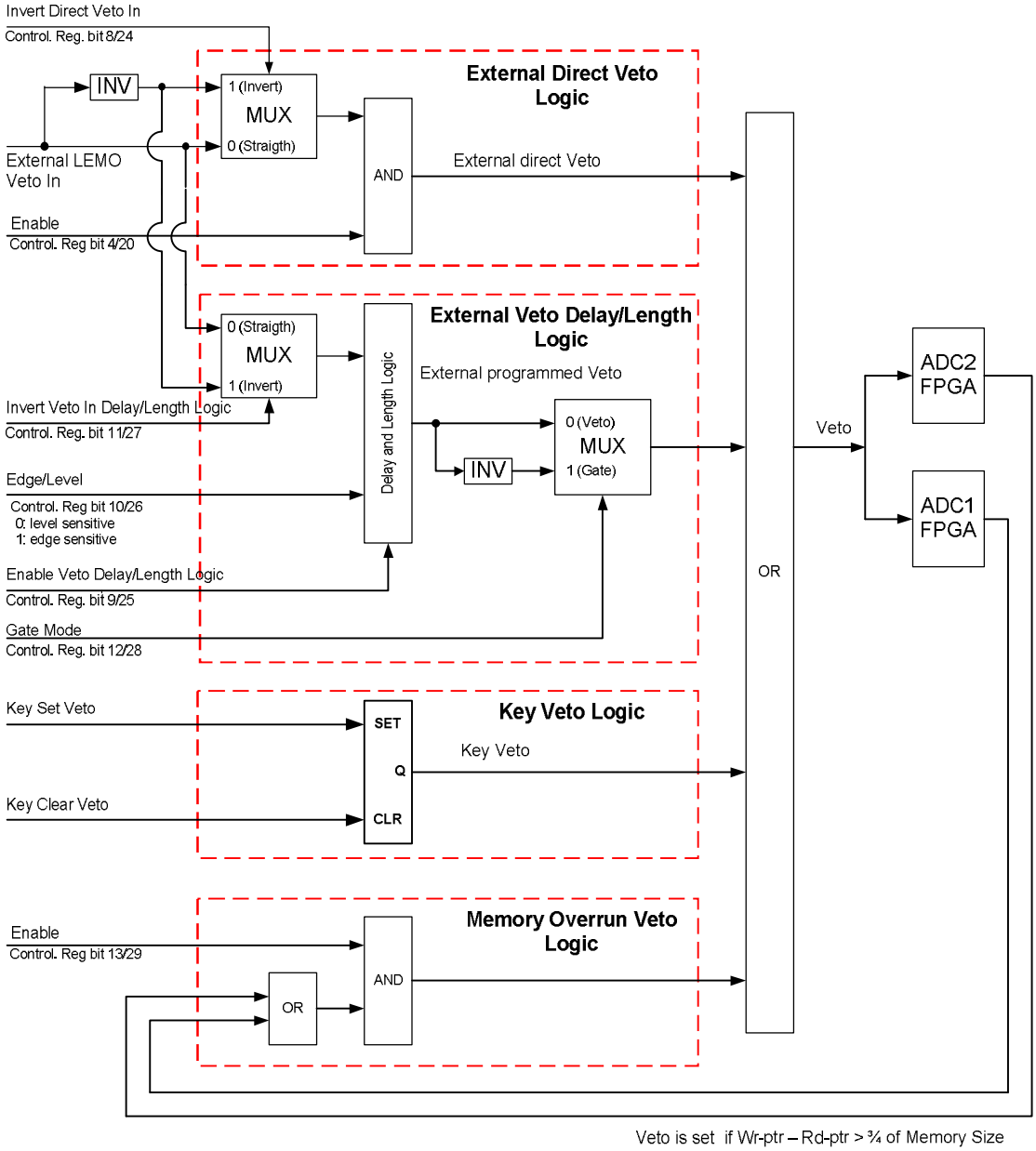


5.4 Veto

The schematic of the Veto logic of the ADC1 (channel 1-4) is shown below.

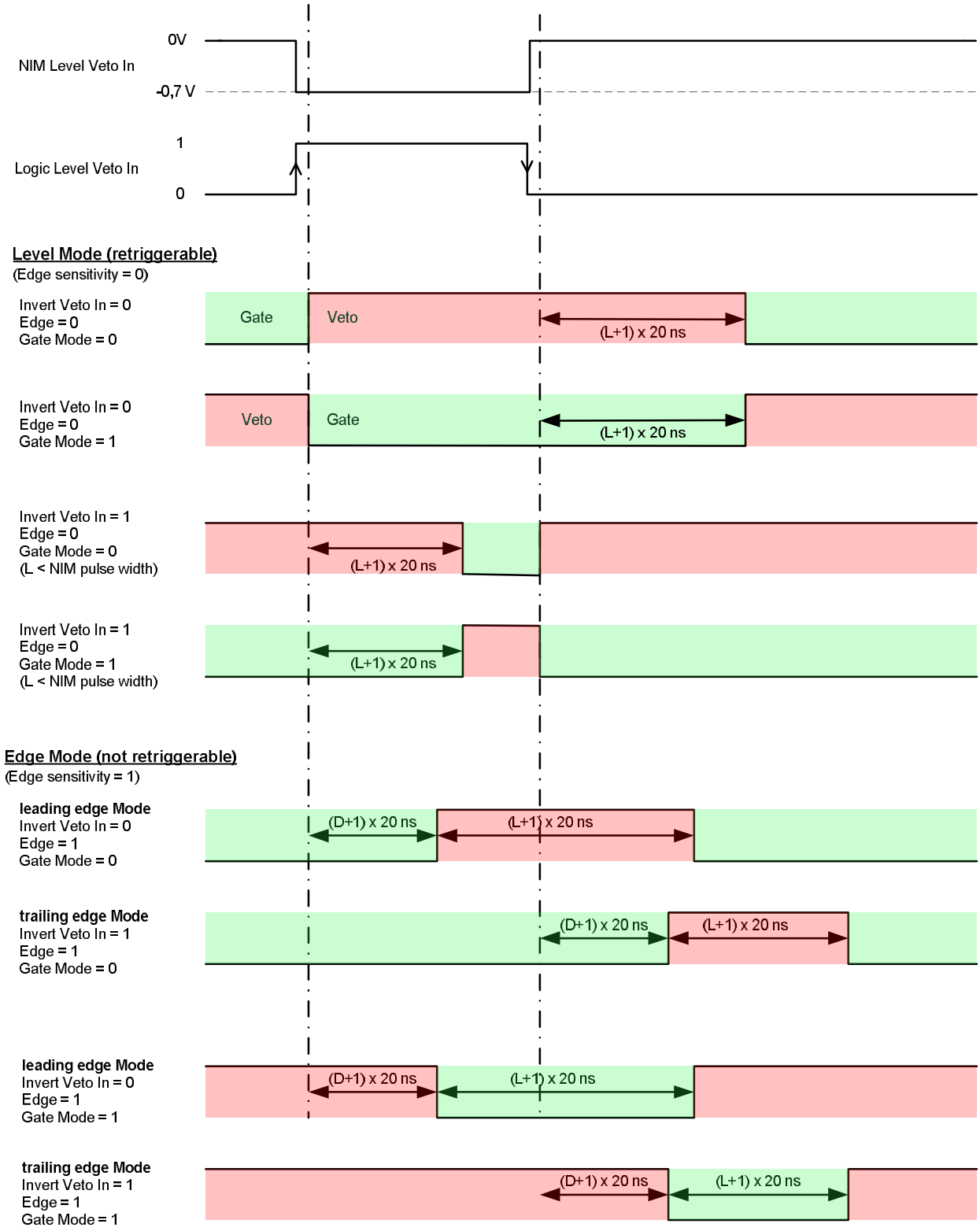


The schematic of the global veto logic is shown below.



5.4.1 External Veto Delay/Length Logic

The effect of the Invert (bits 22/27), Edge sensitivity (bits 10/26) and Gate mode (bits 12/28) control bits is illustrated below.



5.4.2 Memory Overrun Veto Logic

The Memory Overrun Veto Flag will be set if the Write Pointer (Sample Address) – the Read Pointer is greater than ¾ of the Memory size.

5.5 Event Saving Modes

Different Event Saving Modes are implemented to save Events:

- Event FIFO Mode
- Event Direct Memory Start Mode
- Event Direct Memory Stop Mode

Note: refer to the example code in sis3305_adc_tests.c, where you can find the full setup in the routines:

```
int RunTest_SIS3305_Test_Event_Aquisition (void)  ;
int RunTest_SIS3305_Test_Direct_Memory_Start_Mode_Aquisition (void)  ;
int RunTest_SIS3305_Test_Direct_Memory_Stop_Mode_Aquisition (void)  ;
```

5.5.1 Event FIFO Mode

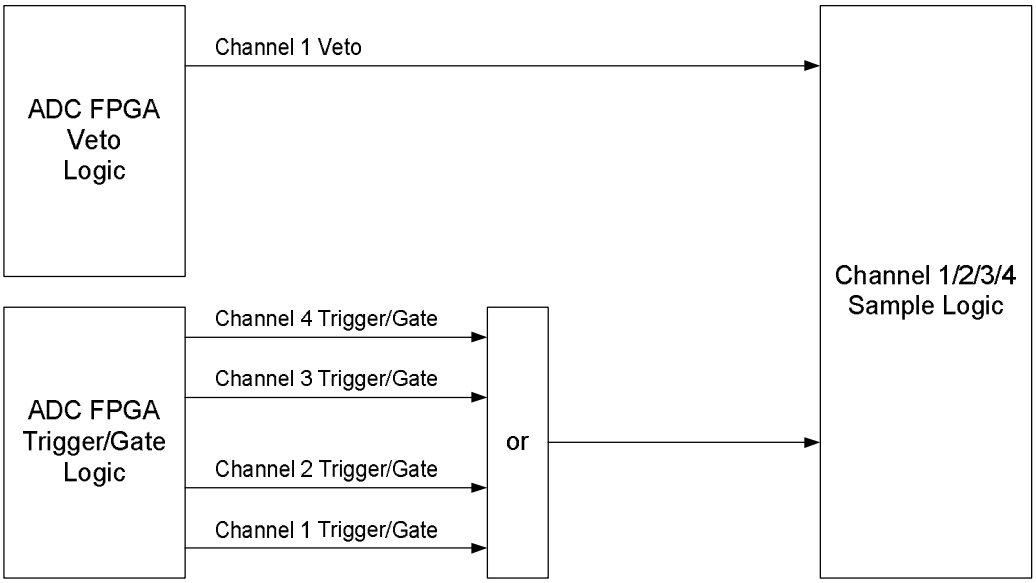
The Event FIFO Mode is implemented for events with a maximum size of 3072 samples for each channel.

Three Event FIFO Modes are implemented:

- 4-channel Event FIFO Mode (asynchronous mode 5 Gsps or synchronous mode 5Gsps / 2.5Gsps / 1.25Gsps)
- 2-channel Event FIFO Mode (synchronous Mode 2.5Gsps)
- 1-channel Event FIFO Mode (synchronous Mode 1.25Gsps)

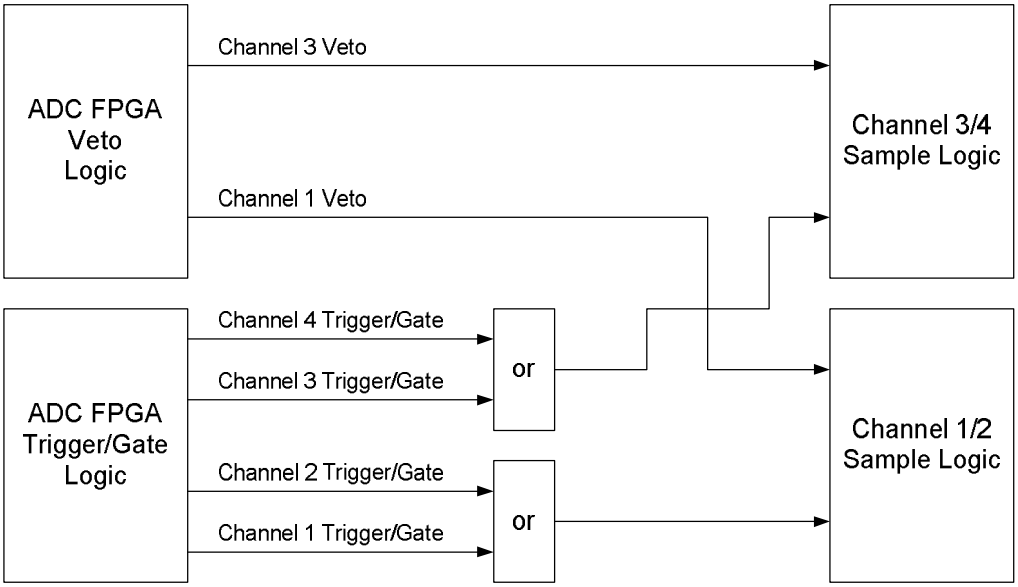
5.5.1.1 4-channel Event FIFO Mode

In 4-channel Event FIFO Mode the logic saves the ADC values of 4 channels in one Data Block.
This mode is used to save 5Gsps Events which are triggered externally (global trigger, synchronous) or triggered internally (“or” of channel 1 to 4 triggers, asynchronous).
This mode is also used to save 1.25Gsps/2.5Gsps Events which are triggered externally (global trigger, synchronous).



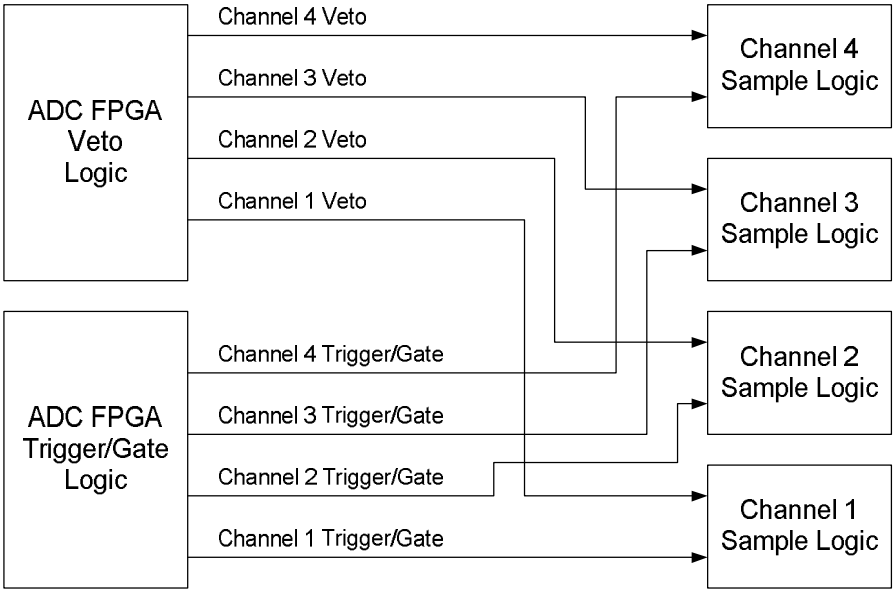
5.5.1.2 2-channel Event FIFO Mode

In 2-channel Event FIFO Mode the logic saves the ADC values of 2 channels in one Data Block.
This mode is used to save 2.5Gsps Events which are triggered internally (“or” of channel 1 to 2 triggers and “or” of channel 3 to 4 triggers) .



5.5.1.3 1-channel Event FIFO Mode

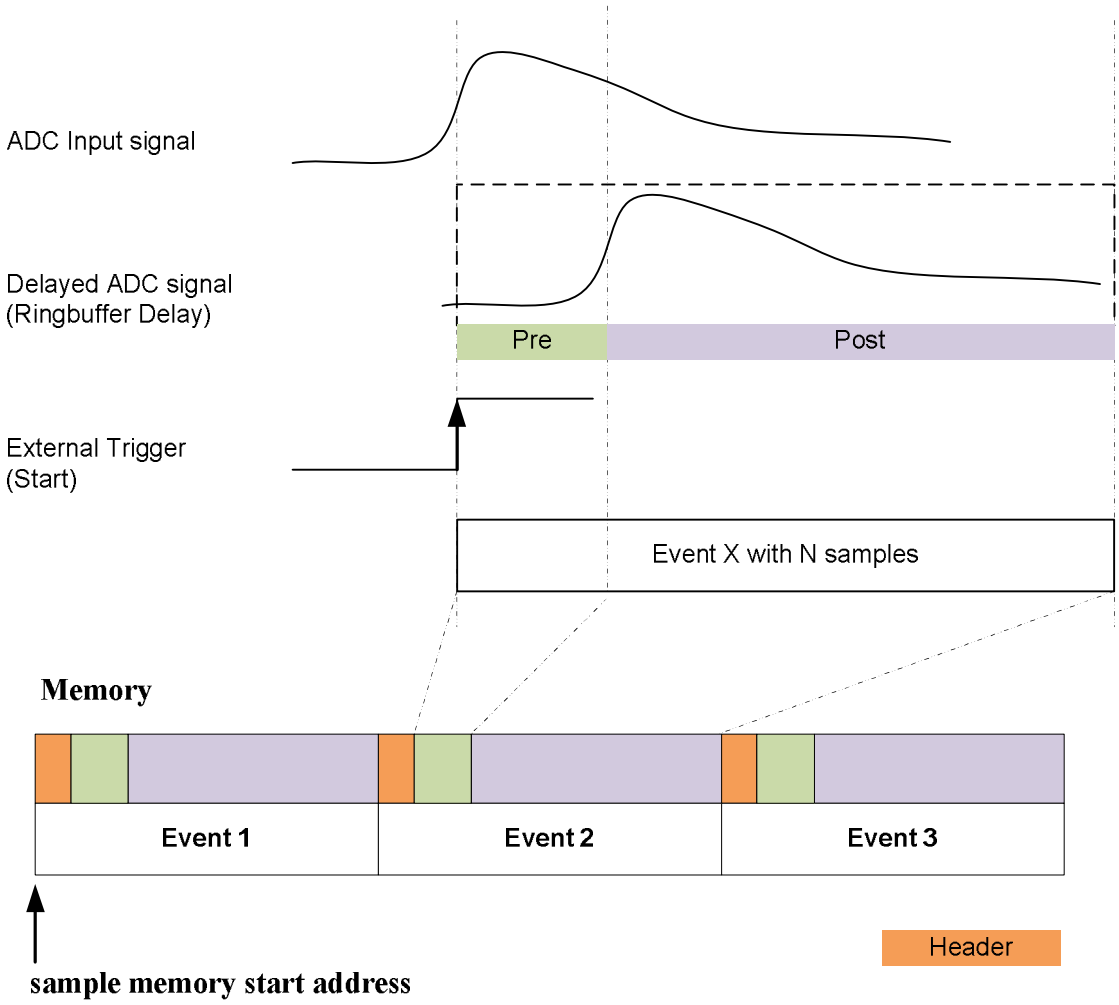
In 1-channel Event FIFO Mode the logic saves the ADC values of 1 channels in one Data Block.
This mode is used to save 1.25Gsps Events which are triggered internally (channel 1 trigger, … , channel 4 trigger) .



5.5.2 4-channel Event Direct Memory Start Mode

The logic saves the ADC values of 4 channels to memory in one data block with a header in 4-channel Event Direct Memory Start Mode.
An external trigger starts the sampling and the logic writes N samples to the Memory with an information header If the sample logic is enabled. In Multi Event Mode, the logic is ready for a new trigger after the event is written.

- programmable Event Length up to
  - 4 x 201.326.592 (1.25Gsps)
  - 2 x 402.653.184 (2.5Gsps)
  - 1 x 805.306.368 (5Gsps)
- programmable Number of Events (Multi Event)
- programmable Ringbuffer Delay for the ADC data (6 to 6138 for each channel)

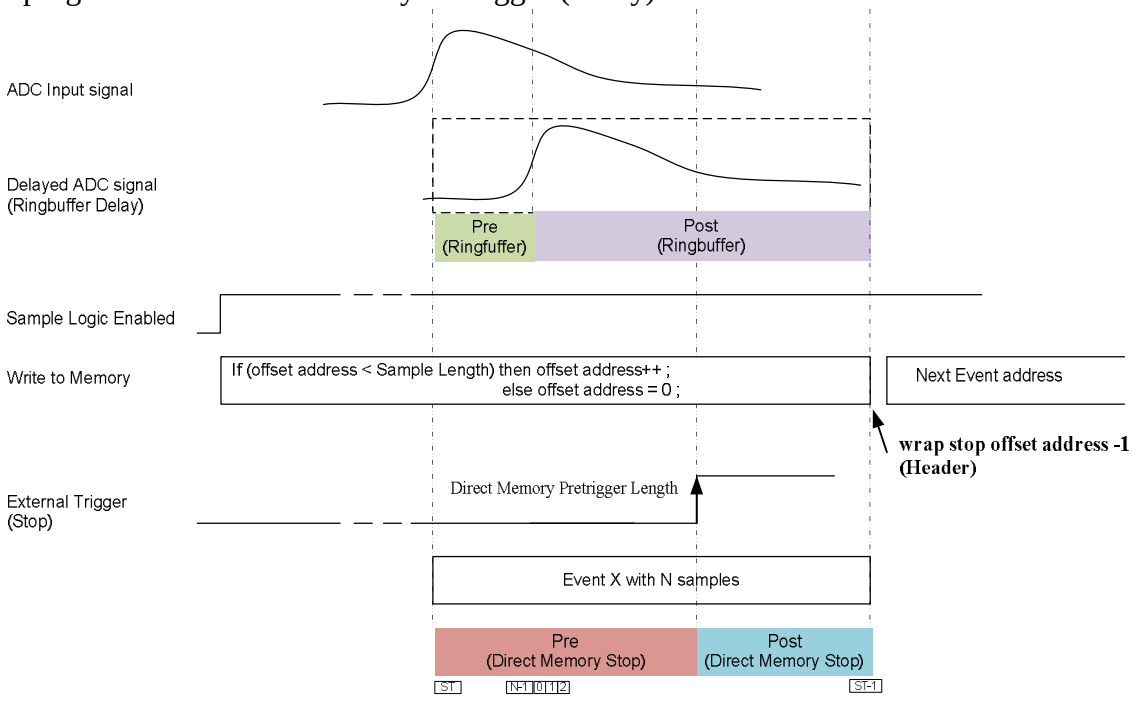


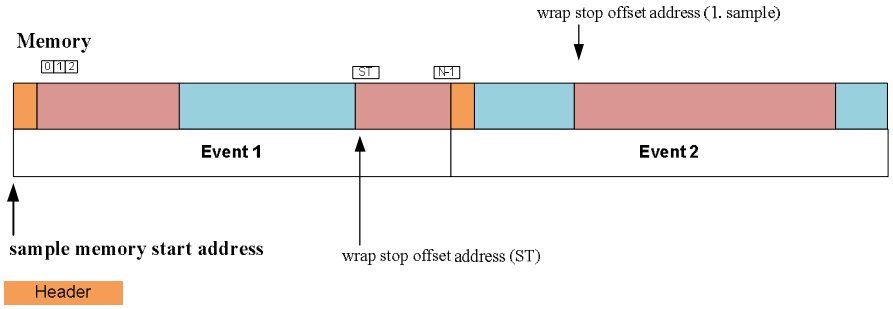
5.5.3 4-channel Event Direct Memory Stop Mode

The logic saves the ADC values of 4 channels to memory in one data block with a header in 4-channel Event Direct Memory Stop Mode.
The sampling of the ADC data starts immediately with “sample logic is enabled”.
The logic writes immediately to memory in a wrap around mode if the sample logic is enabled. The Sample ADC Data Start Address is the programmed Sample Memory Start Address + Header Length. The Sample Address will be incremented up to the programmable Sample Block Length and start then again from the Sample ADC Data Start Address.

Stop Mode is recommended if the required Pre-Trigger Length is greater than the maximum of the Ringbuffer Delay.

- programmable Event Length up to
  - 4 x 201.326.592 (1.25Gsps)
  - 2 x 402.653.184 (2.5Gsps)
  - 1 x 805.306.368 (5Gsps)
- programmable Number of Events (Multi Event)
- programmable Ringbuffer Delay to delay of the ADC data (6 to 6138 for each channel)
- programmable Direct Memory Pretrigger (Delay)

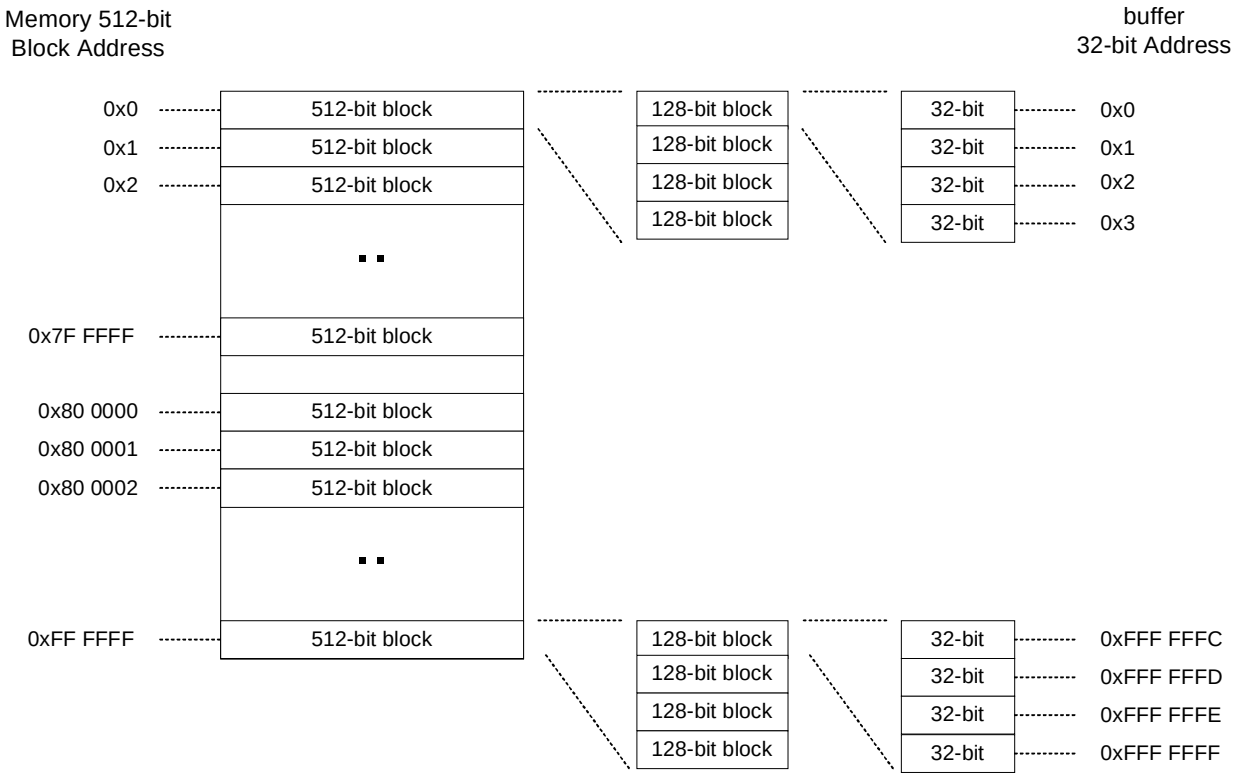




6 ADC memory

The two four channel groups have a one GByte memory space each.
It can be accessed by VME via the “fast data transfer logic” and it’s FIFOs.
The ADC sampling logic stores “Events” to memory in 512-bit blocks.
The smallest event size is 128-bit. Therefore the last 512-bit block is filled by the logic with 0xFFFFFFFF -as needed- after the sample logic is disabled.

1G x 8bit = 256M x 32bit = 64M x 128bit = 16M x 512bit



6.1 Event Data formats

ADC and TDC events are stored to memory tagged with an event ID. The event ID is used to distinguish between the different event types.

Event ID table:

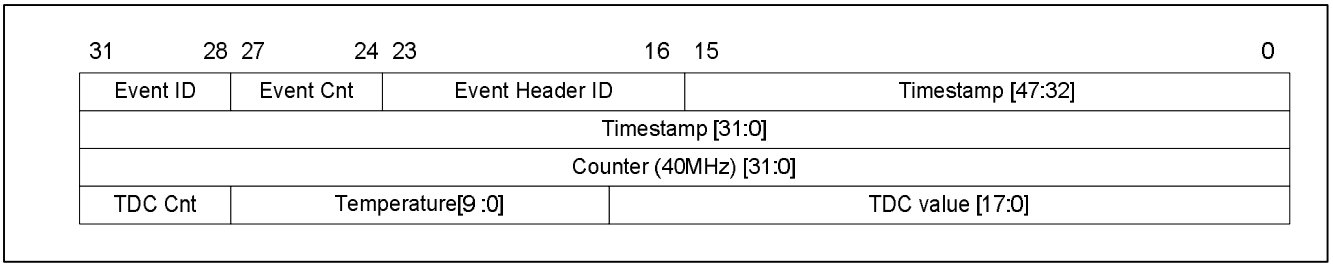
Event ID	Event Type
0x0	1.25 Gsps ADC 1 FIFO Event Data Format (internal trigger)
0x1	1.25 Gsps ADC 2 FIFO Event Data Format (internal trigger)
0x2	1.25 Gsps ADC 3 FIFO Event Data Format (internal trigger)
0x3	1.25 Gsps ADC 4 FIFO Event Data Format (internal trigger)
0x4	2.5 Gsps ADC 1/2 FIFO Event Data Format (internal trigger)
0x5	2.5 Gsps ADC 3/4 FIFO Event Data Format (internal trigger)
0x6	reserved
0x7	5 Gsps ADC 1/2/3/4 FIFO Event Format Data (5Gsps internal trigger or 1.25/2.5/5Gsps global trigger)
0x8	TDC FIFO Event Data Format
0x9	reserved
0xA	reserved
0xB	reserved
0xC	ADC Direct Memory Start Mode Event Data Format (global trigger)
0xD	ADC Direct Memory Wrap (Stop) Mode Event Data Format (global trigger)
0xE	reserved
0xF	Endmarker or rather the 512-bit block is filled with 0xF..F at the end

6.1.1 TDC FIFO Event Data format

TDC Fifo Event: (external Trigger In)

Event ID = 8

Header (4 x 32-bit words)



Event Cnt:	4-bit TDC Event Counter: counts the External Triggers in the ADC FPGA
Event Header ID:	programmable by the Event configuration registers
Timestamp:	could be cleared with Sampling enable or with first TDC-Event. Incremented with Clock/12 (2.5Ghz-> 208,33MHz). Latched with the TDC Event (External Trigger).
Counter 40MHz:	cleared with Sampling enable or with external Clear Incremented with external Count (max. 80MHz). Latched with the TDC Event (External Trigger).
TDC Cnt:	4-bit TDC Event Counter: counts the received TDC data messages (caused by the External Trigger in the VME FPGA)
Temperature:	value of the temperature sensor (see Temperature register).
TDC value:	value of the TDC measurement.

Example:

```
HEADER_EVENT_ID_TDC
82820000     decac6          0   32d40368
```

meaning:
82820000: Event ID = 8
82820000: Event Cnt = 2
82820000: "82" indicates Base Address 0x41000000, ADC chip 1

6.1.2 ADC 1.25 Gsps FIFO Event Data format (internal Trigger)

ADC Fifo Event: 1.25 Gsps (internal Trigger)

Event ID = 0 for Channel 1
Event ID = 1 for Channel 2
Event ID = 2 for Channel 3
Event ID = 3 for Channel 4

Header (4 x 32-bit words)

31 28	27 24	23 16	15 0
Event ID	Event Header Info	Event Header ID	Timestamp [47:32]
Timestamp [31:0]			
Counter (40MHz) [31:0]			
0x000		Trigger Index	Length [15:0] in Data blocks

1. Data Block (4 x 32-bit words)

00	sample 1 [9:0]	sample 2	sample 3
00	sample 4	sample 5	sample 6
00	sample 7	sample 8	sample 9
00	sample 10	sample 11	sample 12

2. Data Block

00	sample 13 [9:0]	sample 14	sample 15
00	sample 16	sample 17	sample 18
00	sample 19	sample 20	sample 21
00	sample 22	sample 23	sample 24

Event Cnt: 4-bit TDC Event Counter. It counts the External Trigger In pulses.

Event Header Info: programmable by the Event configuration registers
Event Header ID: programmable by the Event configuration registers

Timestamp: see TDC FIFO Event
Counter 40MHz. see TDC FIFO Event

Trigger Index: 4-bit value, it indicates the point in time of the internal trigger inside a 6-sample group (marked yellow). The point in time of a 6-sample group depends on the Ringbuffer Predelay.

Bit 3: indicates trigger condition GT (else LT)
Bit 2-0: indicates trigger position inside the 6-sample group (1 to 6)

Examples:

- Trigger Mode and internal Trigger
- ADC 5 (channel 5) Threshold GT = 0x262 (610)
- Sample Block Length = 4 (programmed 3) -> 4 x 12 samples = 48 samples

```
HEADER_EVENT_ID_1_25G_ADC1
  920000     9f78d8          0      a0004
 30   33   35     39   3e   44     4e   5c   6b     7b   90   aa
 c4   e1   ff     11f  141  163    187  1ab  1ce    1f0  210  22e
24c  266  280     29a  2ae  2c1    2d3  2e2  2f1    2fe  30a  310
31a  320  324     327  32b  32c    32d  32c  32c    32d  32c  32b
```

920000: Event ID = 0; Event Info = 0; "9" indicates ADC chip 2 -> channel 5 (bit 0 of the 9)

a0004: "a" indicates Trigger GT (bit 3) and on 2. position (0x266)

a0004: "4" indicates 4 x 128-bit blocks -> 48 samples

```
HEADER_EVENT_ID_1_25G_ADC1
  920000     a2a70f          0      e0004
 2e   2e   2e     30   33   34     37   3a   3f     46   50   5d
 6f   82   97     b0   cb   e9    108  127  14b    16c  190  1b3
1d5  1f9  219    236  252  26d    286  2a0  2b5    2c8  2d9  2e8
2f6  301  30a    313  31b  321    324  328  32a    32e  32f  32f
```

e0004: "a" indicates Trigger GT (bit 3) and on 6. position (0x26d)

```
HEADER_EVENT_ID_1_25G_ADC1
  920000     a5d547          0      c0004
 2e   31   31     32   38   3b     40   49   51     5c   6e   7f
 97   b2   cf     ec  108  12a    14c  170  192    1b5  1d7  1f9
219  237  253    26e  288  29f    2b5  2c9  2da    2ea  2f7  304
30c  314  31a    321  323  328    32a  32d  32d    32d  32b  32a
```

c0004: "a" indicates Trigger GT (bit 3) and on 4. position (0x26e)

6.1.3 ADC 2.5 Gsps FIFO Event Data format (internal Trigger)

ADC Fifo Event: 2.5 Gsps (internal Trigger)

Event ID = 4 for Channel 1,2
Event ID = 5 for Channel 3,4

Header (4 x 32-bit words)

31 28	27 24	23 16	15 0
Event ID	Event Header Info	Event Header ID	Timestamp [47:32]
Timestamp [31:0]			
Counter (40MHz) [31:0]			
0x00		ADC2/4 Trigger Index	ADC 1/3 Trigger Index	Length [15:0] in Data blocks

1. Data Block (8 x 32-bit words)

ADC 1/3	00	sample 1 [9:0]	sample 3	sample 5
	00	sample 7	sample 9	sample 11
	00	sample 13	sample 15	sample 17
	00	sample 19	sample 21	sample 23
ADC 2/4	00	sample 2 [9:0]	sample 4	sample 6
	00	sample 8	sample 10	sample 12
	00	sample 14	sample 16	sample 18
	00	sample 20	sample 22	sample 24

Examples:

- Trigger Mode and internal Trigger
- ADC 5/6 (channel 5) Threshold GT = 0x262 (610)
- Sample Block Length = 4 (programmed 3) -> 4 x 24 samples = 96 samples

```
HEADER_EVENT_ID_2_5G_ADC12
41920000    3deac70          0     e00004
 35   34   35     35   38   3c     42   47   4f     5a   6a   7a
 37   38   3b     3c   3d   41     48   4f   58     64   73   85
 8d   a6   bc     d5   f1  10e    12c  14d  16c    18a  1aa  1c9
 9b   b2   cc     e5  101  11c    13d  15b  17a    199  1b6  1d6
1e7  203  21e    236  24c  262    276  289  297    2a6  2b1  2bd
1f1  20e  226    23e  252  268    27a  28c  29d    2ab  2b6  2bf
2c4  2cd  2d5    2da  2db  2e1    2e7  2e5  2e4    2e4  2e6  2e4
2c7  2ce  2d5    2d7  2da  2dd    2e0  2e0  2e2    2e3  2e2  2e1
```

41920000: Event ID = 4; Event Info = 1; "9" indicates ADC chip 2 -> channel 5 (bit 0 of the 9)

e00004: "e0" indicates Trigger GT (bit 3) and on 6. position of ADC2 (0x26d)

```
HEADER_EVENT_ID_2_5G_ADC12
41920000    3e1daba          0     990004
 3d   41   4a     53   5e   6e     7e   93   a8     c2   db   f8
 42   48   51     5b   69   78     8a   9f   b5     ce   ea  106
114  134  153    173  192  1b0    1d0  1ec  207    223  239  24f
123  141  162    180  1a0  1bd    1dc  1f6  211    22c  244  259
265  278  28c    299  2a7  2b5    2bf  2c8  2d1    2d6  2d9  2dd
26d  27f  290    2a1  2ae  2b8    2c0  2c9  2cf    2d4  2da  2db
2e1  2e4  2e4    2e6  2e7  2e5    2e5  2e5  2e4    2e4  2e2  2e0
2df  2e1  2e1    2e2  2e1  2e2    2e2  2e2  2e0    2de  2dd  2dc
```

990004: "99" indicates Trigger GT (bit 3) and on 6. position (0x26d)

6.1.4 ADC 5 Gsps FIFO Event Data format

ADC Fifo Event: 5 Gsps (internal/external trigger)
2.5 Gsps (external trigger)
1.25 Gsps (external trigger)

Event ID = 7

Header (4 x 32-bit words)

31 28	27 24	23 16	15 0
Event ID	Event Header Info	Event Header ID	Timestamp [47:32]
Timestamp [31:0]			
Counter (40MHz) [31:0]			
ADC 4 Trigger Index	ADC 3 Trigger Index	ADC 2 Trigger Index	ADC 1 Trigger Index	Length [15:0] in Data blocks

1. Data Block (16 x 32-bit words)

Note: Sample N (1.25 Gsps) / N (2.5 Gsps) / N (5 Gsps)

ADC 1	00	sample 1 / 1 / 1 [9:0]	sample 2 / 3 / 5	sample 3 / 5 / 9
	00	sample 4 / 7 / 13	sample 5 / 9 / 17	sample 6 / 11 / 21
	00	sample 7 / 13 / 25	sample 8 / 15 / 29	sample 9 / 17 / 33
	00	sample 10 / 19 / 37	sample 11 / 21 / 41	sample 12 / 23 / 45
ADC 2	00	sample 1 / 2 / 3 [9:0]	sample 2 / 4 / 7	sample 3 / 6 / 11
	00	Sample 4 / 8 / 15	sample 5 / 10 / 19	sample 6 / 12 / 23
	00	sample 7 / 14 / 27	sample 8 / 16 / 31	sample 9 / 18 / 35
	00	sample 10 / 20 / 39	sample 11 / 22 / 43	sample 12 / 24 / 47
ADC 3	00	sample 1 / 1 / 2 [9:0]	sample 2 / 3 / 6	sample 3 / 5 / 10
	00	sample 4 / 7 / 14	sample 5 / 9 / 18	sample 6 / 11 / 22
	00	sample 7 / 13 / 26	sample 8 / 15 / 30	sample 9 / 17 / 34
	00	sample 10 / 19 / 38	sample 11 / 21 / 42	sample 12 / 23 / 46
ADC 4	00	Sample 1 / 2 / 4 [9:0]	sample 2 / 4 / 8	sample 3 / 6 / 12
	00	sample 4 / 8 / 16	sample 5 / 10 / 20	sample 6 / 12 / 24
	00	sample 7 / 14 / 28	sample 8 / 16 / 32	sample 9 / 18 / 36
	00	sample 10 / 20 / 40	sample 11 / 22 / 44	sample 12 / 24 / 48

Examples:

- Trigger Mode and internal Trigger (5 Gsps)
- ADC 1-4 (channel 1) Threshold GT = 0x262 (610)
- Sample Block Length = 4 (programmed 3) -> 4 x 48 samples = 192 samples

```
HEADER_EVENT_ID_5G_ADC1234
72820000     c4b50e          0   cdcd0004
 34   33   34     34   33   36     37   38   3c     44   4d   58
 34   32   32     34   33   35     38   3b   40     47   51   5c
 35   34   35     34   33   35     37   38   3e     46   52   5c
 33   33   33     32   34   37     39   3c   42     4b   55   62
 66   76   8a     a3   be   dc     fc  11f  143    16a  192  1b8
 6d   7f   95     b0   cc   eb    10f  132  155    17c  1a6  1cd
 6a   7b   90     a8   c4   e2    106  12a  14e    174  19c  1c4
 70   85   9c     b8   d4   f3    114  13a  160    186  1af  1d8
1e1  20b  232    257  27a  29f    2c0  2e0  2fc    316  332  348
1f5  21a  242    267  28a  2ae    2cd  2ec  306    322  33b  350
1ed  214  23b    25f  284  2a8    2c7  2e7  302    31f  337  34d
1ff  226  24a    270  293  2b6    2d7  2f3  310    328  340  353
35b  36c  37a    38a  394  39e    3a4  3aa  3ae    3b1  3b2  3b3
363  372  383    38f  398  3a0    3a4  3aa  3b0    3b3  3b4  3b5
361  372  380    38e  399  3a0    3a7  3aa  3ae    3b3  3b3  3b5
366  375  384    390  39a  3a3    3a8  3ac  3b1    3b3  3b4  3b4
```

cdcd0004: "cdcd" indicates Trigger GT (bit 3) and
on 5. position ADC1/3 and 4. position ADC2/4
→ 1.trigger (0x267) on 4. position ADC2

```
HEADER_EVENT_ID_5G_ADC1234
72820000     e488ca          0   abbb0004
 34   33   33     35   36   3a     41   45   4c     56   64   74
 30   33   34     36   38   3b     40   46   50     5c   6a   7c
 33   34   36     37   37   39     3e   45   4e     59   66   7a
 32   32   35     36   38   3d     42   49   54     60   71   84
 89   a1   bb     d9   f9  11a    13e  165  18e    1b6  1dc  205
 93   ac   c8     e6  107  12c    151  178  1a0    1c7  1f2  216
 8e   a7   c1     de  100  123    148  16e  197    1c0  1e9  20f
 9a   b3   cf     ee  110  137    15a  184  1ab    1d2  1fa  221
22d  252  277    29a  2bc  2db    2f9  315  32e    345  358  367
23e  262  285    2a8  2c9  2e8    305  320  338    34d  361  372
236  25a  280    2a3  2c4  2e4    301  31c  333    34a  35f  36f
247  26c  28f    2b2  2d2  2f1    30d  327  33d    351  362  375
378  387  391    39c  3a4  3aa    3af  3b3  3b5    3b6  3b6  3b7
381  38a  396    39d  3a7  3ab    3af  3b1  3b2    3b5  3b5  3b5
37f  38b  394    39d  3a5  3ac    3b0  3b4  3b4    3b4  3b6  3b6
384  391  39a    3a1  3a6  3ac    3ae  3b0  3b4    3b6  3b6  3b6
```

abbb0004: "abbb" indicates Trigger GT (bit 3) and
on 2. position ADC4 and 3. position ADC1/3/2
→ 1.trigger (0x26C) on 2. position ADC4

6.1.5 ADC Direct Memory Event Data format (external Trigger)

ADC Direct Memory Event:

Event ID = 0xC for ADC Direct Memory Start Mode
Event ID = 0xD for ADC Direct Memory Wrap (Stop) Mode

Header (16 x 32-bit words)

31 28	27 24	23 16	15 0
Event ID	Event Header Info	Event Header ID	Timestamp [47:32]
Timestamp [31:0]			
Counter (40MHz) [31:0]			
Length [31:0] in Data blocks (16x32-bit words)			
Wrap-flag	0000000	Wrap stop offset [23:0] in Data blocks	
0x0000			Event Counter
0x00000000			
0x00000000			

redundant second block

Event ID	Event Header Info	Event Header ID	Timestamp [47:32]
Timestamp [31:0]			
Counter (40MHz) [31:0]			
Length [31:0] in Data blocks			
Wrap-flag	0000000	Wrap stop offset [23:0] in Data blocks	
0x0000			Event Counter
0x00000000			
0x00000000			

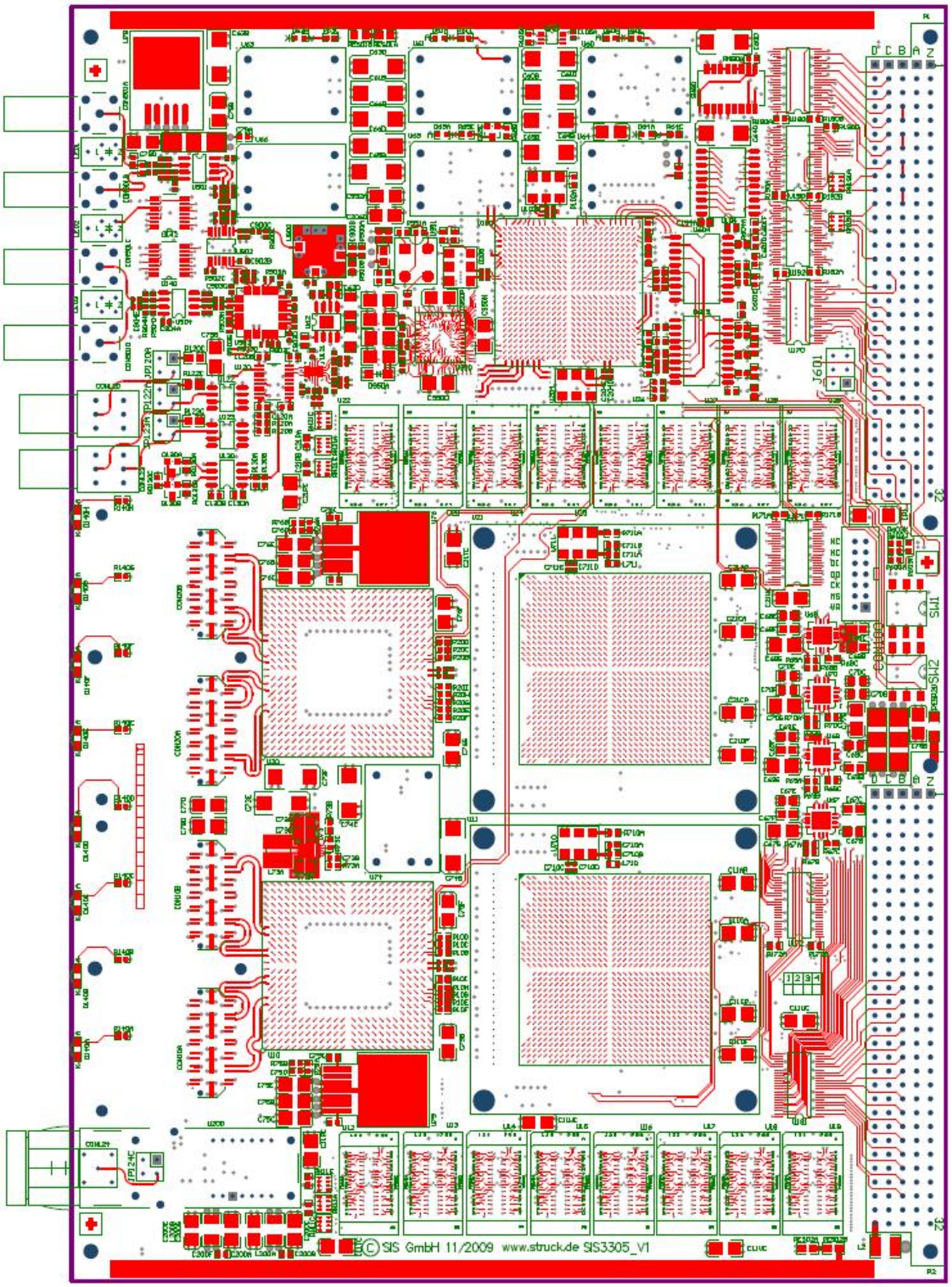
1. Data Block (16 x 32-bit words)

Note: Sample N (1.25 Gsps) / N (2.5 Gsps) / N (5 Gsps)

ADC 1	00	sample 1 / 1 / 1 [9:0]	sample 2 / 3 / 5	sample 3 / 5 / 9
	00	sample 4 / 7 / 13	sample 5 / 9 / 17	sample 6 / 11 / 21
	00	sample 7 / 13 / 25	sample 8 / 15 / 29	sample 9 / 17 / 33
	00	sample 10 / 19 / 37	sample 11 / 21 / 41	sample 12 / 23 / 45
ADC 2	00	sample 1 / 2 / 3 [9:0]	sample 2 / 4 / 7	sample 3 / 6 / 11
	00	Sample 4 / 8 / 15	sample 5 / 10 / 19	sample 6 / 12 / 23
	00	sample 7 / 14 / 27	sample 8 / 16 / 31	sample 9 / 18 / 35
	00	sample 10 / 20 / 39	sample 11 / 22 / 43	sample 12 / 24 / 47
ADC 3	00	sample 1 / 1 / 2 [9:0]	sample 2 / 3 / 6	sample 3 / 5 / 10
	00	sample 4 / 7 / 14	sample 5 / 9 / 18	sample 6 / 11 / 22
	00	sample 7 / 13 / 26	sample 8 / 15 / 30	sample 9 / 17 / 34
	00	sample 10 / 19 / 38	sample 11 / 21 / 42	sample 12 / 23 / 46
ADC 4	00	Sample 1 / 2 / 4 [9:0]	sample 2 / 4 / 8	sample 3 / 6 / 12
	00	sample 4 / 8 / 16	sample 5 / 10 / 20	sample 6 / 12 / 24
	00	sample 7 / 14 / 28	sample 8 / 16 / 32	sample 9 / 18 / 36
	00	sample 10 / 20 / 40	sample 11 / 22 / 44	sample 12 / 24 / 48

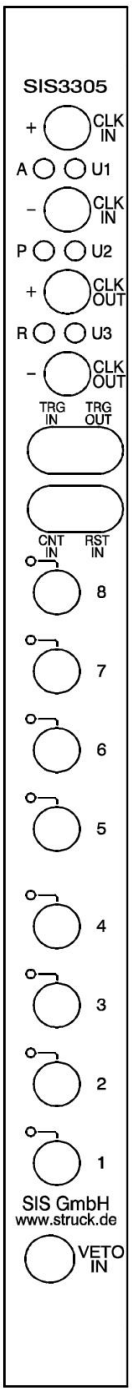
7 Board layout

A printout of the silk screen of the component side of the PCB is shown below.



8 Front panel

The SIS3305 is a single width (4TE) 6U VME module. A sketch of the SIS3305 front panel (without handles) is shown below.



8.1 Front Panel LED's

The SIS3305 has 6 front panel LEDs to visualise part of the modules status. The access LED is a good way to check first time communication/addressing with the module.

Color	Designator	Function
Yellow	A	Access to SIS3305 VME slave port
Red	P	Power
Green	R	Ready, on board logic configured
Yellow	U1	User, to be set/cleared under program control*
Red	U2	User, to be set/cleared under program control* or Data sampling (ADC data transfer to Memory acitve) *
Green	U3	User, to be set/cleared under program control* or Data sample logic enabled*

* see Control Register
The three USER Leds (U1,U2,U3) are flashing with 4 Hz to indicate the over temperature state (U2 is inverted to U1,U3).

8.2 Channel LED's L1-L8

The 8 card edge surface mounted LEDs L1, ..., L8 can be seen through the corresponding holes in the front panel. They visualize the trigger status of the corresponding channel. The on duration is stretched for better visibility of short pulses.

8.3 PCB LEDs

Surface mounted red LEDs are used to signal power status, trigger status and FPGA debug information (the use of the debug LEDs is firmware design dependent).
A table with the SMD LEDs is given below.

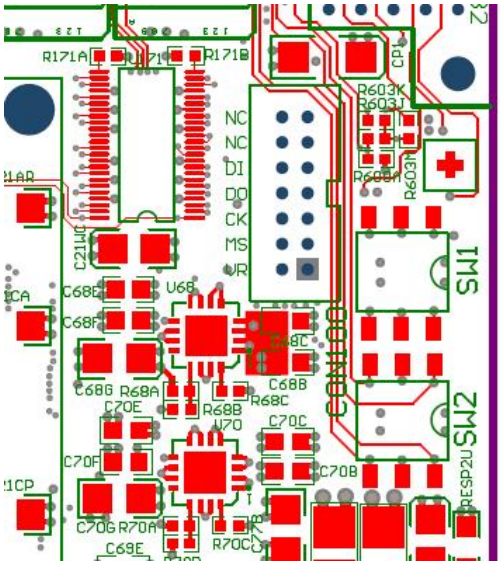
Designator	Function
D140A	Front panel trigger LED L1
D140B	Front panel trigger LED L2
D140C	Front panel trigger LED L3
D140D	Front panel trigger LED L4
D140E	Front panel trigger LED L5
D140F	Front panel trigger LED L6
D140G	Front panel trigger LED L7
D140H	Front panel trigger LED L8
D60A	Power D+1.0V core voltage Virtex5
D61A	Power D+1.2V core voltage Virtex4
D63A	Power D+2.5V
D64A	Power D+3.3V
D65A	Power D+1.8V

9 Jumpers/Connectors

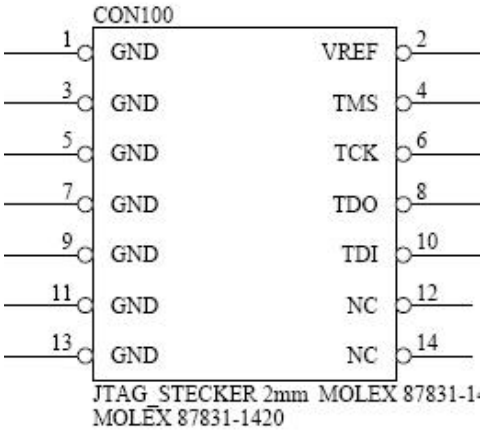
The following subsections list the configuration jumpers and connectors of the SIS3305.

9.1 CON100 JTAG

The SIS3305 on board logic can load its firmware from a serial PROMs , via the JTAG port on connector CON100 or over VME. A list of firmware designs can be found under http://www.struck.de/sis3305firm.htm.
Hardware like the XILINX HW-USB-JTAG in connection with the appropriate software will be required for in field JTAG firmware upgrades. The JTAG chain configuration is selected with the register XX is used to choose VME or CON100 as JTAG source.
CON100 is a 2mm (i.e. metric) 14 pin header that allows you to reprogram the firmware of the SIS3305 with a JTAG programmer. The pin out is shown in the schematic below. It is compatible with the cable that comes with the XILINX HW-USB platform cable.



The schematic for CON100 is shown below.

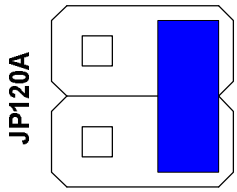


Note: The SIS3305 has to be powered for reprogramming over JTAG.

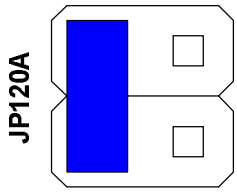
9.2 JP120A 50 Ohm Termination NIM_TRIGGER_IN

50 Ohm termination of the trigger input signal is enabled or disabled with the jumper JP120A you can enable or disable the.

(Position 1-2 closed 50 Ohm termination enabled):



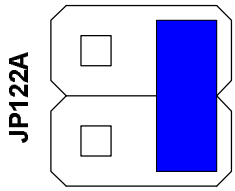
(Position 3-4 closed 50 Ohm termination disabled):



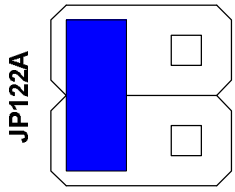
9.3 JP122A 50 Ohm Termination NIM_COUNT_IN

50 Ohm termination of the count input signal is enabled or disabled with the jumper JP122A

(Position 1-2 closed 50 Ohm Termination enabled):



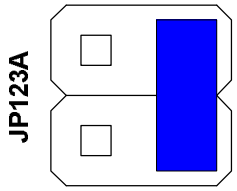
(Position 3-4 closed 50 Ohm Termination disabled):



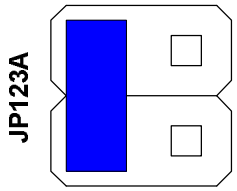
9.4 JP123A 50 Ohm Termination NIM_RESET_IN

50 Ohm termination of the reset signal is enabled or disabled with the jumper JP123A

(Position 1-2 closed 50 Ohm Termination enabled):



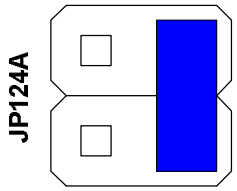
(Position 3-4 closed 50 Ohm Termination disabled):



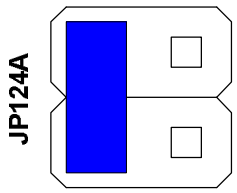
9.5 JP124C 50 Ohm Termination NIM_VETO_IN

50 Ohm termination of the Veto signal is enabled or disabled with the jumper JP124C

(Position 1-2 closed 50 Ohm Termination enabled):

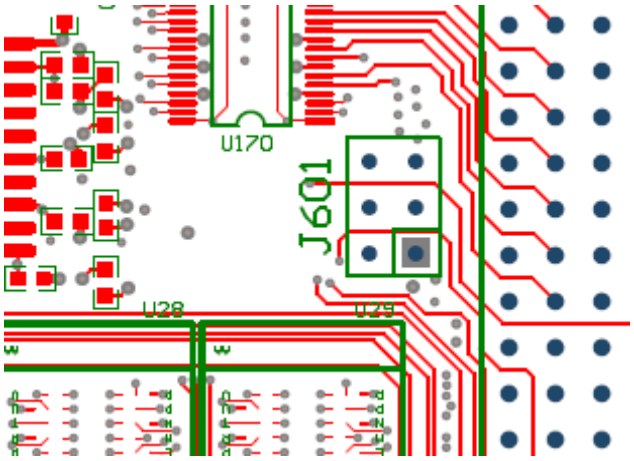


(Position 3-4 closed 50 Ohm Termination disabled):

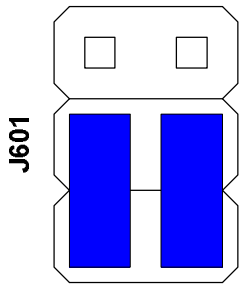


9.6 J601 JTAG chain

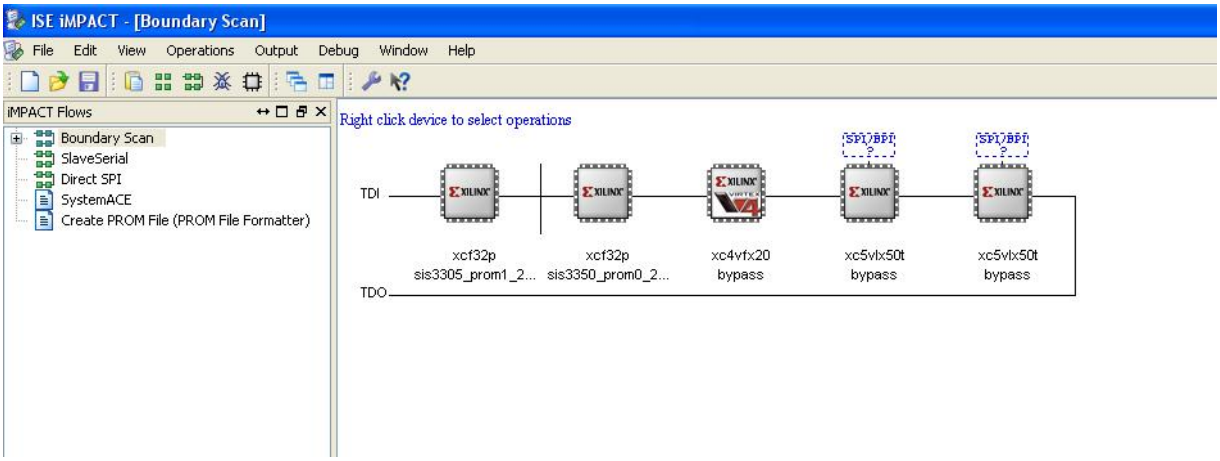
The JTAG chain on the SIS3305 can be configured to comprise the serial PROM only (short JTAG chain) or to comprise the serial PROM and the Virtex FPGA (long chain). The configuration is selected with the 6-pin array J601 as sketched below:



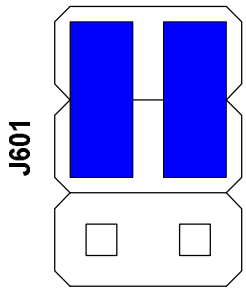
Long Chain (1-3 and 2-4 closed):



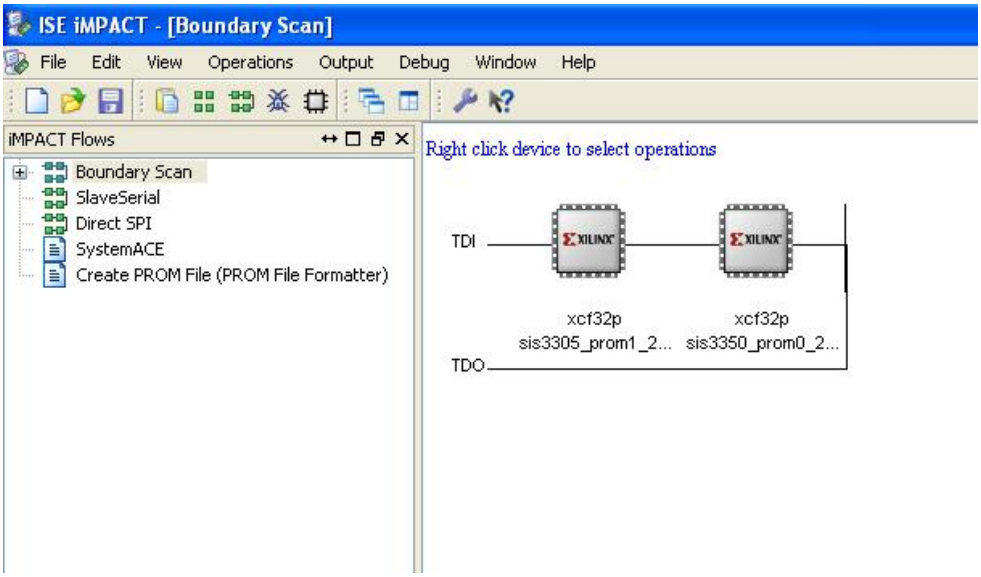
In the Impact software you will see all 5 Xilinx devices as shown below:



Short Chain (3-5 and 4-6 closed, factory default):



In the Impact software you will see the two serial Xilinx PROMs as shown below:

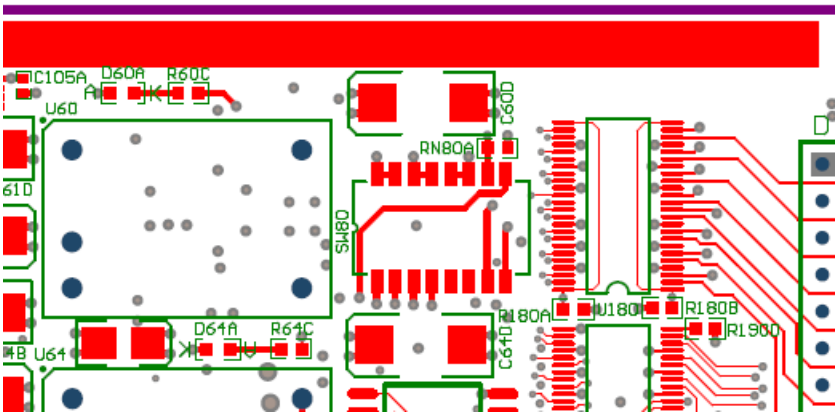


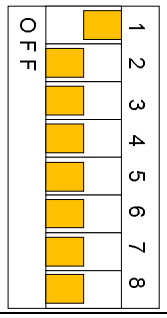
9.7 SW1/SW2 VME Base Address Rotary switches

The two rotary switches of SW1 and SW2 are used to set the base address. The function may depend on the setting of switches 1-4 of SW80 also (refer to the VME addressing section 3).

9.8 SW80 Dip switch /Reset Behavior/Slave Addressing/Watchdog-Disable

The 8 switches of SW80 are in charge of system controller function, reset behaviour and slave addressing as listed in the table below. Factory default settings are illustrated on the left hand side of the table.

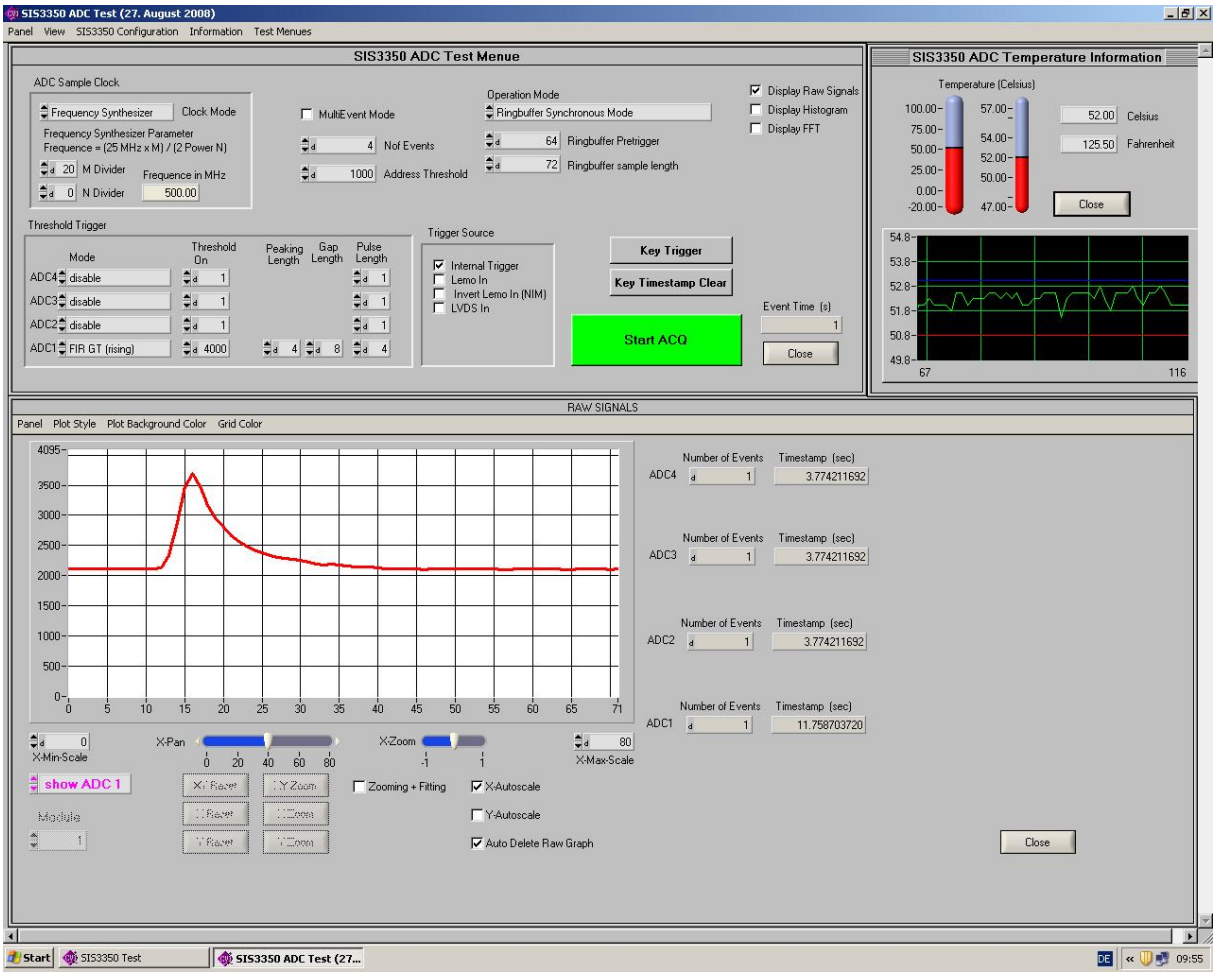


SW80	Function
	EN_A32 Slave Addressing
	EN_A16 reserved for future slave use
	EN_GEO reserved for future slave use
	EN_RES reserved for future slave use
	Not used
	Not used
	Watchdog enable
	Connect VME SYSRESET to FPGA reset

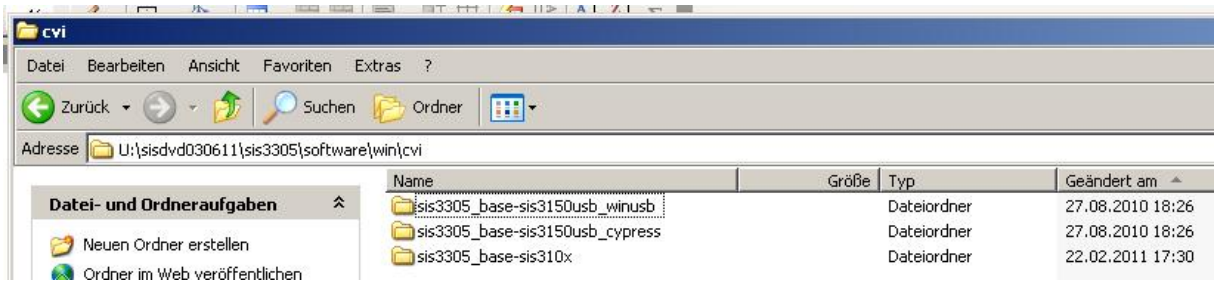
10 Getting started

10.1 SIS3305 base program

The runtime version of the SIS3305 base program in combination with a SIS3150 USB to VME or a SIS1100(e)/310x PCI (Express) to VME interface provides access to all implemented SIS3305 features without the need for coding in the first step under Windows. Feel free to inquire about the possibility for a loaner in case you are working with another VME master.
An example screen shot of the SIS3305 base program (a signal acquired in ring buffer synchronous mode of operation).



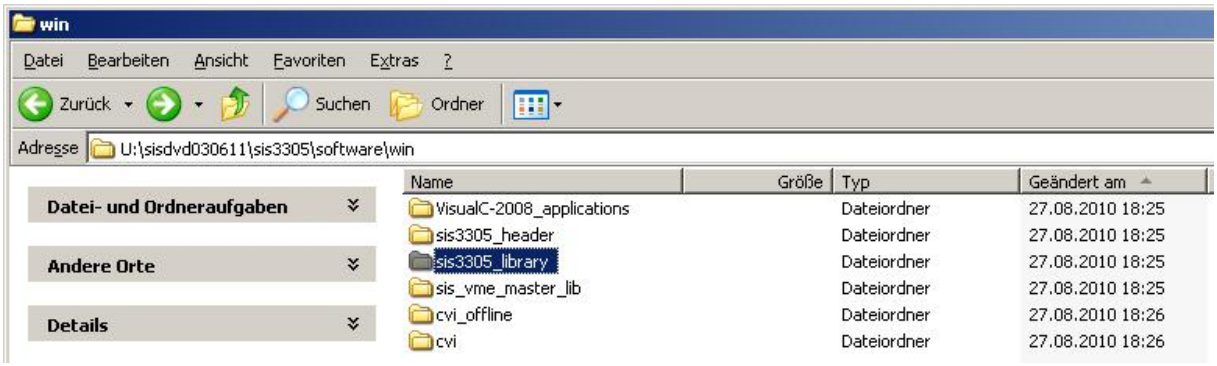
Three different precompiled versions of the SIS3305 base program can be found on the DVD as shown below.



Sis3305_base-sis3150usb_winusb is for operation with the SIS3150USB to VME interface and the standard Windows USB driver installed. Sis3305_base-sis3150usb_cypress is for operation with the SIS3150USB to VME interface under a Cypress USB driver installation and sis3305_base-sis310x for all SIS1100(e)/310x PCI (Express) to VME interfaces.

10.2 Software examples

The SIS3305 software win directory has the structure shown below.



The SIS3305.h file can be found in the sis3305_header directory and the sis3305_library directory contains library elements for SIS3305 operation.
The VisualC-2008_applications folder holds code for firmware upgrade over VME.
The source code and the distribution kits for National Instruments Labwindows CVI can be found n the CVI directory (for SIS3150USB and SIS1100(e)/310x interfaces as above).
.
The `sis3305_adc_test.c` file has routines like:

```
int RunTest_SIS3305_Test_Direct_Memory_Stop_Mode_Aquisition (void)  ;
```

With step by step commented setup:

11 Appendix

11.1 Power consumption

The SIS3305 uses standard VME voltages only.

Voltage	Current
+ 5V	12.5 A
+12 V	0.01 A
- 12 V	0.15 A

11.2 Operating conditions

11.2.1 Cooling

Although the SIS3305 is mainly a 2.5 and 3.3 V low power design, massive power is consumed by the Analog to Digital converter chips, FPGAs and linear regulators however. Hence forced air flow is required for the operation of the board. The board may be operated in a non condensing environment at an ambient temperature between 10° and 25° Celsius. A power up warm up time of some 10 minutes is recommended to ensure equilibrium on board temperature conditions.

Note: an over temperature protection mechanism is implemented to avoid damage to the ADC and FPGA chips (refer to section 4.8)

11.2.2 Non Hot swap/live insertion

Please note, that the VME standard does not support hot swap by default and that the SIS3305 is not hot pluggable. The VME crate has to be powered down for SIS3305 module insertion and removal.

11.3 Connector types

The table below lists the connectors used on the SIS3305.

Designation	Function	Manufacturer	Part Number
CON10A CON10B	Analog_In Piggy Back Ch1-Ch4	SAMTEC	QTE-014-03-L-D-DP-A-K
CON20A CON20B	Analog In Piggy Back Ch5-Ch8	SAMTEC	QTE-014-03-L-D-DP-A-K
CON100	JTAG	MOLEX	87831-1420
CON 120	Trigger_In Trigger_Out	LEMO	EPY.00.250.NTN
CON 123	Count_In Reset_In	LEMO	EPY.00.250.NTN
CON124	VETO_IN	LEMO	EPL.00.250.NTN
CON901A	CLK_IN +	JYEBAO	SMA8400A1-9000
CON901B	CLK_IN -	JYEBAO	SMA8400A1-9000
CON901C	CLK_OUT +	JYEBAO	SMA8400A1-9000
CON901D	CLK_OUT -	JYEBAO	SMA8400A1-9000
CON901D	CLK_OUT -	JYEBAO	SMA8400A1-9000
P1, P2	VME _BUS	HARTING	02 01 160 2101

11.4 Row d and z Pin Assignments

The SIS3305 is prepared for the use with VME64x backplanes. A foreseen feature is geographical addressing . The prepared pins on the d and z rows of the P1 and P2 connectors are listed below.

Position	P1/J1		P2/J2	
	Row z	Row d	Row z	Row d
1		VPC (1)		
2	GND	GND (1)	GND	
3				
4	GND		GND	
5				
6	GND		GND	
7				
8	GND		GND	
9		GAP*		
10	GND	GA0*	GND	
11	RESP*	GA1*		
12	GND		GND	
13		GA2*		
14	GND		GND	
15		GA3*		
16	GND		GND	
17		GA4*		
18	GND		GND	
19				
20	GND		GND	
21				
22	GND		GND	
23				
24	GND		GND	
25				
26	GND		GND	
27				
28	GND		GND	
29				
30	GND		GND	
31		GND (1)		GND (1)
32	GND	VPC (1)	GND	VPC (1)

Note: Pins designated with (1) are so called MFBL (mate first-break last) pins on the installed 160 pin connectors, VPC(1) pins are connected via inductors.

11.5 Firmware upgrade

The firmware of the SIS3305 can be upgraded over JTAG. The upgrade options are VME (on units that have intact firmware) and the JTAG connector CON100. Refer to the section 9.1 also,

12 Index

I

J

K

L

M

O

P

R

S

T

U

V

W

X