Technical Information Manual

Revision n. 3

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MOD. V895 series

16 CHANNEL
LEADING EDGE
DISCRIMINATORS

NPO:
00101/97:V895x.MUTx/03

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Disposal of the Product

The product must never be dumped in the Municipal Waste. Please check your local regulations for disposal of electronics products.

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1. General description

1.1. Functional description

The CAEN Mod. V895 is a 16 CHANNEL LEADING EDGE DISCRIMINATOR housed in a single width VME module. The module accepts 16 negative inputs (positive on request) and produces 16 differential ECL outputs with a fan-out of two on two front panel header connectors (a functional block diagram is shown in Fig. 1.2).

The pulse forming stage of the discriminator produces an output pulse whose width is adjustable in a range from 5 ns to 40 ns via VME.
Each channel can work both in Updating and Non-Updating mode according to on-board jumpers position.

The discriminator thresholds are individually settable in a range from -1 mV to -255 mV (1 mV step), via VME through an 8-bit DAC. The front panel houses also VETO and TEST inputs.

A Current Sum output generates a current proportional to the input multiplicity, i. e. to the number of channels over threshold, at a rate of -1.0 mA per hit ±20 %.

A "MAJORITY" output provides a NIM signal if the number of input channels over threshold exceeds the MAJORITY programmed value.

Several V895 boards can be connected in a daisy chain via the Current Sum output: in this case, by switching the majority logic to “External”, it’s possible to obtain a Majority signal when the number of active channels in the chained modules exceeds a global Majority level.

An "OR" output on a front panel connector provides a global OR of the output channels. The relevant "OR" LED lights up if at least one of the unmasked channels is over threshold. The module's operations are completely controlled via software for each channel through the VME bus. The most important are:

- Setting of the discriminator thresholds (8 bit data) from -1 to -255 mV.
- Setting pattern of inhibit; each channel can be turned "ON" or "OFF" by using a mask register.
- Setting output width in a range from 5 to 40 ns.
- Setting of the Majority threshold value.
- Common TEST.

Several versions are available, refer to Table 1.1 for details.

Table 1.1:Versions available for the Model V895

Version[1]	Number of channels	PAUX connector[2]
V895[3]	16	yes
V895 B	16	no

Fig. 1.1: Model type label (example: V895 B)

[1] A label on the printed board soldering side indicates the module’s version (see Fig 1.1).

[2] The version with the PAUX connector requires the V430 backplane.

[3] Available exclusively on request

1.2. Block diagram

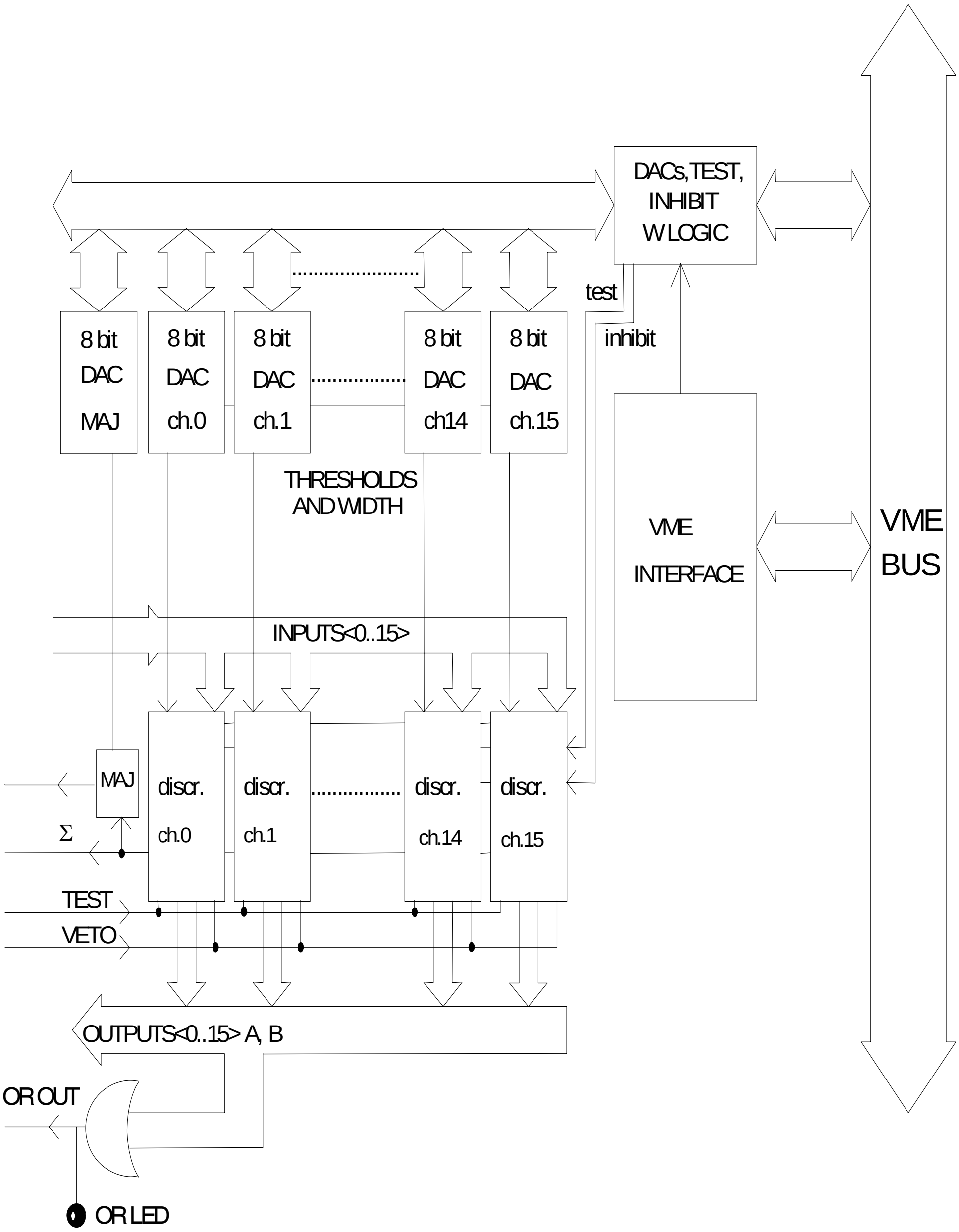


Fig. 1.2: Block Diagram

1.3. Technical specification table

Table 1.2: Technical specification table

General	
Packaging	6U-high, 1U-wide VME unit
Power requirements	Refer to § 2.2
Threshold range	-1 mV to -255 mV (-1 mV step)
Input Signals	
Inputs Channels	16 inputs negative polarity DC coupling
Input Impedance	50 Ω
Reflections	<4% for input pulses of 2 ns rise time
Input Range	-5 mV ÷ -5 V
Input Offset	±5 mV
Max input frequency	140 MHz (Updating mode) 80 MHz (Non Updating mode)
Double Pulse Resolution	7 ns (Updating mode) 12 ns (Non Updating mode)
Test Input	NIM logic signal High impedance Min. FWHM: 5 ns Max. frequency: 60 MHz
Veto Input	NIM logic signal High impedance Min. FWHM: 15 ns

Output Signals	
Outputs	16 ECL outputs with a fan-out of two
Outputs Impedance	110 Ω
Output Width	5±1 ns to 40±5 ns FWHM
Output Rise/Fall Time	<3 ns
Input/Output Delay	15.5 ± 1.5 ns
Crosstalk	<47 dB
Majority Output	NIM logic signal 50 Ω impedance
Or Output	NIM logic signal 50 Ω impedance Max. frequency: 50 MHz
Σ Output	-1 mA ± 20% per hit high impedance Max. frequency: 25 MHz

2. Technical Specifications

2.1. Packaging

The Models V895 and V895 B are housed in a 6U-high 1U-wide VME unit.
The Mod. V895 is provided with P1, P2 and PAUX connectors.
The Mod. V895 B is provided with P1, P2 connectors (NO PAUX).

2.2. Power requirements

The power requirements of the Mod. V895 and Mod. V895 B (NO PAUX) are as follows:

Table 2.3: Power requirements

Power supply	V895	V895 B
+ 12 V	110 mA	110 mA
- 12 V	50 mA	50 mA
+ 5 V	700 m A	5.5 A
- 5 V	3.5 A	-

2.3. Front panel

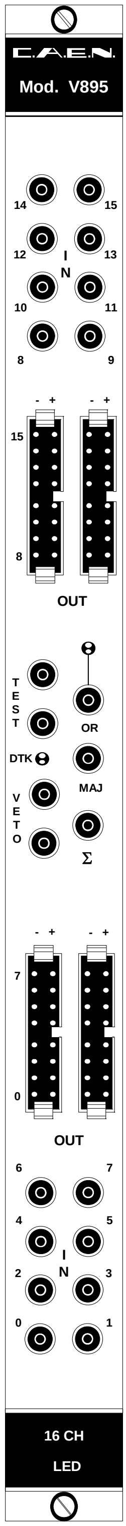


Fig. 2.1: Mod. V895 front panel

2.4. External connectors

The location of the connectors is shown in Fig. 2.1. Their function and electromechanical specifications are listed in the following subsections.

2.4.1. INPUT connectors

INPUT CHANNELS:

Mechanical specifications:
16 LEMO 00 type connectors.
Electrical specifications:
negative polarity, 50 Ohm impedance, DC coupling; input range: -5 mV ÷ -5 V; input offset: ±5 mV; 140 MHz maximum input frequency.

VETO INPUT:

Mechanical specifications:
1 LEMO 00 type connectors.
Electrical specifications:
standard NIM logic signal, high impedance, 15 ns minimum FWHM; leading edge of the VETO signal must precede of at least 8 ns the leading edge of the input and overlap completely the input signal; the VETO signal doesn’t act on TEST input.

TEST INPUT:

Mechanical specifications:
1 LEMO 00 type connectors.
Electrical specifications:
standard NIM logic signal, high impedance, 5 ns minimum FWHM, 60 MHz maximum input frequency.

2.4.2. OUTPUT connectors

OUTPUT CHANNELS:

Mechanical specifications:
4 Header 3M 3408-D202 type, 8+8 pin connectors.
Electrical specifications:
Differential ECL level on 110 Ohm impedance; pulse width adjustment from 5±1 ns to 40±5 ns FWHM.
Input/Output delay: 15.5±1.5 ns.

OR OUTPUT:

Mechanical specifications:
1 LEMO 00 type connectors.
Electrical specifications:
standard NIM logic signal, 50 Ω impedance;
50 MHz maximum input frequency.

Σ OUTPUT:

Mechanical specifications:
1 LEMO 00 type connectors.
Electrical specifications:
current output (-1 mA ± 20% per hit), high impedance; 25 MHz maximum input frequency.

MAJORITY OUTPUT:

Mechanical specifications:
1 LEMO 00 type connectors.
Electrical specifications:
standard NIM logic signal, 50 Ω impedance.

2.5. Other components

2.5.1. Displays

The front panel hosts the following LEDs:

DTACK
Type: 1 green LED
Function: VME selected; it lights up during a VME access.

OR
Type: 1 green LED
Function: it lights up if at least one output signal is present.

2.5.2. Switches

ROTARY SWITCHES
Function: they allow to select module's base address; please refer to Fig. 2.2 for their setting.

2.5.3. Jumpers

JP1
Function: it allows to select the Majority logic (Internal, External); please refer to Fig. 2.3 for the jumper location on the V895 board.

MODE JUMPERS
16 3-pin jumpers allow to select the channel's operating mode (updating / non updating); refer to Fig. 2.3 for the jumpers' location on the V895 board.

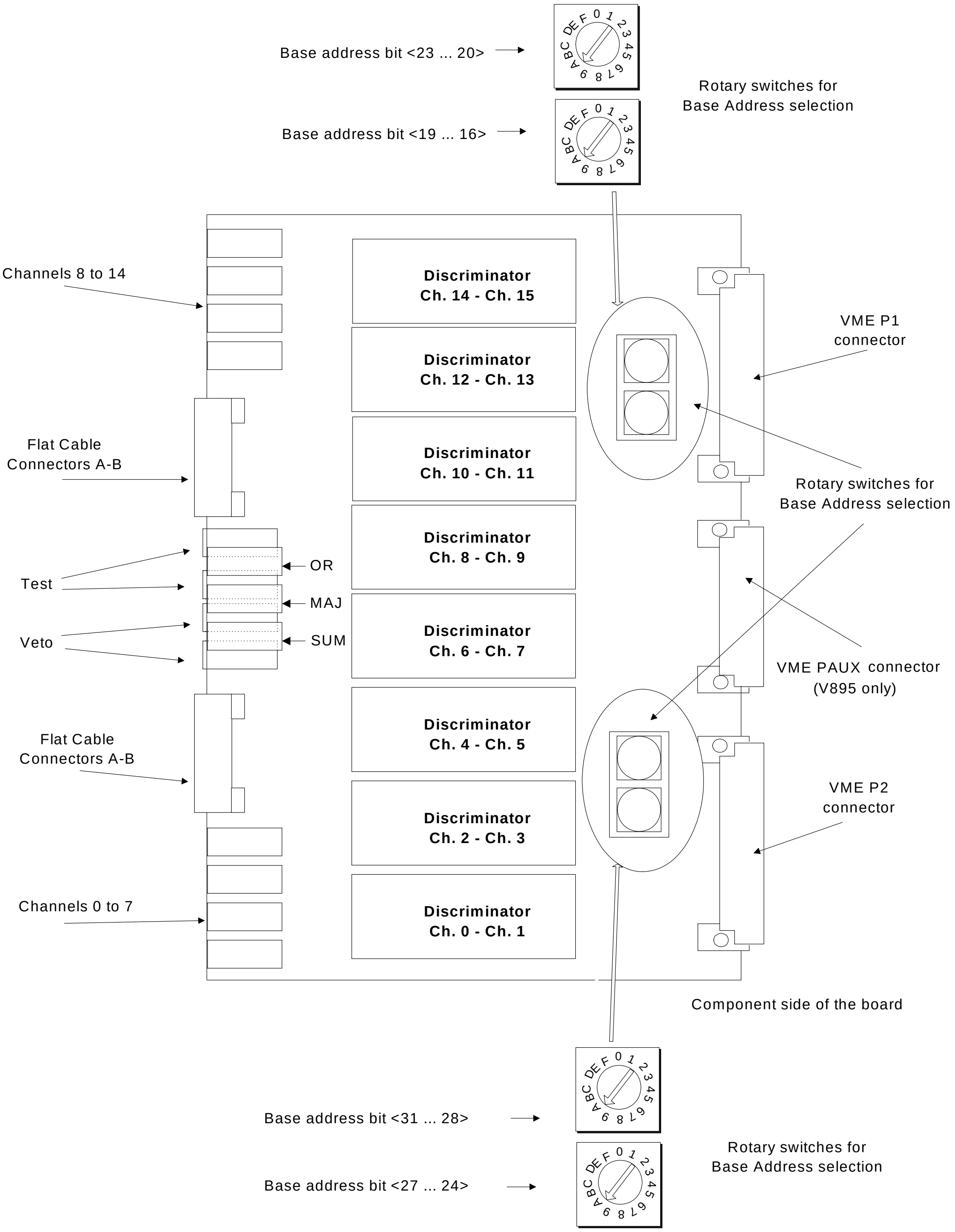


Fig. 2.2: Components location

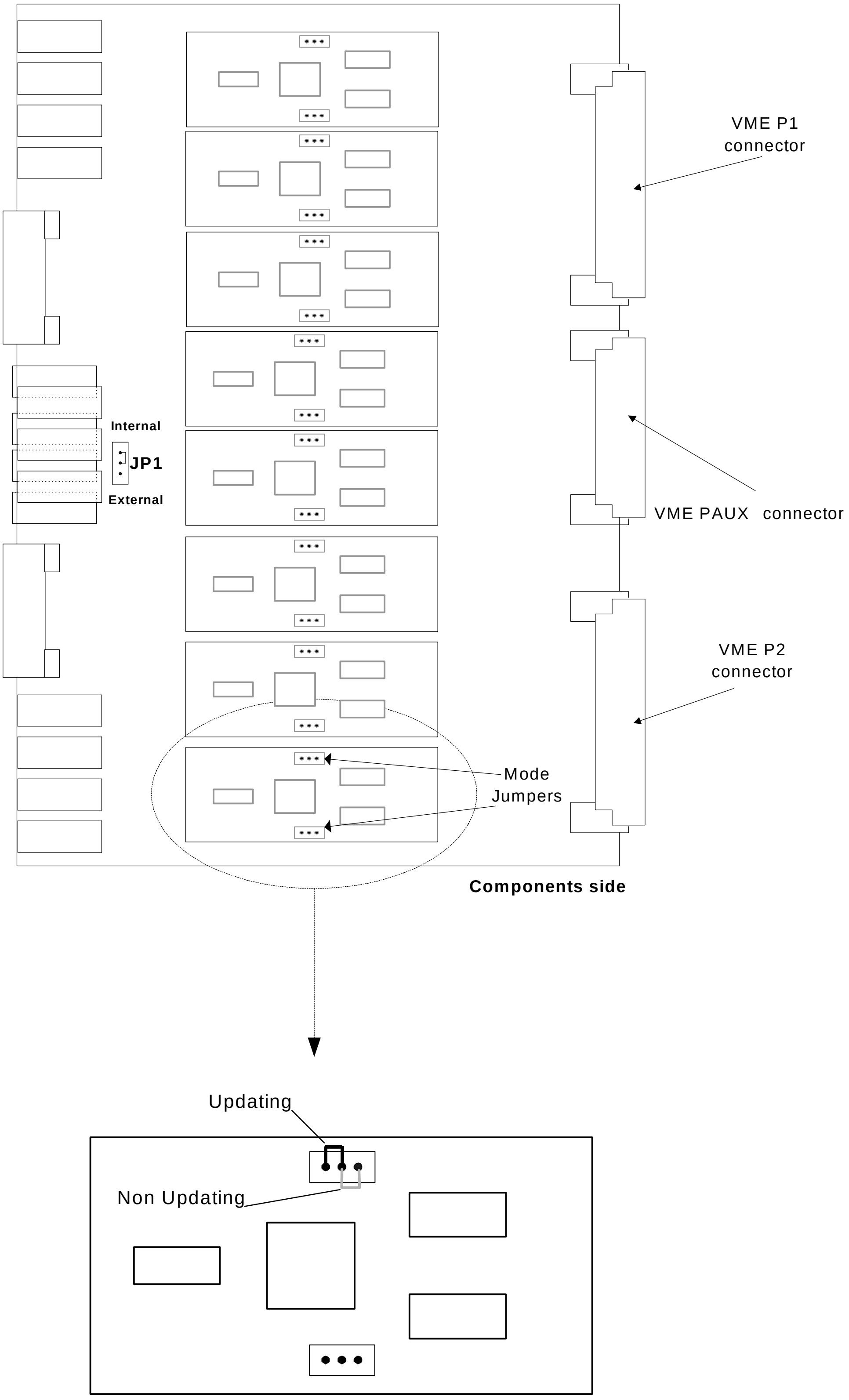


Fig. 2.3: Jumpers location

2.6. Characteristic of the signals

INPUTS

Channels: Negative polarity, 50 Ohm impedance; maximum input frequency:

- 140 MHz (updating)
- 80 MHz (non updating)

DC coupling; input range: -5 mV ÷ -5 V; input offset: ± 5 mV; reflections: ≤ 4% for 2 ns rise time input signals.

VETO: standard NIM logic signal, high impedance, 15 ns minimum FWHM. Leading edge of the VETO signal must precede of at least 8 ns the leading edge of the input and overlap completely the input signal (see Fig. 2.4).

N.B.: the VETO signal doesn't act on TEST input

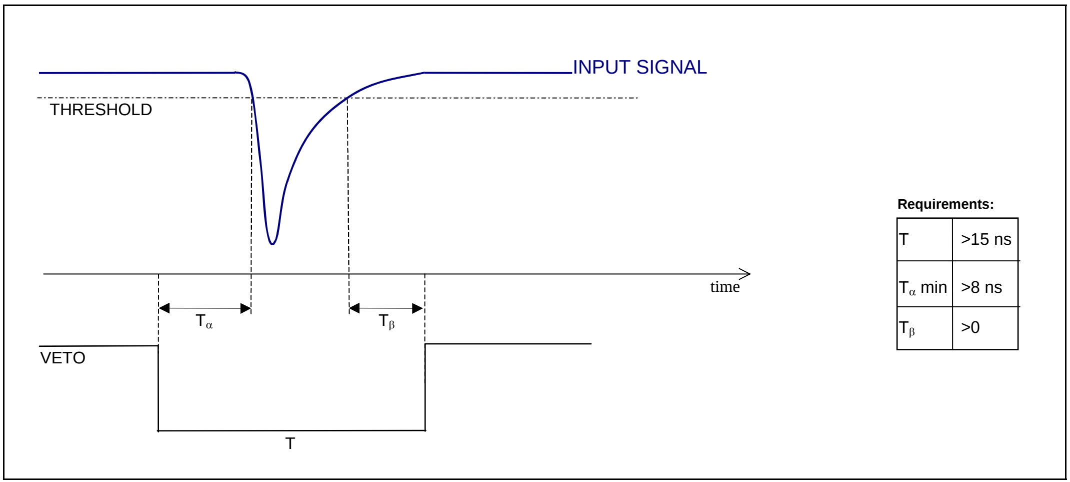


Fig. 2.4: Veto signal

TEST: standard NIM logic signal, high impedance, 5 ns minimum FWHM, 30 MHz maximum input frequency.

OUTPUTS

Outputs: Differential ECL level on 110 Ohm impedance. Pulse width adjustment: from 5±1 ns to 40±5 ns FWHM. Outputs pulses can be programmed either in Updating or Non-Updating mode (see § 4.5). Output pulse rise/fall time: <3 ns. INPUT-OUTPUT delay: 17.5±1.5 ns.

OR: standard NIM logic signal on 50 Ohm; maximum output frequency: 50 MHz; 4 ns rise/fall time.

CURRENT SUM: high impedance with rate of -1 mA ± 20% per hit; maximum output frequency: 25 MHz; 8 ns rise/fall time.

MAJORITY: standard NIM logic signal on 50 Ohm.

3. VME Interface

3.1. Addressing capability

The V895 module works in A24/A32 mode. This implies that the module's address must be specified in a field of 24 or 32 bits. The address modifiers codes recognized by the module are:

AM = %39 Standard user data access
AM = %3D Standard supervisor data access
AM = %09 Extended user data access
AM = %0D Extended supervisor data access

The module's Base address is fixed by 4 Internal rotary switches housed on two piggy-back boards plugged into the main printed circuit board (see Fig. 2.2).
The Base address can be selected in the range:
% 00 0000 <-> % FF 0000 A24 mode
% 0000 0000 <-> % FFFF 0000 A32 mode
The module's address lines A09÷A15 are not connected, so their content is meaningless: for example writing to either Base + 104C or Base + 284C the same register is accessed.

Table 3.1: Address Map

ADDRESS	REGISTER/CONTEN T	TYPE
Base + %00	Threshold register Ch. 0	Write only
Base + %02	Threshold register Ch. 1	Write only
Base + %04	Threshold register Ch. 2	Write only
Base + %06	Threshold register Ch. 3	Write only
Base + %08	Threshold register Ch. 4	Write only
Base + %0A	Threshold register Ch. 5	Write only
Base + %0C	Threshold register Ch. 6	Write only
Base + %0E	Threshold register Ch. 7	Write only
Base + %10	Threshold register Ch. 8	Write only
Base + %12	Threshold register Ch. 9	Write only
Base + %14	Threshold register Ch. 10	Write only
Base + %16	Threshold register Ch. 11	Write only
Base + %18	Threshold register Ch. 12	Write only
Base + %1A	Threshold register Ch. 13	Write only
Base + %1C	Threshold register Ch. 14	Write only
Base + %1E	Threshold register Ch. 15	Write only
Base + %40	Output width register Ch. 0 to 7	Write only
Base + %42	Output width register Ch. 8 to 15	Write only
Base + %48	Majority threshold register	Write only
Base + %4A	Pattern Inhibit register	Write only
Base + %4C	Test pulse register	Write only
Base + %FA	Fixed code	Read only
Base + %FC	Manufacturer & Module type	Read only
Base + %FE	Version & Serial number	Read only

3.2. Discriminator thresholds

(Base address + %00 to %1E write only)

These registers contain the discriminator thresholds values on 8 bit words. The thresholds values can be programmed in a range from -1 mV to -255 mV with 1 mV steps, writing an integer number between 1 and 255 into the register; the thresholds are individually settable.

3.3. Pattern of inhibit

(Base address + %4A write only)

This register contains the Pattern of Inhibit, a 16 bit word indicating which channels are either enabled or disabled (bit X=1 ⇒ Ch. X enabled…bitX=0 ⇒ Ch. X disabled).

3.4. Output width Ch. 0÷7

(Base address + %40 write only)

This register contains the output pulse width value of the channels 0 through 7 on a 8 bit word. This value can be adjusted in the range from 5 ns to 40 ns, writing an integer number between 0 and 255 into the register. The set value corresponds to the width as follows: 255 leads to a 40 ns pulse duration, 0 leads to a 5 ns pulse duration, with a non-linear relation for intermediate values

3.5. Output width Ch. 8÷15

(Base address + %42 write only)

This register contains the output pulse width value of the channels 8 through 15 on a 8 bit word. This value can be adjusted in the range from 5 ns to 40 ns, writing an integer number between 0 and 255 into the register. The set value corresponds to the width as follows: 255 leads to a 40 ns pulse duration, 0 leads to a 5 ns pulse duration, with a non-linear relation for intermediate values

3.6. Majority threshold

(Base address + %48 write only)

This register allows to set the Majority threshold between 1 and 16 for Internal Majority and between 1 and 20 for External Majority writing a proper value in the Base address + %48 (value range: 1÷244).
The Majority threshold can be calculated in the following way:

MAJTHR = NINT[(MAJLEV*50 –25)/4],

where NINT is the nearest integer function (allowed values for MAJLEV: 1 to 20) e.g.: if the desired Majority level is 5, the correct MAJTHR value to use is 56 (see also § 4.7).

3.7. Test pulse

(Base address + %4C write only)

A test pulse on all output channels can be generated by performing a write access at Base address + %4C; the test pulse is generated independently from the number written into this register.

3.8. Module identifier words

(Base address + %FA, + %FC, + %FE, read only)

Three words located at the Base address + %FA,+ %FC, + %FE of the page are used to identify the module, as shown in Fig. 3.1:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
Version				Module's serial number												Base + % FE
Manufacturer number						Module type										Base + % FC
%FA Fixed code								%F5 Fixed code								Base + % FA

Fig. 3.1: Module Identifier Words

The word located at the address Base + %FE identifies the single module via a serial number, and any change in the hardware will be shown by the version number .

For the Mod. V895 the word at the address Base + %FC has the following configuration:

Manufacturer N° = 000010 b
Type of module = 0001010100

4. Operating Modes

4.1. Test, Veto and Or signals

Some operations can be performed sending two external NIM signals:

- **TEST**: an input signal sent through this connector triggers all the enabled channels at once. This feature allows to check the module as well as to generate a pattern of pulses suitable to test any following electronics.
- **VETO**: (see Fig.2.1) an input signal sent through this connector allows to inhibit all channels simultaneously. Its leading edge must precede the input signal leading edge by at least 8 ns and overlap completely the input signal. It doesn't act on TEST input

> **Note:** TEST and VETO are high impedance inputs and each one is provided with two bridged connectors for daisy chaining (the chain has to be terminated on 50 Ohm on the last module)

- An **OR** output connector provides also the logical OR of the output channels. The relevant "OR" LED lights up if at least one of the enabled channels is over threshold.

4.2. Channel test

It is possible to test all channels in the following ways:

- sending a NIM pulse through one of the two "TEST" connectors located on the front panel.
- performing a write access to the + %4C base address (see § 3.8).

4.3. Threshold setting

Each V895 channel is provided with an 8 bit DAC to set the threshold. The threshold value can be programmed in a range from -1 mV to -255 mV with 1 mV steps (valid values: 1÷255).

Threshold for each channel can be set performing a write access to the Base addresses + %00 ÷ + %1E (see § 3.2).

4.4. Output pulse width setting

The output pulse width is adjustable from 5 to 40 ns. Two width values can be programmed: one for channels 0 through 7 and one for channels 8 through 15. Chosen value is set performing a write access to the following registers (see § 3.4 and § 3.5):

Base + %40	sets output width for channels 0 to 7
Base + %42	sets output width for channels 8 to 15

Valid data for the 8 bit registers are:

0	leads to	5 ns
…		
255	leads to	40 ns

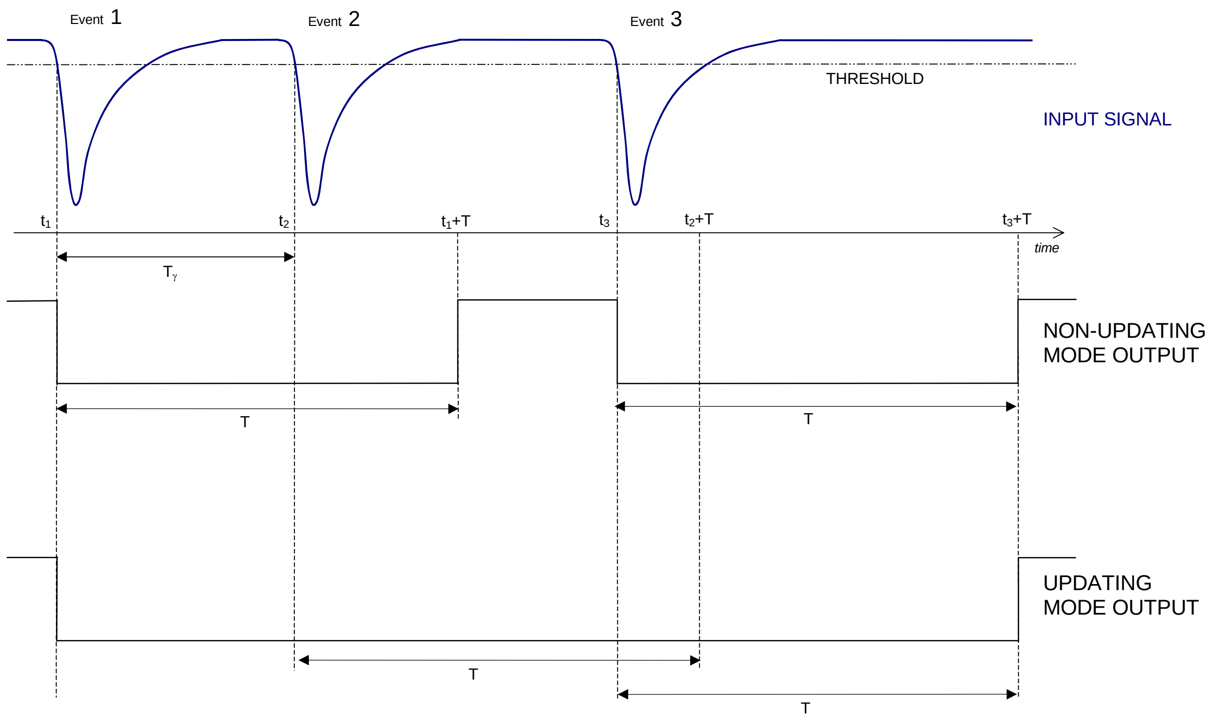
with a non-linear relation for intermediate values.

4.5. Updating and Non-Updating mode setting

Each channel of V895 may provide an Updated (retriggerable) or a Non-Updated (not retriggerable) output. Output mode selection is performed, individually for each channel, via jumpers as shown in Fig 2.2.

Non-Updating output mode: an input pulse over threshold occurring at t_1 (event 1 in fig. 4.1) sets the channel output active for the programmed duration T (T=5÷40 ns, see § 3.4). Any event over threshold occurring at t, with $t_1<t<t_1+T$, will be ignored.

Updating output mode: input pulse over threshold occurring at t_1 (event 1 in fig. 4.1) sets output active for the programmed duration T (T=5÷40 ns, see § 3.4). Any input event over threshold for $t_e<t_1+T$, will restart the pulse forming stage forcing the output to active value until instant t_e+T.



T	5÷40 ns	(programmable)
T_γ min	7ns Double Pulse Resolution (updating) 12ns Double Pulse Resolution (non-updating)	

Fig. 4.1: V895 Updating and Non-Updating mode

4.6. Current Sum signal

The **Current Sum (Σ)** output connector provides a current proportional to the input signal multiplicity, i.e. to the number of channels over threshold, at a rate of -1.0 mA per hit (-50 mV per hit into a 50 Ohm load) ±20%.

> **Note:** The Σ output requires a 50 Ohm termination for a correct operation of the Majority logic.

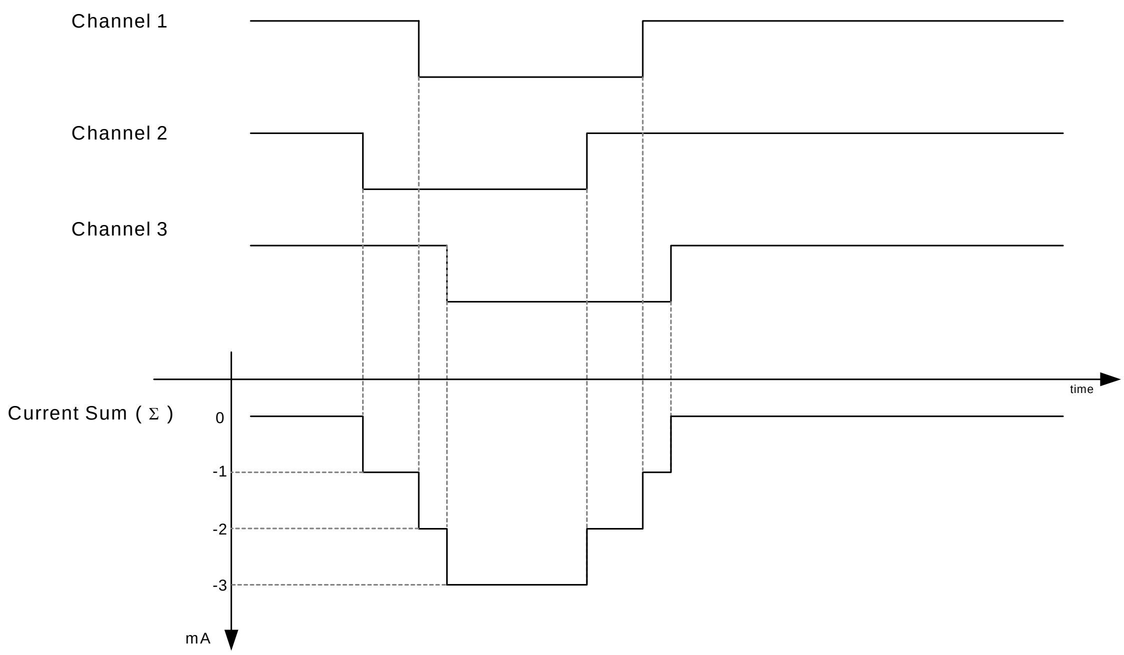


Fig. 4.2: Current Sum signal

4.7. Majority setting

Majority output provides a standard NIM signal if the number of channels over threshold exceeds the programmed majority level (MAJLEV). MAJLEV can be programmed between 1 and 16, writing a proper value (MAJTHR) in the Majority threshold register (see § 3.6); valid values range between 0 and 255. MAJTHR can be calculated in the following way:

MAJTHR = NINT[(MAJLEV*50 – 25)/4]

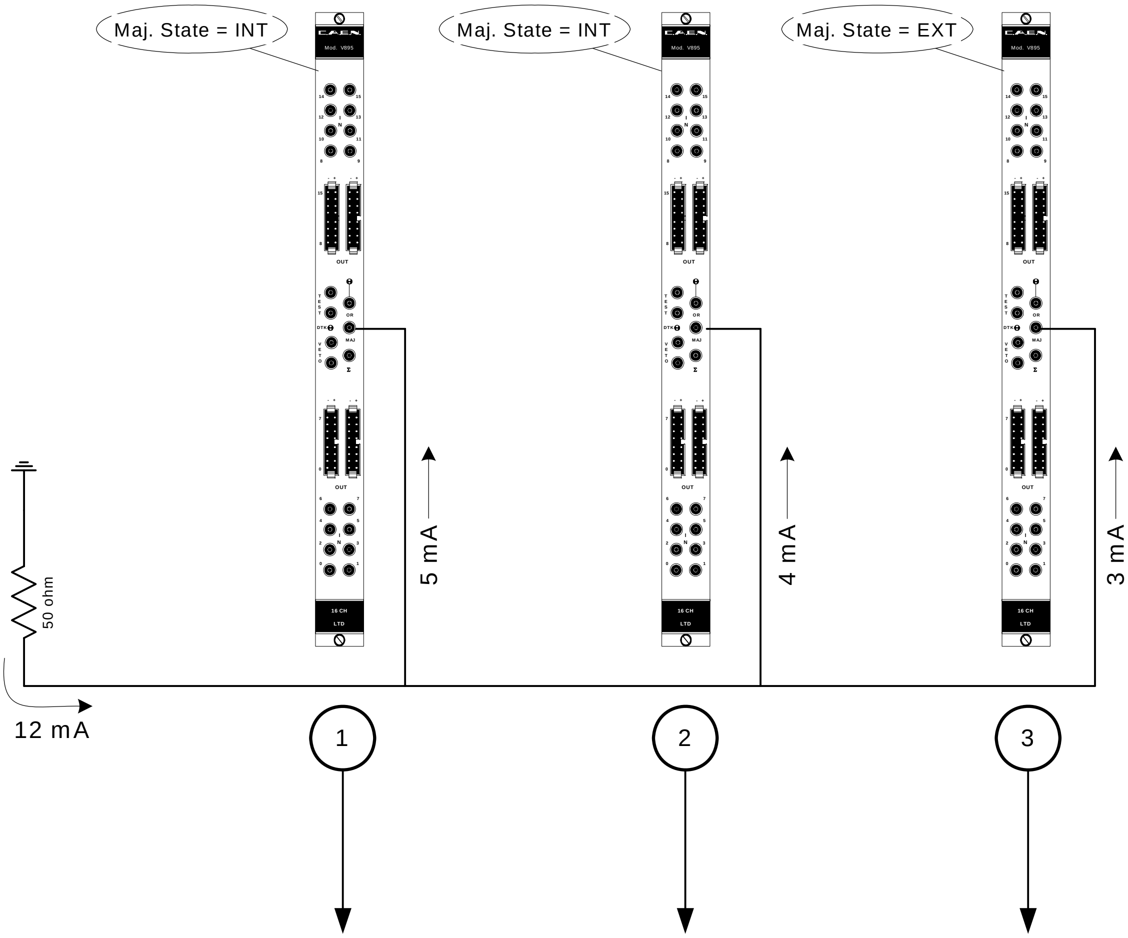
where NINT is the Nearest Integer.

MAJLEV	MAJTHR	MAJLEV	MAJTHR
1	6	11	131
2	19	12	144
3	31	13	156
4	44	14	169
5	56	15	181
6	69	16	194
7	81	17	206
8	94	18	219
9	106	19	231
10	119	20	244

Table 4.1: Majority Level setting values

The Majority logic can be switched from an "Internal" to an "External" position by means of an internal Jumper (see Fig. 2.3).

- **Internal**: With the jumper on the "Internal" position Majority output provides an active signal if the number of the active channels of the module exceeds or is equal to the programmed majority level (MAJLEV). In this case valid values of MAJLEV are from 1 to 16
- **External**: Several modules can be connected in daisy chain via the Σ outputs. In this case, by setting the Jumper to the "External" position, the Majority logic will act on the sum of the Σ outputs of the connected modules. The majority signal will be active if the sum of chained modules active channels exceeds the programmed MAJLEV. (An example with three chained modules is shown in Fig. 4.3). The Σ output line must be terminated with 50 Ohm.



Module Number	1	2	3
Majority State	INT	INT	EXT
Majority Level (MAJLEV)	2 (referred to internal over th. channel)	5 (referred to internal over th. channel)	10 (referred to all over th. channels)
Number of Module's active Channels	5	4	3
Majority Output	ACTIVE (5 > MAJLEV)	NON Active (4 < MAJLEV)	ACTIVE (5+4+3 > MAJLEV)

Fig. 4.3: Example of three daisy chained V895