PRELIMINARY

Data Sheet

Revision n. 0
5 November 2001

MOD. V890

128 CHANNEL
MULTIHIT TDC

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1. General description

1.1 Overview

The Model V890 is a 1-unit wide VME 6U module that houses 128 independent Multi-Hit/Multi-Event Time to Digital Conversion channels. The channels feature dead time rejection. The unit houses 4 TDC chips, developed by CERN/ECP-MIC Division, thus called from now on the CERN/ECP-MIC TDCs. Resolution can be set at 100, 200 or 800 ps with a 17, 19, or 20 bit dynamics respectively.

The CERN/ECP-MIC TDC is a General Purpose time-to-digital converter, with 32 channels per chip. All channels can be enabled to the detection of rising and/or falling edges (i.e. the edges' timing, as well as the hit width, can be measured with the selected resolution) and for each channel there is a digital adjust for the zero-ing of any offsets and pedestals.

Two different versions are available: the **Mod. V890AA** and the **Mod. V890AB**. The two versions differ for the JAUX connector for the CERN V430 VMEbus crate: the Mod. V890AA uses the P1, P2 VME connectors and the JAUX connector, while the Mod. V890AB has only the P1 and P2 VME connectors. ECL inputs are featured and LVDS inputs are available on request.

The data acquisition can be programmed in "EVENTS" (“TRIGGER MATCHING MODE” with a programmable time window) or in "CONTINUOUS STORAGE MODE".

The board houses a 32 kwords deep Output Buffer (expandable), that can be readout via VME (as single data, Block Transfer and Chained Block Transfer) in a completely independent way from the acquisition itself.

The module programming is performed via a microcontroller that implements a high-level user interface in order to mask the board and the TDCs' hardware.

The V890AA Model uses the P1 and P2 connectors of VME and the auxiliary connector for the CERN V430 VMEbus crate (Jaux Dataway).

The V890AB Model uses the P1 and P2 connectors of VME only (i.e. it does not have the auxiliary connector for the CERN V430 VMEbus crate) and consequently hosts a DC-DC converter for the -5V power supply.

The VME interface allows the module to work in A24 and A32 addressing modes.
The internal registers are available in D16 mode only, while the data buffer is available in D32, BLT32 or MBLT64. The module supports also the Chained Block Transfer mechanism (CBLT) and the Multicast commands (MCST). Geographical address is also available.

1.2 Block Diagram

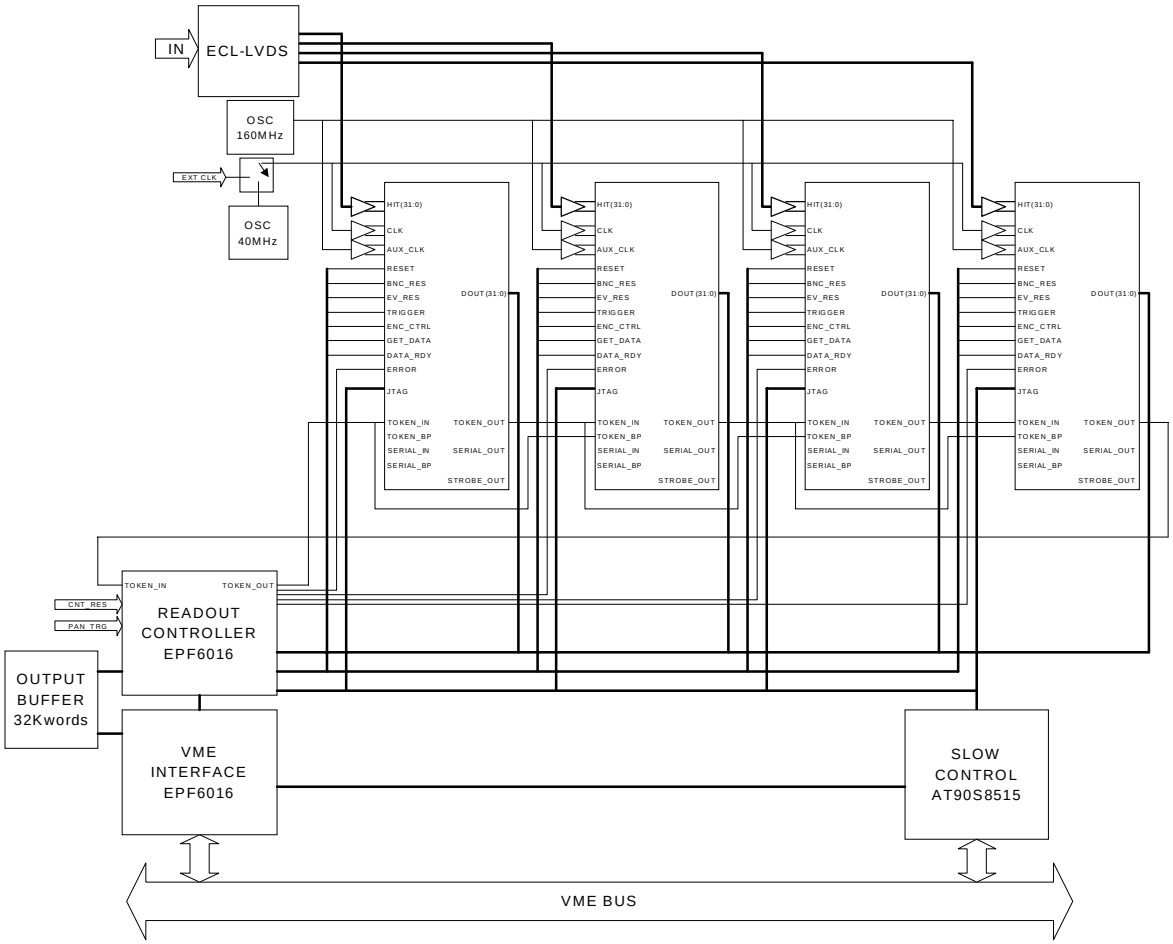

Fig. 1.1: Mod. V890 Block Diagram

2. Technical specifications

2.1 Packaging

The Model V890 is housed in a 6U-high, 1U-wide VME unit. The board hosts the VME P1, P2 connectors and, depending on the version, the PAUX connector.
The version equipped with the PAUX connector (**V890AA**) requires the VME V430 backplane.

2.2 Front Panel

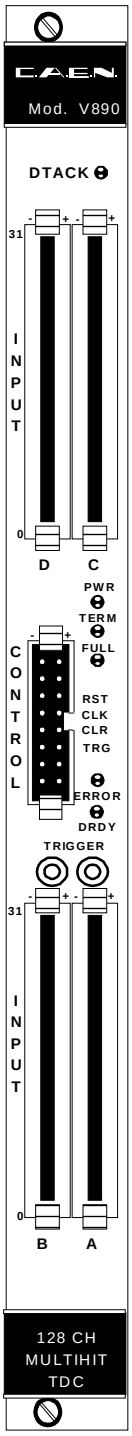

Fig. 2.1: Model V890 front panel

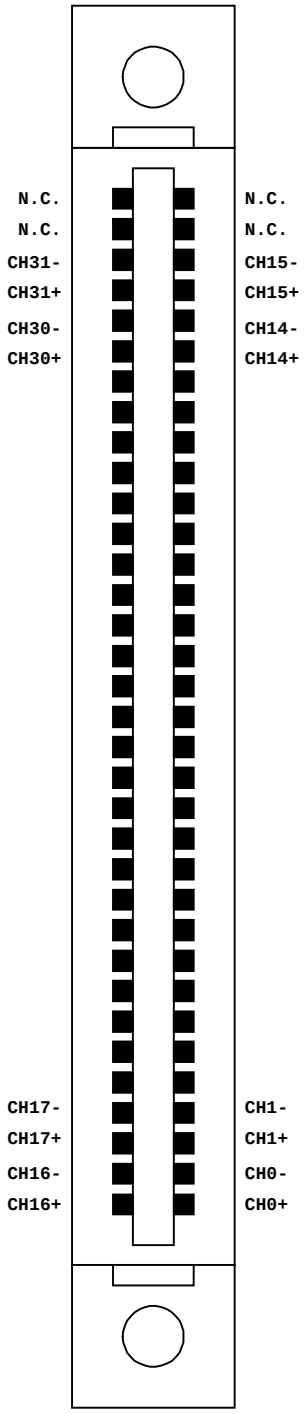

Fig. 2.2: INPUT connector pin assignment

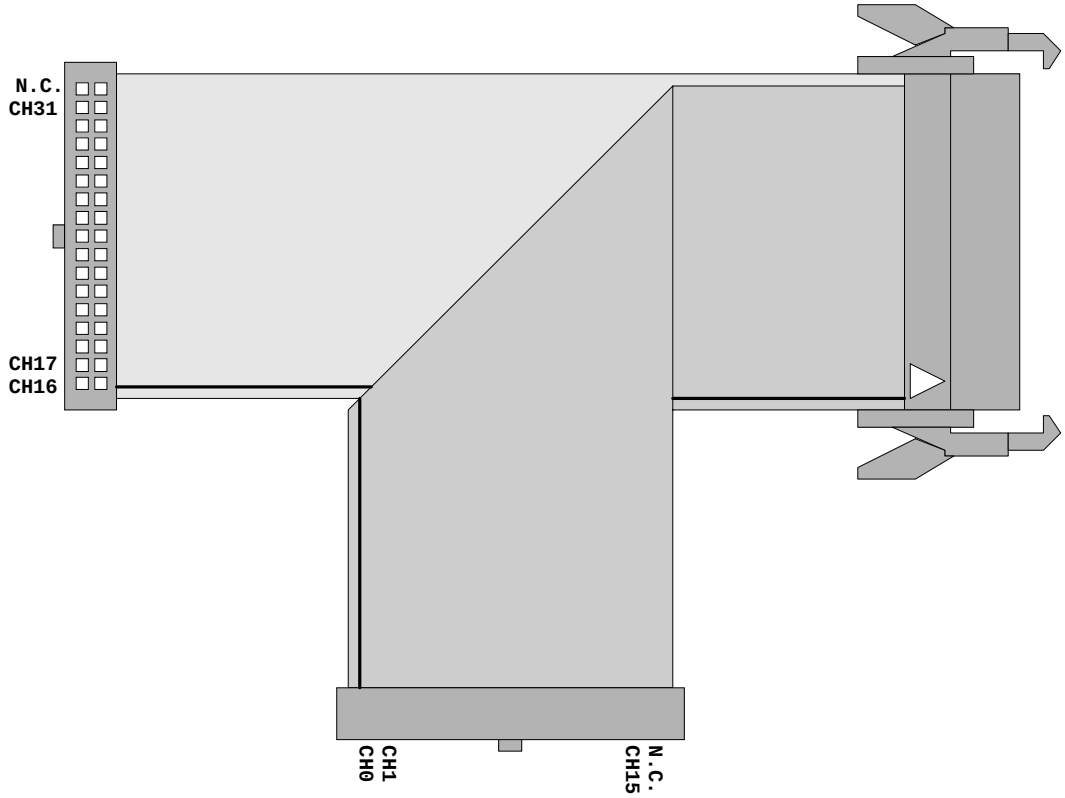

Fig. 2.3: INPUT connector cabling

2.3 External connectors

The location of the connectors is shown in Fig. 2.1.Their function and electro-mechanical specifications are listed in the following subsections.

2.3.1 INPUT connectors

Mechanical specifications:
N. 4 connectors, Robinson Nugent P50E-068-P1-SR1-TG type, (34+34) pins; for the 128 single channel inputs.
Connector A refers to Channels 0 to 31.
Connector B refers to Channels 32 to 63.
Connector C refers to Channels 64 to 95.
Connector D refers to Channels 96 to 127.
Electrical specifications:
ECL input signals, 110 Ω impedance. The 17th higher pair of pins of each connector is not connected.

2.3.2 CONTROL connector

Mechanical specifications:
two 8+8-pin, 3M 3408-5202 Header-type connectors.

- CLOCK: Rising-edge active, differential ECL level, 110 Ω; min. width 25 ns.
- TRIGGER: Rising-edge active, differential ECL level, 110 Ω; min. width 25 ns
- CLR: Active high, differential ECL level, 110 Ω impedance; min. width 25 ns.
- OUT_PROG: Active high, differential ECL level, 110 Ω impedance; min. width 25 ns.
- RESET: Active high, differential ECL level, 110 Ω impedance; min. width 25 ns.

Pin assignment is shown in Fig. 2.4.

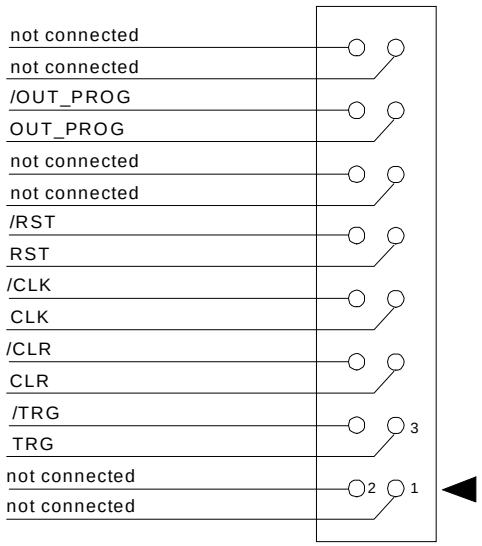

Fig. 2.4: CONTROL connector pin assignment

2.3.3 EXTERNAL TRIGGER connectors

Mechanical specifications:
two 00-type LEMO connectors (bridged).
Electrical specifications:
Rising-edge active, NIM, 110 Ω; min. width 25 ns

2.4 Other front panel components

2.4.1 Displays

The front panel (refer to Fig. 2.1) hosts the following LEDs:

DTACK: *Colour:* green.

Function: it lights up green whenever a VME read/write access to the board is performed.

PWR: *Colour:* green/red.
Function: it lights up green when the board is inserted into the crate and the crate is powered up; when it is red, it indicates that there is an over-current status: in this case, remove the overload source, switch the module off and then switch it on again.

TERM: *Colour:* green/orange.
Function: it lights up green when all the lines of the control bus are terminated, it also lights up orange for a while at power ON to indicate that the board is configuring.

FULL: *Colour:* red.
Function: it lights up when the Multi-Event Buffer is full; it also lights up for a while at power ON to indicate that the board is configuring.

ERROR: *Colour:* red.
Function: it lights up to signal a TDC global error.

DRDY: *Colour:* yellow.
Function: it lights up when at least one event is present in the output buffer; it also lights up for a while at power ON to indicate that the board is configuring.

2.5 Internal hardware components

The V890 module is constituted by a motherboard with a piggy-back board plugged into it. In the following some hardware setting components, located on the boards, are listed. See Fig. 2.5 for their exact location on the PCB and their settings.

2.5.1 Switches

ROTARY SWITCHES: *Type:* 4 rotary switches.
Function: they allow to select the VME address of the module. See Fig. 2.5 for their location.

SW1: *Type:* DIP switch.
Function: it allows the hardware termination (if enabled) of the Control Bus on 110 Ω

Right position (dot visible): Control Bus not terminated;

Left position (dot not visible): Control Bus terminated.

SW2: *Type:* DIP switch.
Function: it allows to switch from/to internal/external clock

Right position (dot visible): internal clock;

Left position (dot not visible): external clock.

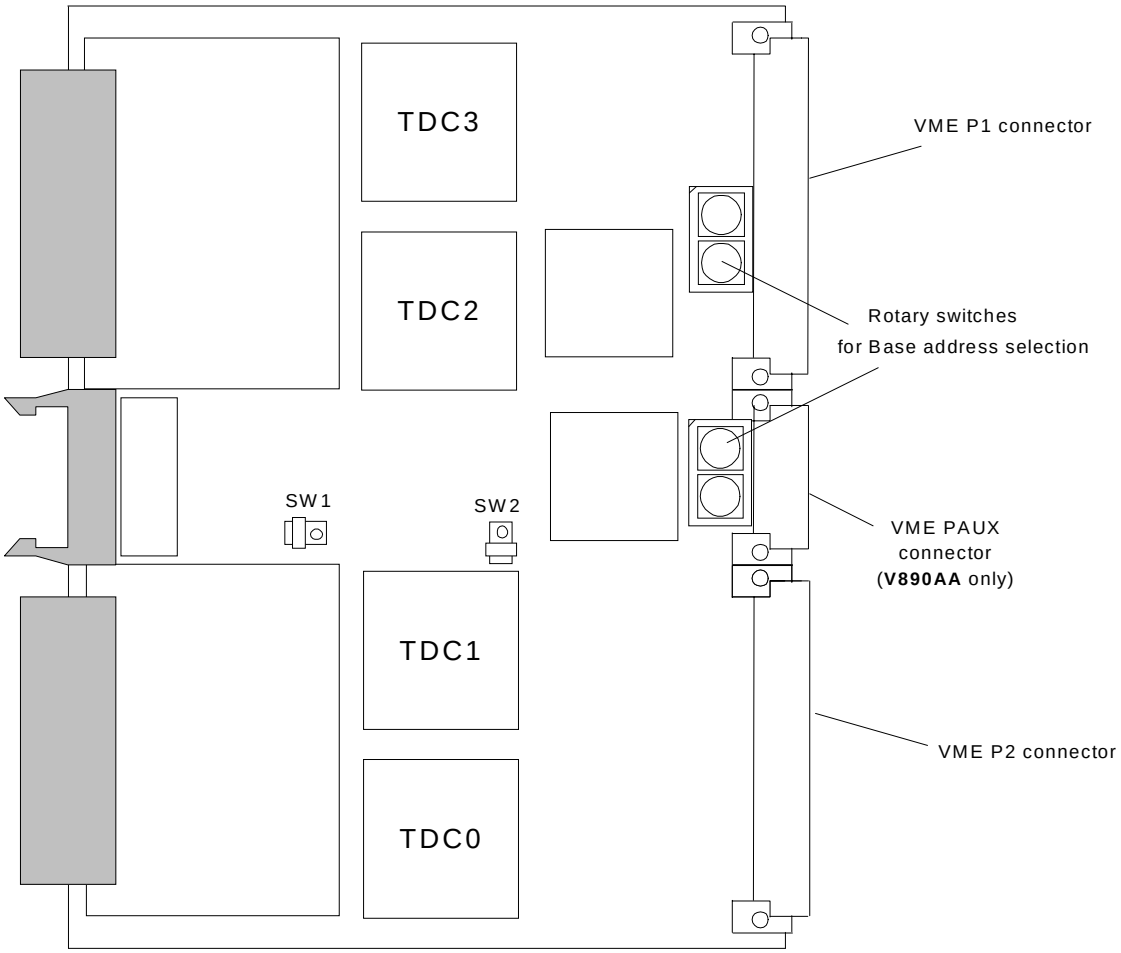

Fig. 2.5: Component Location (component side)

2.6 Technical specifications table

Table 2.1 : Model V890 technical specifications

Packaging	6U-high, 1U-wide VME unit (version AA requires the V430 backplane)
Inputs	128 ECL (LVDS also available) inputs, 110 Ω impedance
Acquisition modes	Trigger Matching Mode; Continuous Storage Mode
Built-in memory	32 kwords deep Output Buffer (expandable)
Resolution/Input dynamics	800 ps→17 bit 200 ps→19 bit 100 ps→20 bit
EXT TRIGGER input	Two LEMO 00 bridged connectors, ECL signal, 110 Ω
Double pulse resolution	4 ns
Clock source	Internal (40 MHz) or External (on *Control* connector), dip switch selectable
Control inputs	active-high, differential ECL input signals: RST: resets Output Buffer, Status and Control registers. CLR: FAST CLEAR of TAC sections rising-edge active, differential ECL input signals: CLK: external clock TRG: trigger for the TDC latching
Control outputs	differential ECL output signal: OUT_PROG: control output signal, programmable via the *out prog control* register
Displays	DTACK: green LED; lights up at each VME access. PWR: green/red LED; green: power ON, red: failure status. TERM: green LED; control bus termination ON. FULL: red LED; memory full. ERROR: red LED; TDC global error. DRDY: yellow LED; at least one datum in the output buffer
VME	*Addressing modes*: A24, A32, MCST *Data transfer modes*: D16, D32, BLT32, BLT64, CBLT *Readout rate*: 10 MHz