TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1. DESCRIPTION

1.1. FUNCTIONAL DESCRIPTION

The model V512 is a 1-unit wide VME module; it is an 8 Channels 4 Fold AND/OR Programmable Logic Unit.

Each of the 8 channels has four inputs A, B, C, D and the channel output have a fan-out of 2.

The four inputs of each channel are divided into two couples (A,B) and (C,D), via VME it is possible to program an AND/OR logic function independently for each couple:

- $\mathscr{F}_0$(A,B) and $\mathscr{F}_1$(C,D) (First Level Logic).

Via VME it is also programmable an AND/OR logic function on the two resulting signals:

- $\mathscr{F}_2(\mathscr{F}_0,\mathscr{F}_1)$ (Second Level Logic)

The output obtained has a fan-out of 2.

The outputs of the First Level Logic are combined to obtain two OR signals OR0 and OR1 that are the logical OR of the First Level Logic of channel<0..3> and channel<4..7> respectively. Through internal jumpers it is possible to obtain a general OR of the First Level Logic signals with a fan-out of two.

The 8 channel outputs are inhibited by means of an external VETO signal or via VME; the OR0 and OR1 outputs are never inhibited.

The VETO input is high impedance and is provided with two bridge connectors for daisy chaining.

The channels' logic diagram is shown in fig 1.1.

The module houses a fully programmable VME ROAK INTERRUPTER[1] that generates a VME interrupt (if enabled) whenever one of the two OR signals becomes true.

The module V512 is an A24/A32 D16 VME slave; its Base address is fixed by 6 internal rotary switches. A front panel LED (DTACK) lights up each time the module generates the VME signal DTACK.

The Model uses the P1 and P2 connector of VME and the auxiliary connector for the backplane of the CERN V430[2] VMEbus crate (Jaux Dataway).

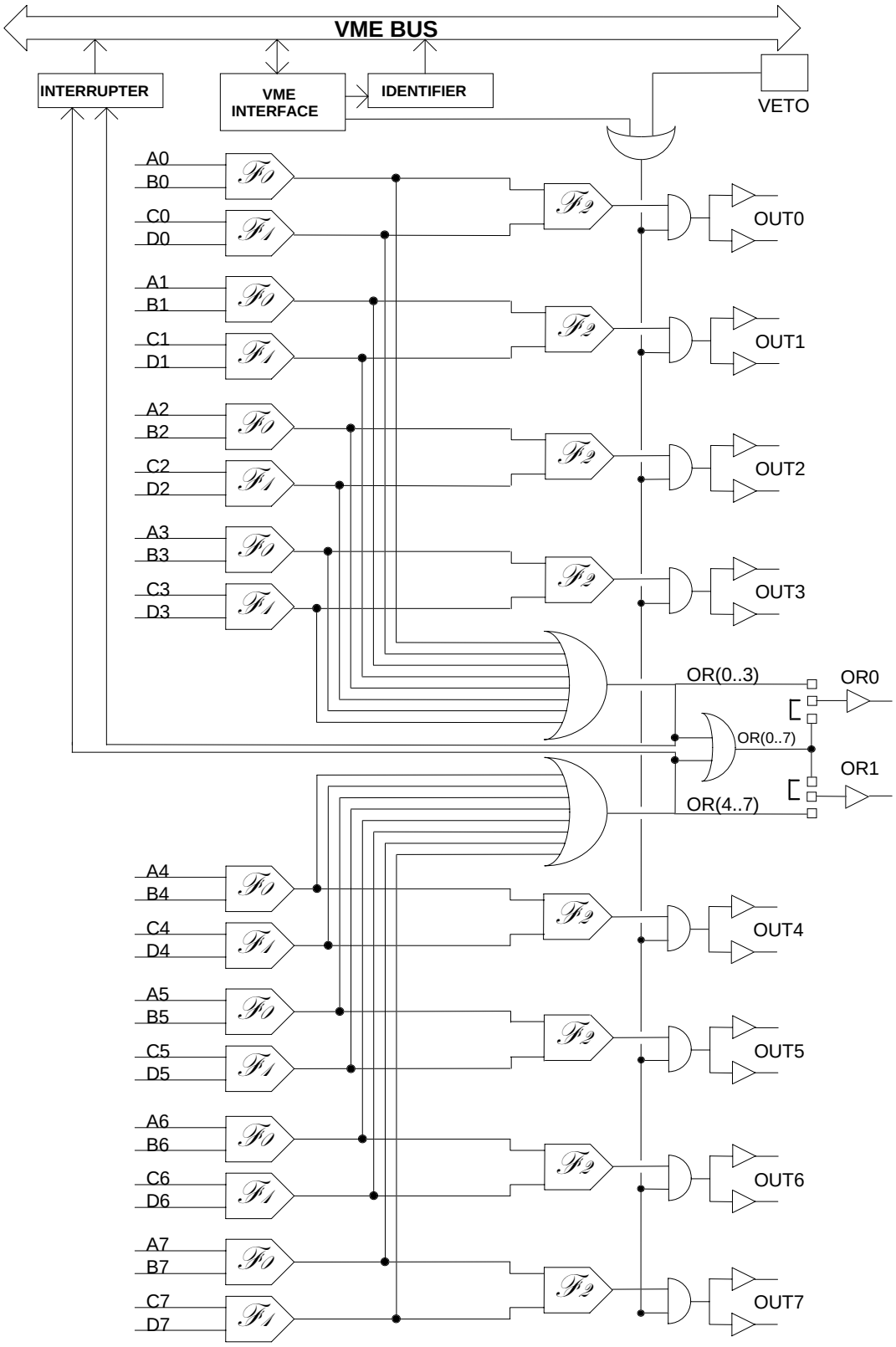

Fig. 1.1: Mod. V512 Block Diagram

2. SPECIFICATIONS

2.1. PACKAGING

1-unit wide VME unit. Height: 6U.

2.2. EXTERNAL COMPONENTS

CONNECTORS

- No.2, "IN A..B","IN C..D", Condo header, 3M 3408-D203 type connector, 2x(8+8) pins 110Ω impedance; for the 32 input channels.

- No.2, "OUT", Condo header, 3M 3408-D203 type connector, 2x(8+8) pins 110Ω impedance; for the 8x2 output signals.

- No.1, "OR 0..3", LEMO 00 type, 50Ω impedance;

- No.1, "OR 4..7", LEMO 00 type, 50Ω impedance;

- No.2, "VETO", LEMO 00 type 50Ω impedance; two bridge connectors (for daisy chaining) for the VETO input signal.

LEDs

- No.1, "DTACK", green; VME Selected; it lights up during a VME access.

- No.1, "OR AB", red; signalling when aligth that $\mathscr{F}_0$ = OR.

- No.1, "OR CD", red; signalling when aligth that $\mathscr{F}_1$ = OR.

- No.1, "OR AB-CD", red; signalling when aligth that $\mathscr{F}_2$ = OR.

- No.1, "AND AB", red; signalling when aligth that $\mathscr{F}_0$ = AND.

- No.1, "AND CD", red; signalling when aligth that $\mathscr{F}_1$ = AND.

- No.1, "AND AB-CD", red; signalling when aligth that $\mathscr{F}_2$ = AND.

- No.1, "OR 0..7", red; signalling when aligth that on the two OR outputs is available the general OR of the First Level Logic OR(0..7).

2.3. INTERNAL COMPONENTS

(refer to fig.2.2 and Appendix B - components location)

SWITCHES

- No.2, changeover switches "JP2..JP3". For the OR selection.

- No.6, rotary switches for the module VME Base address selection.

2.4. POWER REQUIREMENTS

+ 5 V	500 mA
- 2 V	300 mA
- 5 V	1.1 A

2.5. CHARACTERISTICS OF THE SIGNALS

INPUT CHANNELS:	std. differential ECL level, 110 Ω impedance;		
MAXIMUM RATE (duty cycle 50%):	Outputs(1): 150 MHz ; OR (Local mode 4 channels)(2): 150 MHz OR (General mode 8 channels)(3): 80 MHz		
MINIMUM WIDTH:	Outputs(1): 3 ns; OR (Local mode 4 channels)(2): 3 ns OR (General mode 8 channels)(3): 7 ns		
VETO(4):	std. NIM level, high impedance; must overlap the coincidence of the inputs by >2ns.		
OUTPUTS:	std. differential ECL level, capable of driving differential 110 Ω loads.		
OR OUTPUTS:	std. NIM logic levels on 50 Ω impedance.		
DOUBLE PULSE RESOLUTION:(5)	7 ns at minimum input width;		
COINCIDENCE WIDTH:	> 2.5 ns determined by input pulse width		
INPUT-OUTPUT DELAY:	min. 3.5 ns	max. 5.6 ns	
INPUT- OR DELAY:	(Local mode 4 ch.) (General mode 8 ch.)	min. 4.20 ns min. 5 ns	max. 6.8 ns max. 13.7 ns

(1) The measurement for maximum rate and minimum width for the Outputs is made by applying pulses to one of the 4 inputs with the three logic functions $\mathscr{F}_0$, $\mathscr{F}_1$, $\mathscr{F}_2$ set to the OR mode .

(2) The measurement for maximum rate and minimum width for the OR outputs in Local mode is made by applying pulses to one of the 16 inputs with OR0 = OR(0..3) and OR1 = OR(4..7).

(3) The measurement for maximum rate and minimum width for the OR outputs in General Mode is made by applying pulses to one of the 32 inputs with OR0 = OR1= OR(0..7).

(4) This input is high impedance and is provided with two bridge connectors for daisy chaining. Note that the high impedance makes this input sensitive to noise, so the chains have to be terminated on 50 Ω on the last module; the same is needed also if one module only is used, whose input has thus to be properly matched.

(5) The DPR measurements are obtained with the three logic functions $\mathscr{F}_0$, $\mathscr{F}_1$, $\mathscr{F}_2$ set to the OR mode and feeding two pulses from different cables into two of the four inputs.

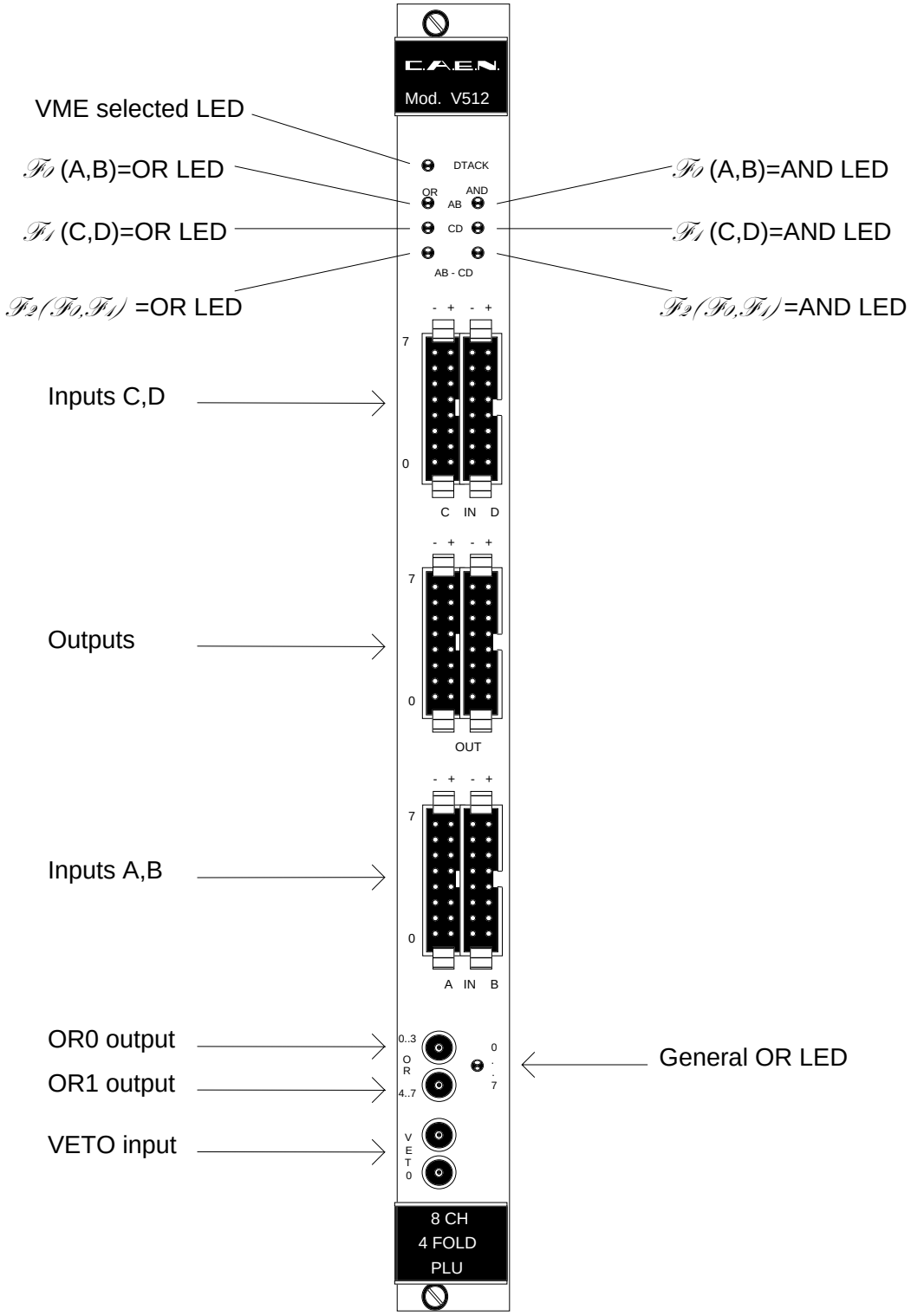

Fig. 2.1: Mod. V512 Front Panel

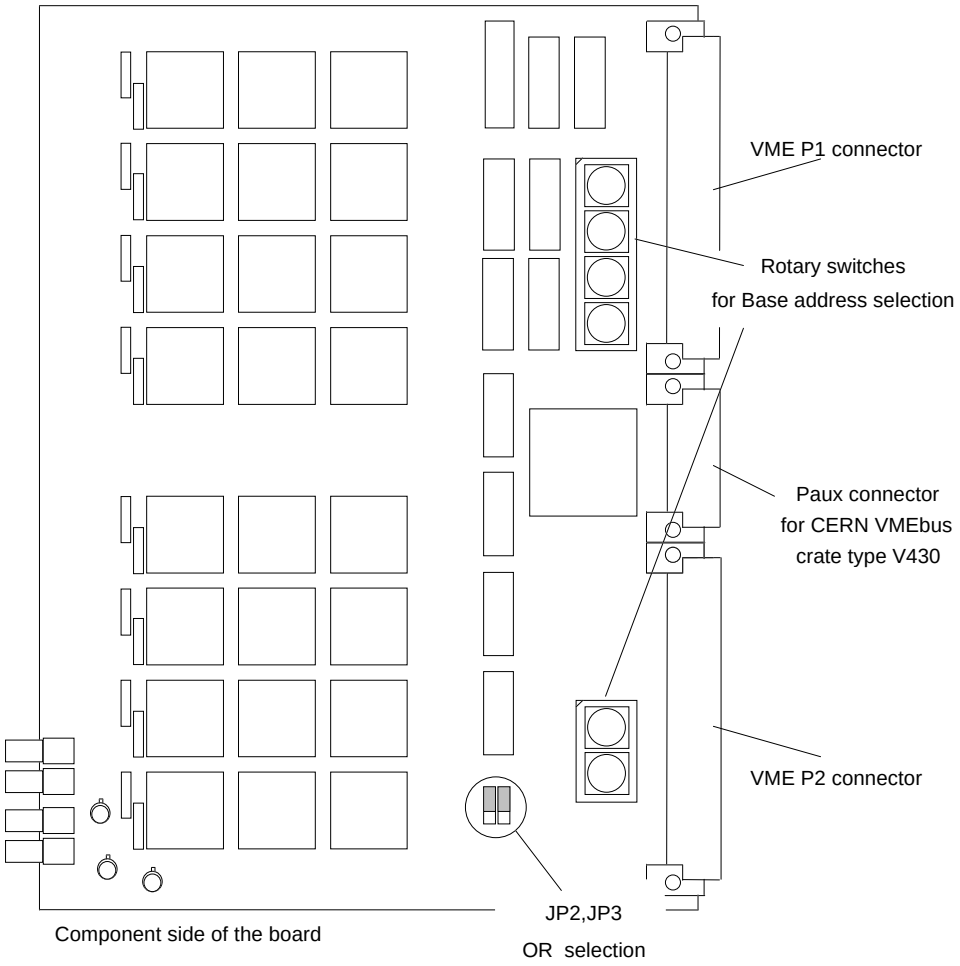

Fig. 2.2: Mod. V512 Components Locations

3. OPERATING MODES

3.1. CHANNEL OPERATION

The Mod. V512 is a 8 Channels 4 Fold AND/OR Programmable Logic Unit.

Each channel has four inputs A,B,C,D and one output with a fan-out of 2.

All inputs accept differential ECL levels into 110 Ω input impedance.

The four inputs of each channel are divided into two couples (A,B) and (C,D), the output is a Boolean function of the 4 inputs and has the following expression:

- OUT = $\mathscr{F}_2(\mathscr{F}_0(A,B),\mathscr{F}_1(C,D))$.

$\mathscr{F}_0$, $\mathscr{F}_1$, $\mathscr{F}_2$ are logic functions that are common for all the V512 channels.

Via VME it is possible to program an AND/OR logic function independently for $\mathscr{F}_0$, $\mathscr{F}_1$, $\mathscr{F}_2$. The 3 LSB of the Function register (Base address + %10) control the choice of the Boolean functions:

- Function register <n> =0 $\mathscr{F}_n$ = AND;
- Function register <n> =1 $\mathscr{F}_n$ = OR.

For example, if $\mathscr{F}_0$ = AND (∗), $\mathscr{F}_1$ = OR (+) and $\mathscr{F}_2$ = AND (∗) the output of the channel i is:

- $OUT_i = (A_i * B_i) * (C_i + D_i)$.

The VME VETO or the external VETO signal inhibits the outputs regardless of the state of the four inputs.

3.2. OR OUTPUTS

The first stages of the Boolean function of the channels $\mathcal{F}_i$(A,B), $\mathcal{F}_i$(C,D) (first level logic), are combined to obtain two OR signals OR0 and OR1. The jumpers JP2 and JP3 control the OR generation (see fig. 3.1).

$$OR0 = OR(0..3) = \sum_{i=0}^{3} \mathcal{F}_i(A, B) + \sum_{i=0}^{3} \mathcal{F}_i(C, D)$$

(JP2 and JP3: Local OR position);

$$OR1 = OR(4..7) = \sum_{i=4}^{7} \mathcal{F}_i(A, B) + \sum_{i=4}^{7} \mathcal{F}_i(C, D)$$

(JP2 and JP3: Local OR position);

$$OR0 = OR1 = OR(0..7) = \sum_{i=0}^{7} \mathcal{F}_i(A, B) + \sum_{i=0}^{7} \mathcal{F}_i(C, D)$$

(JP2 and JP3: General OR position).

The OR0 and OR1 output are never inhibited.

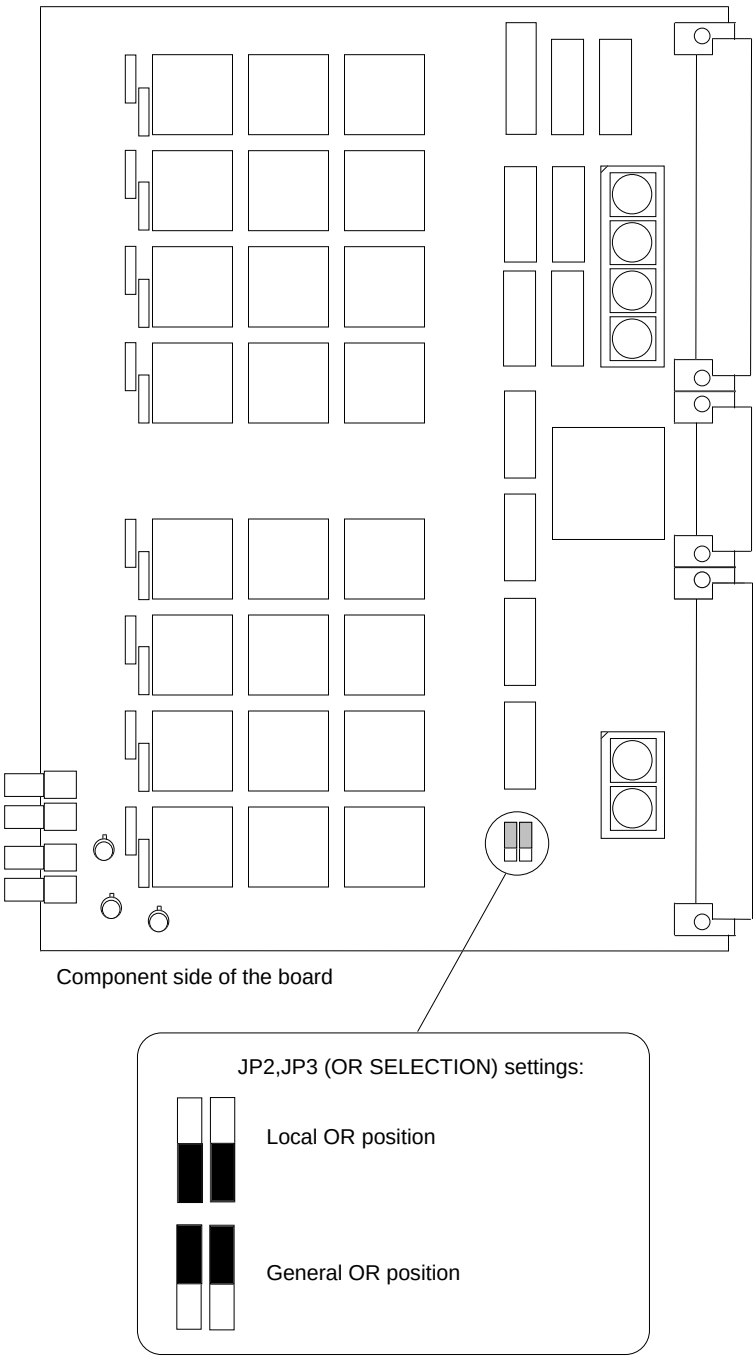

Fig. 3.1: Mod. V512 JP2, JP3 settings

3.3. OUTPUTS INHIBIT

It is possible to inhibit the outputs regardless of the state of the four inputs in this way:

- by sending a NIM signal through one of the two "VETO" connectors located on the front panel;
- by setting the VME VETO (bit 3 of the Function register =1). The register is available at VME address Base +%10.

The VETO input is high impedance and is provided with two bridge connectors for daisy chaining.

Note that the high impedance makes this input sensitive to noise, so the chain has to be terminated on 50 ohm on the last module; the same is needed also if one module only is used, whose input has thus to be properly matched.

3.4. INTERRUPT GENERATION

The operations of the V512 VME INTERRUPTER are fully software programmable; via VME it is possible:

- to enable /disable the VME interrupt generation;
- to set the VME interrupt level;
- to program the VME interrupt vector (STATUS/ID).

If the VME INTERRUPTER is enabled, it generates a VME interrupt whenever one of the two OR signal becomes true.

3.5. V430 BACKPLANE

The model V512 requires the backplane of the VMEbus crates type V430 [2] because it make intensive use of ECL integrated circuits that need - 5.2 V and - 2V powers..

This backplane (VMEbus BIN type V431, see [2] § 2) is a monolithic printed circuit board that provides the VMEbus standard J1 and J2 dataway and a third dataway (named "Jaux") which is not foreseen by the VME standard.

The Jaux dataway provides some signals, the -5.2 V and -2 V requested by fast ECL logic front end modules and the +15 V and -15 V rails. This dataway is situated in the free space available between J1 and J2.

4. VME INTERFACE

4.1. ADDRESSING CAPABILITY

The module works in A32/A24 mode. This means that the module address must be specified in a field of 32 or 24 bits. The Address Modifiers code recognized by the module are:

AM=%39:	standard user data access
AM=%3D:	standard supervisor data access
AM=%09:	extended user data access
AM=%0D:	extended supervisor program access

The module's Base Address is fixed by 6 internal rotary switches housed on two piggy-back boards plugged into the main printed circuit board (see Fig. 4.1).

The Base Address can be selected in the range:

% 00 0000 <-> % FF FF00 A24 mode

% 0000 0000 <->% FFFF FF00 A32 mode

The Base Address reserves in this way a page of 256 bytes for the module. The address map of the page is shown in table 4.1.

4.2. DATA TRANSFER CAPABILITY

The V512 registers are accessible in D16 mode;

Table 4.1: Address Map for the Mod. V512

ADDRESS	REGISTER/CONTENT	TYPE
Base + %FE	Version & Series	read only
Base + %FC	Manufacturer & Module Type	read only
Base + %FA	Fixed code	read only
Base + %12...Base + %F8	Reserved	
Base + %10	Function register	read/write
Base + %08..Base + %0E	Reserved	
Base + %06	Interrupt Enable register	read/write
Base + %04	Reserved	
Base + %02	Interrupt Level register	read/write
Base + %00	Interrupt Vector register	read/write

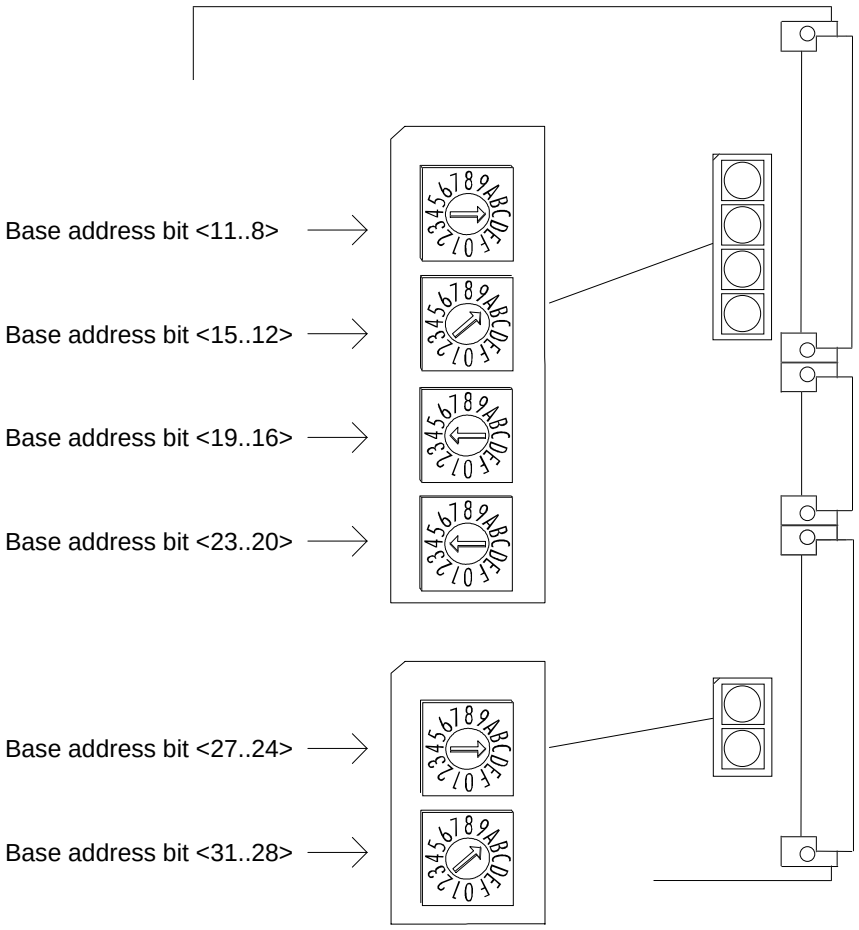

Fig. 4.1: Mod. V512 Base address setting

4.3. MODULE IDENTIFIER WORDS

(Base address + %FA ,+%FC, +%FE read only)

The Three words located at the highest address on the page are used to identify the module as shown in figure 4.1:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
Version				Module's serial number												Base + % FE
Manufacturer number						Module type										Base + % FC
%FA Fixed code								%F5 Fixed code								Base + % FA

Fig. 4.2: Module identifier words

At the address Base + % FA the two particular bytes allow the automatic localization of the module.

For the Mod. V512 the word at address Base + % FC has the following configuration:

Manufacturer N°= 000010 b

Type of module = 0000011010 b

The word located at the address Base + %FE identifies the single module via the module's serial number and any change in the hardware, (for example the use of faster logic) will be shown by the Version number.

4.4. FUNCTION REGISTER

(Base address + %10 r/w)

This register allows to control the channel operations:

The 3 LSB are dedicated to the Boolean function $\mathscr{F}_0$, $\mathscr{F}_1$, $\mathscr{F}_2$:

- Function register <n> = 0 $\mathscr{F}_n$ = AND;
- Function register <n> = 1 $\mathscr{F}_n$ = OR.

The fourth bit allows to set the VME VETO:

- Function register <3> = 1 VME VETO active: the outputs are disabled.

The following figure shows the structure of the Function register.

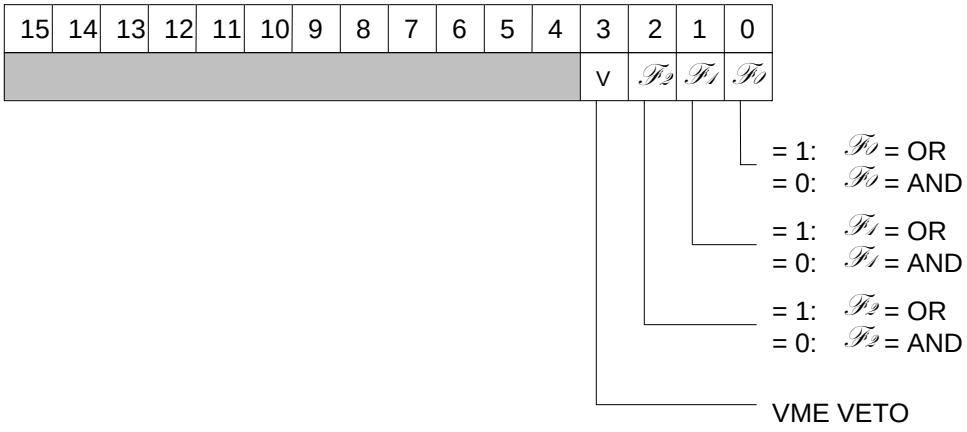

Fig. 4.3: Function Register

4.5. INTERRUPT ENABLE REGISTER

(Base address + % 06 r/w)

This 1 bit register allows to enable/disable the interrupt generation:

- Interrupt Enable register <0> = 0 Interrupt disabled;.
- Interrupt Enable register <0> = 1 Interrupt enabled;.

A VME access (read or write) to the address Base +% 0A disables the VME interrupt generation.

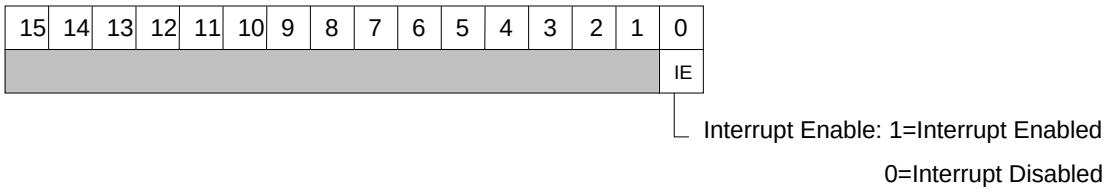

Fig. 4.4: Interrupt Enable Register

4.6. INTERRUPT LEVEL REGISTER

(Base address + %02 r/w)

The 3 LSB of this register contain the value of the interrupt level. (Bits <15..3> are unused and are read as "one" on the VME data bus).

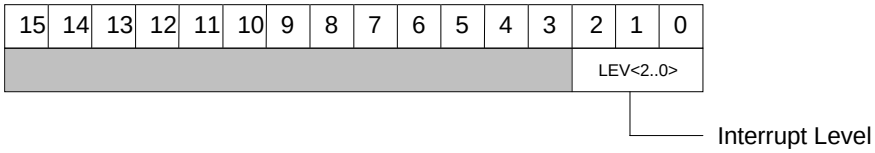

Fig. 4.5: Interrupt Level Register

4.7. INTERRUPT VECTOR REGISTER

(Base address + %00 r/w)

The value stored in this register is the STATUS/ID that the V512 INTERRUPTER places on the VME data bus during the interrupt acknowledge cycle. (Bits 8 to 15 are unused and are read as "one" on the VME data bus).

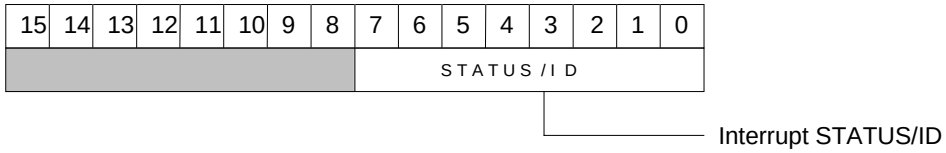

Fig. 4.6: Interrupt Vector Register

5. MOD. V512 INTERRUPTER

5.1. INTERRUPTER CAPABILITY

The V512 Module houses a VME ROAK INTERRUPTER D08(o) type[1].This means that:

- it responds to 8 bit, 16 bit and 32 bit interrupt acknowledge cycles providing an 8-bit STATUS/ID on the VME data lines D00..D07;
- it removes its interrupt request when the VME Master reads the V512 STATUS/ID during the Interrupt Acknowledge Cycle (ROAK: Release On Acknowledge).

5.2. INTERRUPT LEVEL

The interrupt level corresponds to the value stored in the Interrupt Level register <2..0>. the register is available at the VME address Base + % 02.

5.3. INTERRUPT STATUS/ID

The interrupt STATUS/ID is 8 bit wide, and it is contained in the Interrupt Vector register<7..0> (address Base + % 00).

5.4. ENABLE/DISABLE INTERRUPT GENERATION

It is possible to enable/disable the Mod. V512 interrupt generation in the following way:

- enable: by setting the Interrupt Enable register <0> to 1 (Base address + %06);
- disable: by setting the Interrupt Enable register <0> to 0 (Base address + %06).

5.5. INTERRUPT SEQUENCE

If the VME interrupt generation is enabled (Interrupt Enable register<0>=1):

{

- if OR0 or OR1 becomes true and the value of the interrupt level is different from 0:

    {

    - It requests interrupt by driving an interrupt request line IRQ1..7 low according to the Interrupt Level register <2..0> value;

    - during the following acknowledge cycle it places on the VME data lines D00..D07 the STATUS/ID; it is the byte contained in the 8 LSB of the Interrupt vector register;

    }

- if OR0 and OR1 are not active;

    {

    - it releases its VME interrupt request line during the acknowledge cycle;.

    }

else

    {

    it repeats the interrupt request action.

    }

}

6. REFERENCES

[1] VMEbus Specification Manual Revision C.1 October 1985

[2] G. Bianchetti et al., Specification for VMEbus CRATE Type V430, CERN-EP, January 1990.

APPENDIX A: ELECTRICAL DIAGRAMS

APPENDIX B: COMPONENT LIST AND LOCATIONS