

Technical Information Manual

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MOD. V1740

64 CHANNEL 12 BIT

65 MS/S DIGITIZER

MANUAL REV.11

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TABLE OF CONTENTS

1. GENERAL DESCRIPTION.....	8
1.1. OVERVIEW	8
1.2. BLOCK DIAGRAM.....	9
2. TECHNICAL SPECIFICATIONS.....	10
2.1. PACKAGING AND COMPLIANCY.....	10
2.2. POWER REQUIREMENTS	10
2.3. FRONT PANEL.....	11
2.4. EXTERNAL CONNECTORS.....	12
2.4.1. ANALOG INPUT connectors.....	12
2.4.2. CONTROL connectors.....	12
2.4.3. ADC REFERENCE CLOCK connectors	13
2.4.4. Digital I/O connectors.....	13
2.4.5. Optical LINK connector	14
2.5. OTHER FRONT PANEL COMPONENTS	14
2.5.1. Displays	14
2.6. INTERNAL COMPONENTS	14
2.7. TECHNICAL SPECIFICATIONS TABLE	16
2.8. ADAPTERS FOR ERNI SMC HEAD CONNECTORS	17
3. FUNCTIONAL DESCRIPTION.....	18
3.1. ANALOG INPUT.....	18
3.2. CLOCK DISTRIBUTION	19
3.2.1. Direct Drive Mode.....	20
3.2.2. PLL Mode	20
3.2.3. Trigger Clock.....	20
3.2.4. Output Clock.....	20
3.2.5. AD9510 programming	20
3.2.6. PLL programming	21
3.2.7. Direct Drive programming	21
3.2.8. Configuration file	22
3.2.9. Multi-board synchronization	22
3.3. ACQUISITION MODES	23
3.3.1. Acquisition run/stop.....	23
3.3.2. Data acquisition and storage.....	23
3.3.3. Acquisition Triggering: Samples and Events.....	24
3.3.3.1. Custom size events	25
3.3.4. Event structure.....	25
3.3.4.1. Header	25
3.3.4.2. Samples	26
3.3.4.3. Event format examples	26
3.3.5. Memory FULL management.....	27

3.4.	TRIGGER MANAGEMENT	28
3.4.1.	External trigger	28
3.4.2.	Software trigger.....	28
3.4.3.	Local channel auto-trigger.....	28
3.4.3.1.	Trigger coincidence level	29
3.4.4.	Trigger distribution	30
3.5.	FRONT PANEL I/OS.....	30
3.6.	TEST PATTERN GENERATOR	31
3.7.	ANALOG MONITOR.....	31
3.7.1.	Trigger Majority Mode (Monitor Mode = 0).....	31
3.7.2.	Test Mode (Monitor Mode = 1).....	32
3.7.3.	Buffer Occupancy Mode (Monitor Mode = 3).....	32
3.7.4.	Voltage Level Mode (Monitor Mode = 4).....	32
3.8.	RESET, CLEAR AND DEFAULT CONFIGURATION	32
3.8.1.	Global Reset	32
3.8.2.	Memory Reset	33
3.8.3.	Timer Reset.....	33
3.9.	VMEBUS INTERFACE	33
3.9.1.	Addressing capabilities.....	33
3.9.1.1.	Base address.....	33
3.9.1.2.	CR/CSR address.....	34
3.9.1.3.	Address relocation.....	34
3.10.	DATA TRANSFER CAPABILITIES	34
3.11.	EVENTS READOUT	34
3.11.1.	Sequential readout.....	34
3.11.1.1.	SINGLE D32	35
3.11.1.2.	BLOCK TRANSFER D32/D64, 2eVME	35
3.11.1.3.	CHAINED BLOCK TRANSFER D32/D64	36
3.11.2.	Event Polling	36
3.12.	OPTICAL LINK	36
3.13.	SOFTWARE TOOLS	36
4.	VME INTERFACE.....	38
4.1.	REGISTERS ADDRESS MAP	38
4.2.	CONFIGURATION ROM (0xF000-0xF084; R).....	39
4.3.	GROUP N THRESHOLD (0x1N80; R/W)	40
4.4.	GROUP N STATUS (0x1N88; R)	40
4.5.	GROUP N AMC FPGA FIRMWARE (0x1N8C; R).....	41
4.6.	GROUP N BUFFER OCCUPANCY (0x1N94; R)	41
4.7.	GROUP N DAC (0x1M98; R/W).....	41
4.8.	GROUP N ADC CONFIGURATION (0x1N9C; R/W)	41

4.9.	GROUP N CHANNEL TRIGGER MASK (0x1nA8; r/w)	41
4.10.	GROUP CONFIGURATION (0x8000; r/w)	42
4.11.	GROUP CONFIGURATION BIT SET (0x8004; w)	42
4.12.	GROUP CONFIGURATION BIT CLEAR (0x8008; w)	42
4.13.	BUFFER ORGANIZATION (0x800C; r/w)	42
4.14.	CUSTOM SIZE (0x8020; r/w)	43
4.15.	ACQUISITION CONTROL (0x8100; r/w).....	43
4.16.	ACQUISITION STATUS (0x8104; r).....	44
4.17.	SOFTWARE TRIGGER (0x8108; w).....	44
4.18.	TRIGGER SOURCE ENABLE MASK (0x810C; r/w).....	45
4.19.	FRONT PANEL TRIGGER OUT ENABLE MASK (0x8110; r/w)	45
4.20.	POST TRIGGER SETTING (0x8114; r/w)	46
4.21.	FRONT PANEL I/O DATA (0x8118; r/w).....	46
4.22.	FRONT PANEL I/O CONTROL (0x811C; r/w).....	46
4.23.	GROUP ENABLE MASK (0x8120; r/w)	47
4.24.	ROC FPGA FIRMWARE REVISION (0x8124; r).....	47
4.25.	EVENT STORED (0x812C; r)	48
4.26.	SET MONITOR DAC (0x8138; r/w).....	48
4.27.	BOARD INFO (0x8140; r)	48
4.28.	MONITOR MODE (0x8144; r/w).....	48
4.29.	EVENT SIZE (0x814C; r).....	48
4.30.	VME CONTROL (0xEF00; r/w)	48
4.31.	VME STATUS (0xEF04; r).....	49
4.32.	BOARD ID (0xEF08; r/w).....	49
4.33.	MCST BASE ADDRESS AND CONTROL (0xEF0C; r/w).....	49
4.34.	RELOCATION ADDRESS (0xEF10; r/w).....	50
4.35.	INTERRUPT STATUS ID (0xEF14; r/w).....	50
4.36.	INTERRUPT EVENT NUMBER (0xEF18; r/w)	50
4.37.	BLT EVENT NUMBER (0xEF1C; r/w).....	50
4.38.	SCRATCH (0xEF20; r/w)	50
4.39.	SOFTWARE RESET (0xEF24; w)	50
4.40.	SOFTWARE CLEAR (0xEF28; w)	50
4.41.	FLASH ENABLE (0xEF2C; r/w).....	51
4.42.	FLASH DATA (0xEF30; r/w).....	51
4.43.	CONFIGURATION RELOAD (0xEF34; w).....	51

5. INSTALLATION	52
5.1. POWER ON SEQUENCE	52
5.2. POWER ON STATUS	52
5.3. FIRMWARE UPGRADE.....	52
5.3.1. V1740 Upgrade files description.....	53

LIST OF FIGURES

FIG. 1.1: MOD. V1740 BLOCK DIAGRAM	9
FIG. 2.1: MOD. V1740 FRONT PANEL.....	11
FIG. 2.2: ERNI SMC CONNECTORS.....	12
FIG. 2.3: AMP CLK IN/OUT CONNECTOR	13
FIG. 2.4: PROGRAMMABLE IN/OUT CONNECTOR	13
FIG. 2.5: LC OPTICAL CONNECTOR	14
FIG. 2.6: ROTARY AND DIP SWITCHES LOCATION.....	15
FIG. 2.7: HEAD CONNECTORS ADAPTERS	17
FIG. 3.1: INPUT DIAGRAM	18
FIG. 3.2: CLOCK DISTRIBUTION DIAGRAM	19
FIG. 3.3: CAENPLLCONFIG MAIN MENU	21
FIG. 3.4: SAMPLING CLOCK PHASE SHIFT	22
FIG. 3.5: DATA STORAGE (UNDERScoreD = STORED)	24
FIG. 3.6: TRIGGER OVERLAP	25
FIG. 3.7: EVENT ORGANIZATION	27
FIG. 3.8: BLOCK DIAGRAM OF TRIGGER MANAGEMENT.....	28
FIG. 3.9: LOCAL TRIGGER GENERATION.....	29
FIG. 3.10: LOCAL TRIGGER RELATIONSHIP WITH COINCIDENCE LEVEL.....	29
FIG. 3.11: TRIGGER INTEGRATION	30
FIG. 3.12: MAJORITY LOGIC (2 TRIGGERING GROUPS; "POLARITY" BIT[6] OF GR. CONFIG. REG. =0)	32
FIG. 3.13: A24 ADDRESSING.....	33
FIG. 3.14: A32 ADDRESSING.....	33
FIG. 3.15: CR/CSR ADDRESSING.....	34
FIG. 3.16: SOFTWARE RELOCATION OF BASE ADDRESS	34
FIG. 3.17: EXAMPLE OF BLT READOUT	35
FIG. 3.18: BLOCK DIAGRAM OF THE SOFTWARE TOOLS.....	37

LIST OF TABLES

TABLE 1.1: MOD. V1740 VERSIONS	9
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TABLE 2.1: MODEL V1740 POWER REQUIREMENTS.....	10
TABLE 2.2 : FRONT PANEL LEDS	14
TABLE 2.3 : MOD. V1740 TECHNICAL SPECIFICATIONS	16
TABLE 3.1 : FRONT PANEL I/Os DEFAULT SETTING	31
TABLE 4.1: ADDRESS MAP FOR THE MODEL V1740.....	38
TABLE 4.2: ROM ADDRESS MAP FOR THE MODEL V1740.....	40
TABLE 4.3: OUTPUT BUFFER MEMORY BLOCK DIVISION.....	43

1. General description

1.1. Overview

The Mod. V1740 is a 1-unit wide VME 6U module housing a 64 Channel 12 bit 65 MS/s Flash ADC Waveform Digitizer with threshold Auto-Trigger capabilities.

Maximum sampling frequency is 65 MS/s using an external clock and 62.5 MS/s using the internal source.

The high channel density is allowed by the AD9222 Octal 12-bit 65 MSPS Analog-to-Digital Converter; therefore most channel settings are performed over "groups" of 8 channels (one group per ADC chip). The single ended analog input signal has a dynamic range of 2 V_{pp} (10 V_{pp} available on request).

The DC offset of the input signal can be adjusted (for group of 8 channels) by a programmable 16bit DAC.

The modules feature a front panel clock/reference In/Out and a PLL for clock synthesis from internal/external references. This allows multi board phase synchronizations to an external clock reference or to a clock Digitizer master board.

The data stream is continuously written in a circular memory buffer. When the trigger occurs, the FPGA writes further N samples for the post trigger and freezes the buffer that can be read either via VME or via Optical Link. The acquisition can continue without dead time in a new buffer.

VME and Optical Link accesses take place on independent paths and are handled by the on-board controller, therefore when accessed through Optical Link the board can be operated outside the VME Crate (see § 2.1).

Each Group has a SRAM memory (see Table below) with independent read-write access divided in buffers (1 ÷ 1024) of programmable size.

The trigger signal can be provided via the front panel input as well as via the VMEbus, but it can also be generated internally. The trigger from one board can be propagated to the other boards through the front panel Trigger Output.

An Analog Output allows to reproduce the sum of the input signals as well as the majority of the buffer occupancy.

The Modules VME interface is VME64X compliant and the data readout can be performed in Single Data Transfer (D32), 32/64 bit Block Transfer (BLT, MBLT, 2eVME, 2eSST) and 32/64 bit Chained Block Transfer (CBLT).

The built-in daisy chainable Optical Link is able to transfer data at 80 MB/s, thus it is possible to connect up to eight ADC boards (512 ADC channels) to a single Optical Link Controller (Mod. A2818). Optical Link and VME access are internally arbitrated..

The board is available with different input range, memory and connector configuration, as summarized by the following table:

Table 1.1: Mod. V1740 versions

Model	Input type	SRAM Memory	Optical link	AMC FPGA	Form factor
V1740	Single ended	192Ksamples / ch	Yes	EP3C16	6U-VME64
V1740B	Single ended	1.5Msamples / ch	Yes	EP3C16	6U-VME64
VX1740	Single ended	192 Ksamples / ch	Yes	EP3C16	6U-VME64X
VX1740B	Single ended	1.5Msamples / ch	Yes	EP3C16	6U-VME64X

1.2. Block Diagram

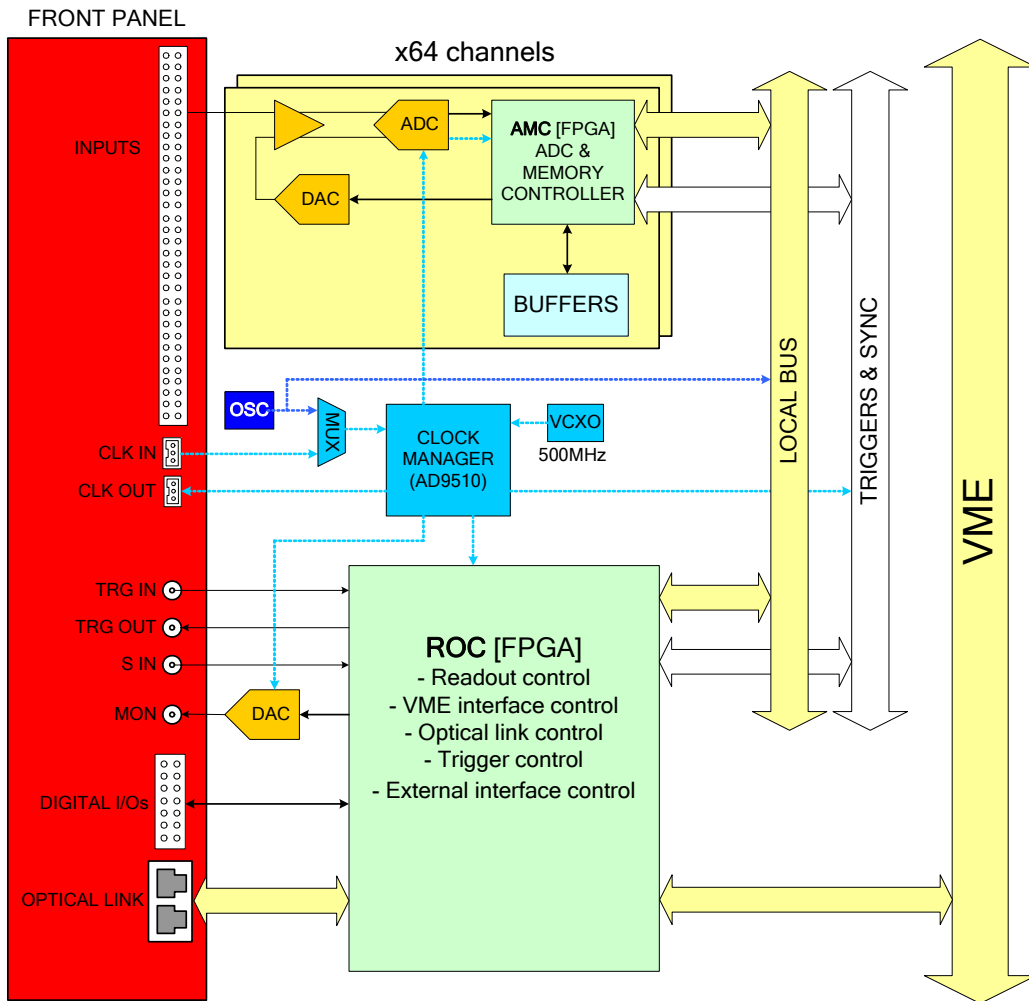


Fig. 1.1: Mod. V1740 Block Diagram

The function of each block will be explained in detail in the subsequent sections.

2. Technical specifications

2.1. Packaging and Compliancy

The module is housed in a 6U-high, 1U-wide VME unit. The board hosts the VME P1, and P2 connectors and fits into both VME/VME64 standard and V430 backplanes. VX1740 versions fit VME64X compliant crates. In all cases only well ventilated crates must be used.

The V1740 cannot be operated with CAEN crates VME8001/8002/8004/8004A

2.2. Power requirements

The power requirements of the module are as follows:

Table 2.1: Model V1740 power requirements

+5 V	5.5 A
+12 V	0.8 A
-12 V	0.9 A

2.3. Front Panel

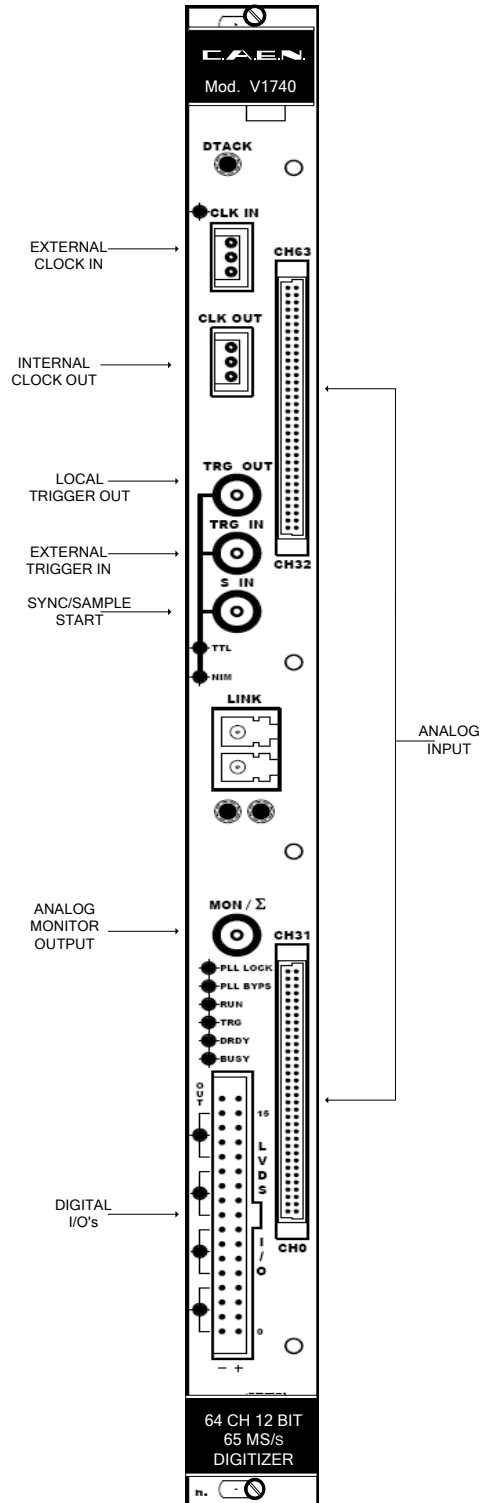


Fig. 2.1: Mod. V1740 front panel

2.4. External connectors

2.4.1. ANALOG INPUT connectors

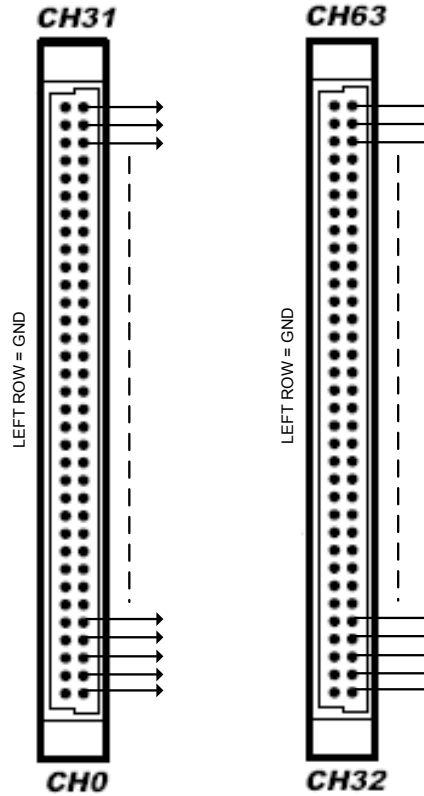


Fig. 2.2: ERNI SMC Connectors

Function: Analog input, single ended, input dynamics: 2Vpp $Z_{in}=50\Omega$ (on request: 10Vpp $Z_{in}=1K\Omega$)

Mechanical specifications: Two ERNI SMC-114805 Dual Row 68pin connectors

N.B.: absolute max analog input voltage = 6Vpp (with V_{rail} max to +6V or -6V) for any DAC offset value. Ensure that alignment is correct during insertion/extraction operations; incorrect alignment may lead to connector damage.

2.4.2. CONTROL connectors

Function:

- TRG OUT: Local trigger output (NIM/TTL, on $R_t = 50\Omega$)
- TRG IN: External trigger input (NIM/TTL, $Z_{in} = 50\Omega$)
- SYNC/SAMPLE/START (S_IN): Sample front panel input (NIM/TTL, $Z_{in}=50\Omega$)
- MON/ Σ : DAC output 1Vpp on $R_t=50\Omega$

Mechanical specifications: 00-type LEMO connectors

2.4.3. ADC REFERENCE CLOCK connectors

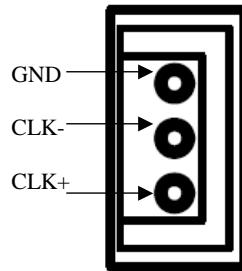


Fig. 2.3: AMP CLK IN/OUT Connector

CLK_IN

Function: CLK IN: External clock/Reference input, AC coupled (diff. LVDS, ECL, PECL, LVPECL, CML), Zdiff= 110Ω.

Mechanical specifications: AMP 3-102203-4 connector

CLK_OUT

Function: CLOCK OUT: Clock output, DC coupled (diff. LVDS), Zdiff= 110Ω.

Mechanical specifications: AMP 3-102203-4 connector

2.4.4. Digital I/O connectors

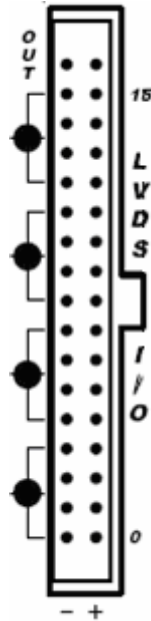


Fig. 2.4: Programmable IN/OUT Connector

Function: N.16 programmable differential LVDS I/O signals, Zdiff_in= 110 Ohm. Four Independent signal group 0÷3, 4÷7, 8÷11, 12÷15, In / Out direction control; Lowest couple: 0; highest couple: not connected. See also § 3.5.

Mechanical specifications: 3M-7634-5002- 34 pin Header Connector

2.4.5. Optical LINK connector

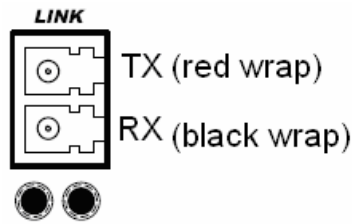


Fig. 2.5: LC Optical Connector

Mechanical specifications: LC type connector; to be used with Multimode 62.5/125µm cable with LC connectors on both sides (see also § 3.12); CAEN provides optical fiber cables with a duplex connector on the A2818 side and two simplex connectors on the board side; the simplex connector with the black wrap is for the RX line (lower) and the one with the red wrap is for the TX (higher).

Electrical specifications: Optical link for data readout and slow control with transfer rate up to 80MB/s; TX/RX, daisy chainable.

2.5. Other front panel components

2.5.1. Displays

The front panel hosts the following LEDs:

Table 2.2 : Front panel LEDs

Name:	Colour:	Function:
DTACK	green	VME read/write access to the board
CLK_IN	green	External clock enabled.
NIM	green	Standard selection for CLK I/O, TRG OUT, TRG IN, S IN.
TTL	green	Standard selection for CLK I/O, TRG OUT, TRG IN, S IN.
LINK	green/yellow	Network present; Data transfer activity
PLL_LOCK	green	The PLL is locked to the reference clock
PLL_BYPS	green	The reference clock drives directly ADC clocks; the PLL circuit is switched off and the PLL_LOCK LED is turned off.
RUN	green	RUN bit set (see § 4.16)
TRG	green	Trigger accepted
DRDY	green	Event/data (depending on acquisition mode) are present in the Output Buffer
BUSY	red	All the buffers are full
OUT_LVDS	green	Signal group OUT direction enabled.

2.6. Internal components

SW2,4,5,6 “Base Addr. [31:16]”: Type: 4 rotary switches
Function: Set the VME base address of the module.

SW3 “CLOCK SOURCE”: Type Dip Switch
Function: Select clock source (External or Internal)

2.7. Technical specifications table

Table 2.3 : Mod. V1740 technical specifications

Package	1-unit wide VME 6U module
Analog Input	64 channels, single-ended; 2 Vpp (10Vpp on request) input range, positive or negative; 30MHz Bandwidth, 2nd order linear phase anti-aliasing low-pass filter ADC sampling clock generator: PLL MODE - internal reference (50MHz local oscillator) PLL MODE - external reference on CLK_IN (100ppm tolerance) Connector: ERNI SMC, (for high density flat cable: conductor spacing: 0.635 mm / 0.025") Programmable DAC for Offset Adjust (one for 8 channels).
Digital Conversion	Resolution: 12 bit Sampling rate: up to 65 MS/s simultaneously on each channel Multi board synchronization (one board can act as clock master). External Gate Clock capability (NIM / TTL) by S_IN input connector, for burst or single sampling mode.
ADC Sampling Clock generation	sampling clock generation supports three operating modes: - PLL mode - internal reference (62.5 MHz local oscillator) - PLL mode - external reference on CLK_IN (Jitter<100ppm). - PLL Bypass mode: External clock on CLK_IN drives directly ADC clocks. External clock Frequency from 10 to 65 MHz.
CLK_IN	AC coupled differential input clock LVDS, ECL, PECL, LVPECL, CML (single ended NIM/TTL available using CAEN A654 cable).
CLK_OUT	DC coupled differential LVDS output clock, locked to ADC sampling clock. Freq.: 10 ÷ 50MHz.
Memory Buffer	192K sample/ch or 1.5M sample/ch; Multi Event Buffer with independent read and write access. Programmable event size and pre-post trigger. Divisible into 1 + 1024 buffers.
Trigger	Common External TRGIN (NIM or TTL) and VME Command. Individual channel auto trigger (time over/under threshold) TRGOUT (NIM or TTL) for the trigger propagation to other V1740 boards.
Trigger Time Stamp	32bit (LSB: 8ns; FSR: 17s). Sync input for Time Stamp alignment.
ADC and Memory controller FPGA	Altera Cyclone EP3C16 for 16 channels
Optical Link	Data readout and slow control with transfer rate up to 80 MB/s, to be used instead of VME bus. Daisy chainable: one A2818 PCI card can control and read eight V1740 boards in a chain.
VME interface	VME64X compliant D32, BLT32, MBLT64, CBLT32/64, 2eVME, 2eSST, Multi Cast Cycles Transfer rate: 60MB/s (MBLT64), 100MB/s (2eVME), 160MB/s (2eSST) Sequential access to the data of the Multi Event Buffer The Chained readout allows to read one event from all the boards in a VME crate with a BLT access
Upgrade	V1740 firmware can be upgraded via VME
Software	General purpose C Libraries and Demo Programs (CAENScope).
LVDS I/O	16 general purpose LVDS I/O controlled by the FPGA Busy, Data Ready, Memory full, Trig-Out flag and other function can be programmed An Input Pattern from the LVDS I/O can be associated to each trigger as an event marker

2.8. Adapters for ERNI SMC head connectors

The Mod. V1740 has ERNI SMC-114805 Dual Row 68pin input connectors, to be mated to ERNI SMC-154743. CAEN provides various solutions to adapt those connectors into the most common formats; such devices are:

Mod.	Function	From/To	To/From
A746A	32ch Adapter for 100x100mils head connector	ERNI SMC-114805	3M – P50E – 068S
A746B	64ch Adapter for Lemo connector	ERNI SMC-114805	00-type LEMO
A967	32 Channel Cable Adapter	3M – P50E – 068S	3M 3431-5202 Header-type

The following figure shows how to use the adapters:

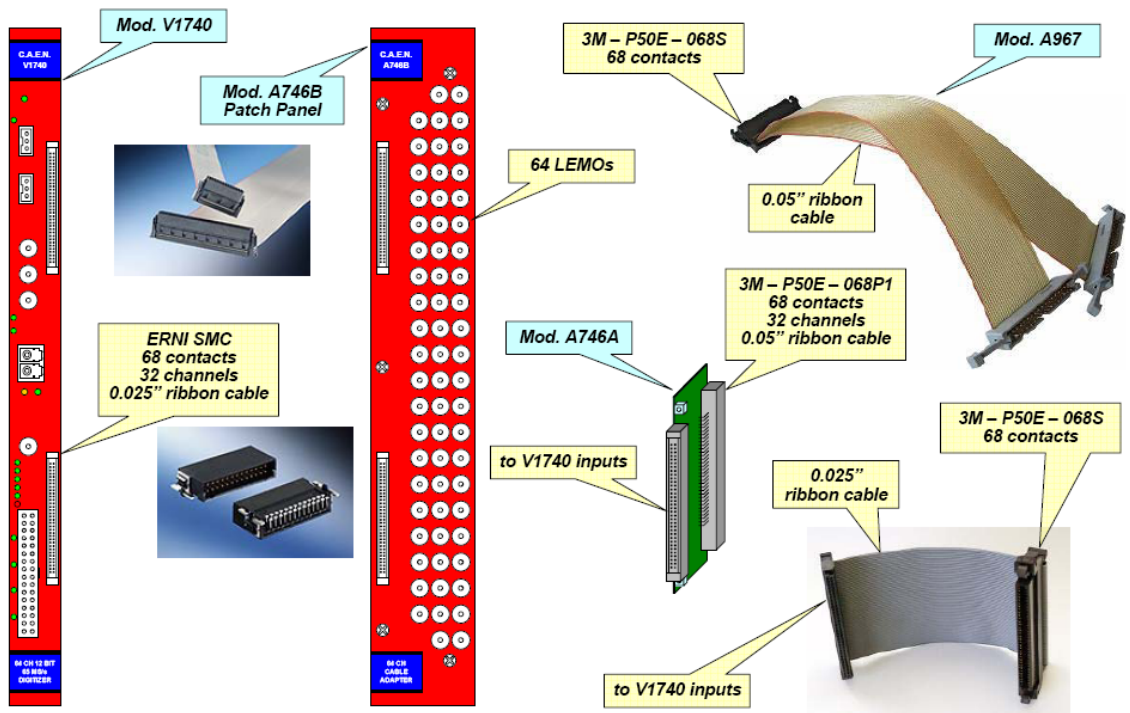


Fig. 2.7: Head connectors adapters

3. Functional description

3.1. Analog Input

Input dynamic is 2Vpp ($Z_{in} = 50 \Omega$). 10Vpp ($Z_{in} = 1K\Omega$) dynamic is available on request. A 16bit DAC allow to add up to $\pm 1V$ ($\pm 5V$ with high-range input) DC offset in order to preserve the full dynamic range also with uni-polar positive or negative input signals. The input bandwidth ranges from DC to 30 MHz (with 2nd order linear phase anti-aliasing low pass filter).

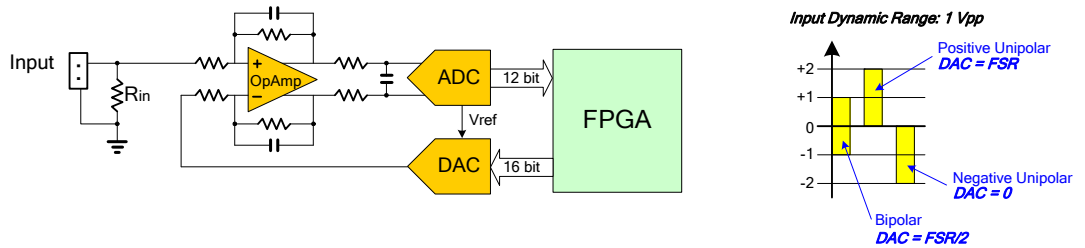


Fig. 3.1: Input diagram

3.2. Clock Distribution

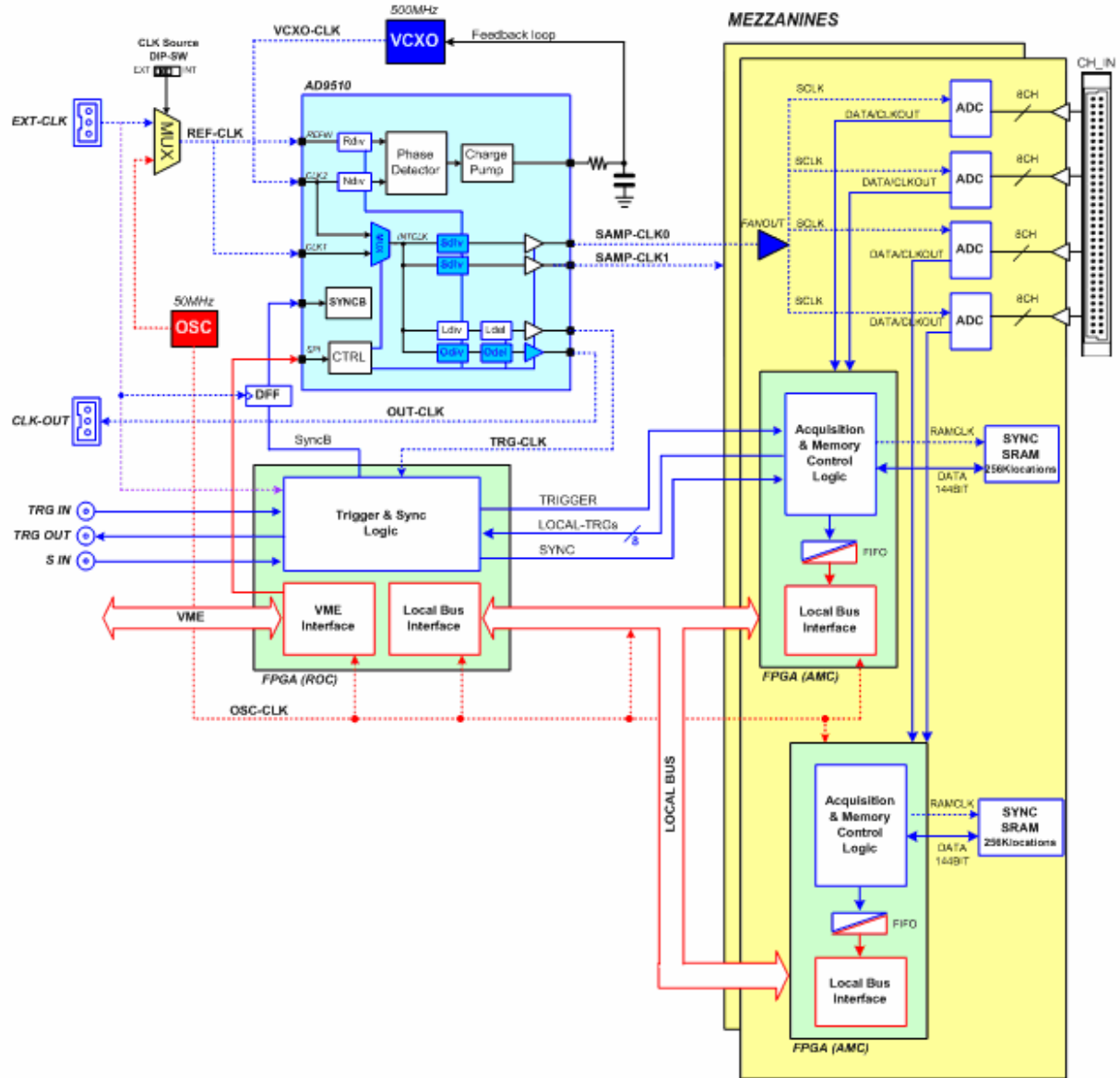


Fig. 3.2: Clock distribution diagram

The module clock distribution takes place on two domains: OSC-CLK and REF-CLK; the former is a fixed 50MHz clock provided by an on board oscillator, the latter provides the ADC sampling clock.

OSC-CLK handles both VME and Local Bus (communication between motherboard and mezzanine boards; see red traces in the figure above).

REF-CLK handles ADC sampling, trigger logic, acquisition logic (samples storage into RAM, buffer freezing on trigger) through a clock chain. Such domain can use either an external (via front panel signal) or an internal (via local oscillator) source (selection is performed via dip switch SW1, see § 2.6); in the latter case OSC-CLK and REF-CLK will be synchronous (the operation mode remains the same anyway).

REF-CLK is processed by AD9510 device, which delivers 6 clock out signals; 4 signals are sent to ADCs, one to the trigger logic and one to drive CLK-OUT output (refer to AD9510 data sheet for more details:

http://www.analog.com/UploadedFiles/Data_Sheets/AD9510.pdf); two operating modes are foreseen: **Direct Drive Mode** and **PLL Mode**

3.2.1. **Direct Drive Mode**

The aim of this mode is to drive externally the ADCs' Sampling Clock; generally this is necessary when the required sampling frequency is not a VCXO frequency submultiple. The only requirement over the SAMP-CLK is to remain within the ADCs' range.

It is important to say that Direct Drive is the only way to achieve the full ADC 65 MS/s sampling frequency, since PLL dividers allow a maximum 62.5 MS/s one.

3.2.2. **PLL Mode**

The AD9510 features an internal Phase Detector which allows to couple REF-CLK with VCXO (500 MHz frequency); for this purpose it is necessary that REF-CLK is a submultiple of 500 MHz.

AD9510 default setting foresees the board internal clock (50MHz) as clock source of REF-CLK.

This configuration leads to $N_{div} = 100$, $R_{div} = 5$, thus obtaining 10MHz at the Phase Detector input and CLK-INT = 500 MHz.

The required Sampling Clock (62.5MHz max) is obtained by processing CLK-INT through Sdiv dividers.

When an external clock source is used, if it has 62.5MHz frequency, then AD9510 programming is not necessary, otherwise Ndiv and Rdiv have to be modified in order to achieve PLL lock.

A REF-CLK frequency stability better than 100ppm is mandatory.

3.2.3. **Trigger Clock**

TRG-CLK signal has a frequency equal to $\frac{1}{2}$ of SAMP-CLK; therefore a 2 samples "uncertainty" occurs over the acquisition window.

3.2.4. **Output Clock**

Front panel Clock Output is User programmable. Odiv and Odel parameters allows to obtain a signal with the desired frequency and phase shift (in order to recover cable line delay) and therefore to synchronize daisy chained boards. CLK-OUT default setting is OFF, it is necessary to enable the AD9510 output buffer to enable it.

3.2.5. **AD9510 programming**

CAEN has developed a software tool which allows to handle easily the clock parameters: CAENPLLConfig is a software tool which allows the PLL management, whenever the module is controlled through a CAEN VME Controller; see www.caen.it path:

Products / Front End / VME / Controller (VME)

The tool is developed through open source classes wxWidgets v.2.6.3

(see <http://www.wxwidgets.org/>)

and requires the CAENVMETool API's to be installed (they can be downloaded at www.caen.it/ with the *SW package for CAEN VME Bridges & Slave Boards*).

CAENPLLConfig is available at: www.caen.it/

And must be simply run on the PC connected to the used CAEN VME Controller. The User has to select the **board type** and **base address** (in the ADC BOARD field), then the used mode (**PLL** or **Direct Feed/BYPASS** in the INPUT field); see figure below:



Fig. 3.3: CAENPLLConfig Main menu

3.2.6. PLL programming

In PLL mode the User has to enter the divider for input clock frequency (**input clock divider** field in CAENPLLConfig Main menu); since the VCXO frequency is 500 MHz, in order to use, for example, a 50MHz ExtClk, the divider to be entered is 20.

Then it is necessary to set the parameters for sampling clock and CLK_OUT (**enable**, **divide ratio** and **phase shift/delay** in **Output Clock** field of CAENPLLConfig Main menu); the tool refuses wrong settings for such parameters.

3.2.7. Direct Drive programming

In Direct Drive/BYPASS mode, the User can directly set the input frequency (**Input Clock** field, real values are allowed). Given an input frequency, it is possible to set the parameters in order to provide the required signals.

3.2.8. Configuration file

Once all parameters are set, the tool allows to save the configuration file which includes all the AD9510 device settings (**SAVE** button in the upper toolbar of CAENPLLConfig Main menu). It is also possible to browse and load into the AD9510 device a pre existing configuration file (**OPEN** button in the upper toolbar of CAENPLLConfig Main menu). For this purpose it is not necessary the board power cycle.

3.2.9. Multi-board synchronization

In order to allow several V1740s to work synchronously (same sampling clock for all channels) it is necessary to use the external clock. For such purpose, two solutions are possible

- a daisy chain where the clock is propagated from one board to another, with the first board used as a “clock master” (whose source could be either the internal clock or an external reference managed by the User),
- a tree structure, with an equalized clock distributor (fan-out unit with “low skew” outputs and constant cables length).

In both cases, the goal is to have all REF-CLK signals with the same phase. Since the PLL aligns the phase of VCXO output signal to REF-CLK, the result of synchronization is that all V1740s have the 500MHz VCXO output signals perfectly aligned in phase.

However, despite the V1740s having all the same 500MHz reference, it is not guaranteed that the sampling clock is in its turn aligned. In fact the use of clock dividers to produce the sampling clock, may lead such signals to have different phases, as shown in the following picture, where two 250MHz (divider = 2, see § 3.2.2) are obtained from a 500MHz VCXO output.

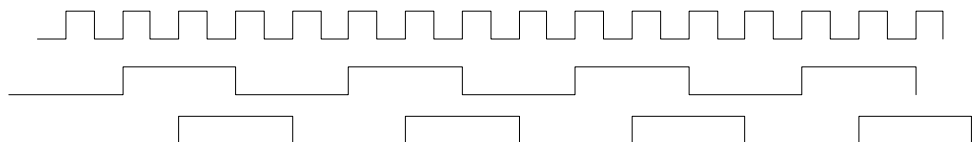


Fig. 3.4: Sampling clock phase shift

In order to keep all dividers outputs aligned, the AD9510 is provided with a SYNCB input (see § 3.2); all dividers are put in phase on a SYNCB edge. This is done automatically within a board at any board reset, therefore it is guaranteed that one board has the same sampling clock for all channels. However if it is necessary to synchronize sampling clock on more V1740s, then SYNCB signals have to be synchronized in their turn as well.

On modules with printed board Rev.2 (or greater), synchronization is achieved by piloting SYNCB through a D-Edge Triggered Flip Flop receiving EXT_CLK as clock input.

In this way it is ensured that the SYNCBs of all modules have the same phase. On modules with printed board Rev.1, however, the synchronization SYNCB can be obtained through the S-IN signal. In fact on S-IN leading edge, when the board is properly programmed (see § 3.3.1), the ROC FPGA sends a pulse on SYNCB. In order to avoid “uncertainty”, it is necessary that S-IN is sent to all the modules in phase with EXT-CLK: this will allow all V1740s to receive it with the same clock period.

After the synchronization of sampling clock signals, the modules will be also in phase with each other and all samples will be written into memory all at the same time.

However, in order to ensure that the windows of acquisition related to the external trigger signal are also perfectly aligned, it is also necessary that the TRG-IN signal is sent to all

modules synchronously with EXT-CLK and in accordance with the setup time related to its leading edge.

In fact, if EXT-TRG is not correlated with EXT-CLK, a board might sense the trigger in a certain period of the clock while another might sense it in the subsequent. Therefore an uncertainty of 1 EXT-CLK period would occur (and then 1 SAMP-CLK hit) on the position of the acquired stored buffer with respect to the trigger arrival time.

The distribution of trigger can be simplified through the use of a daisy-chain: the external trigger signal is sent to the first board in the chain, and this, in coincidence with the TRG-IN received, gets triggered and generates a TRG-OUT which is in turn fed to the adjacent board TRG-IN and so on. There is a fixed latency of few clock hits between TRG-IN and TRG-OUT, the value of this latency depends on the loaded firmware version; this latency, which spreads from board to board, can be easily rejected by acting on the value of the Post Trigger (see § 3.3.3) in order to have acquisition windows of all modules perfectly aligned.

If the external trigger entering the first board is asynchronous, then a one sample uncertainty occurs, as described above; when this uncertainty is resolved on the first board, all the other ones will be aligned to it. If a precise temporal relationship between trigger and samples is required (such as repeated acquisitions where a jitter on the position of the signal in the acquisition window is a major issue), it is suggested to use one input channel (among all the V1740s in the chain) to sample the trigger signal itself: this will allow to reconstruct off-line the trigger edge position in the acquisition window, with a resolution smaller than the sampling period (through interpolation).

3.3. Acquisition Modes

3.3.1. Acquisition run/stop

The acquisition can be started in two ways, according to Acquisition Control register Bits [1:0] setting (see § 4.14):

- setting the RUN/STOP bit (bit[2]) in the Acquisition Control register (bits [1:0] of Acquisition Control must be set to REGISTER-CONTROLLED RUN MODE or S-IN CONTROLLED RUN MODE)
- driving S_IN signal high (bits [1:0] of Acquisition Control must be set to 01)

Therefore acquisition is stopped either:

- resetting the RUN/STOP bit (bit[2]) in the Acquisition Control register (bits [1:0] of Acquisition Control must be set to REGISTER-CONTROLLED RUN MODE or S-IN CONTROLLED RUN MODE)
- driving S_IN signal low (bits [1:0] of Acquisition Control set to 01)

3.3.2. Data acquisition and storage

The S_IN signal (see § 2.4.2) can be used as “gate” to enable samples storage. The samples produced by the 65MHz ADC are stored in memory only if they are validated by the S_IN signal, otherwise they are rejected; one sample per channel is stored at each clock hit in coincidence with S_IN (see data format at § 3.3.4). The values sampled as the S-IN signal is active (high) are stored; SxCy means “Sample x of Channel y” etc.

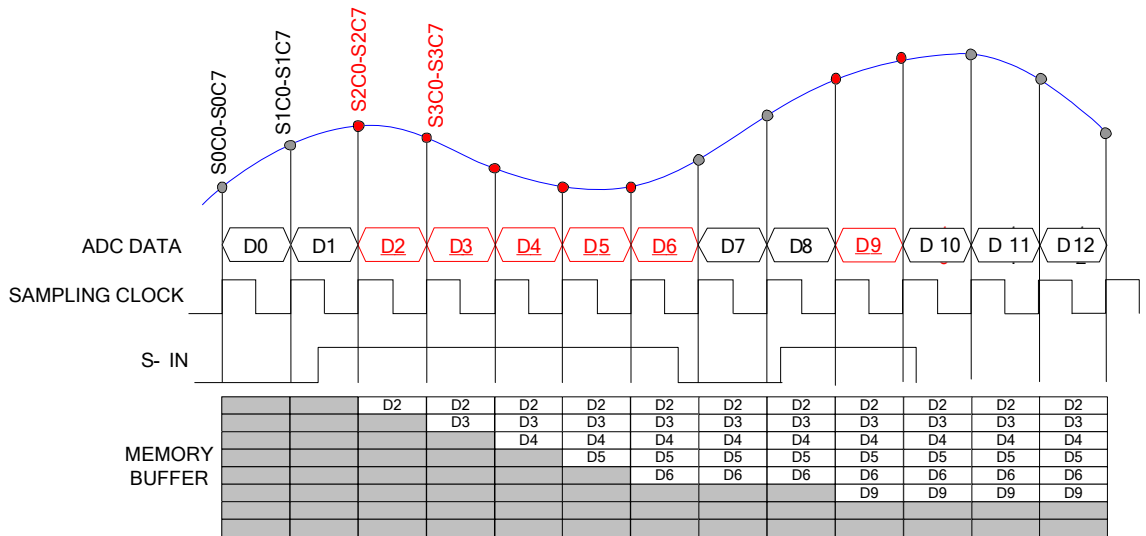


Fig. 3.5: Data Storage (underscored = stored)

3.3.3. Acquisition Triggering: Samples and Events

When the acquisition is running, a trigger signal allows to:

- store a Trigger Time Tag (TTT): the value of a 32 bit counter which steps on with 125 MHz frequency and represents a time reference
- increment the EVENT COUNTER (see § 4.25)
- fill the active buffer with the pre/post-trigger samples, whose number is programmable (Acquisition window width, § 4.20), freezing then the buffer for readout purposes, while acquisition continues on another buffer; buffer size is programmable, see Buffer Organization (0x800C) register, § 4.13.

An event is therefore composed by the trigger time tag, pre- and post-trigger samples and the event counter.

Overlap between "acquisition windows" may occur (a new trigger occurs while the board is still storing the samples related to the previous trigger); this overlap can be either rejected or accepted (programmable via VME).

If the board is programmed to accept the overlapped triggers, as the "overlapping" trigger arrives, the current active buffer is filled up, then the samples storage continues on the subsequent one.

In this case events will not have all the same size (see figure below).

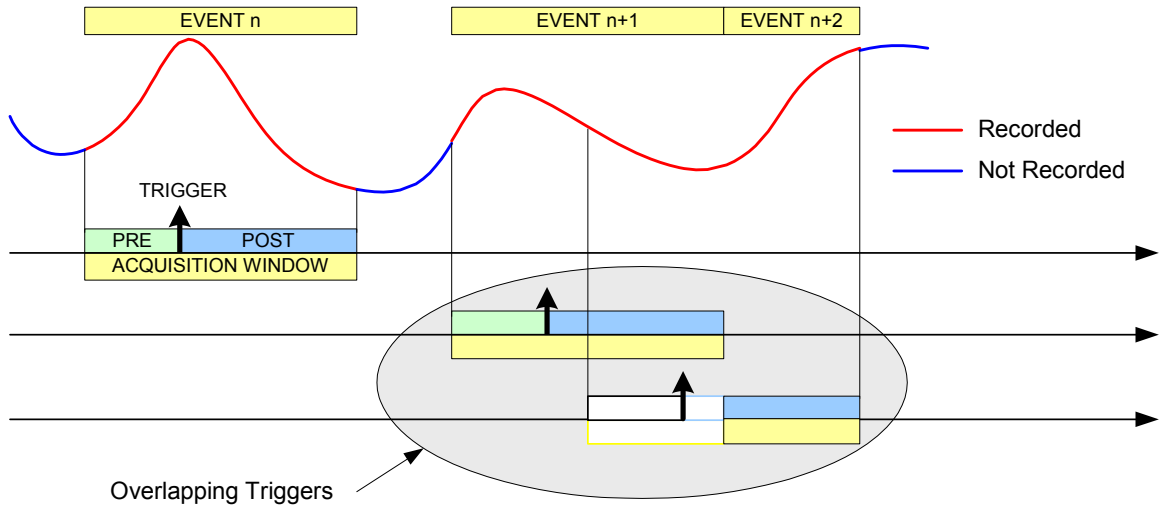


Fig. 3.6: Trigger Overlap

A trigger can be refused for the following causes:

- acquisition is not active
- memory is FULL and therefore there are no available buffers
- the required number of samples for building the pre-trigger of the event is not reached yet; this happens typically as the trigger occurs too early either with respect to the RUN_ACQUISITION command (see § 3.3.1) or with respect to a buffer emptying after a MEMORY_FULL status
- the trigger overlaps the previous one and the board is not enabled for accepting overlapped triggers

As a trigger is refused, the current buffer is not frozen and the acquisition continues writing on it. The Event Counter can be programmed in order to be either incremented or not. If this function is enabled, the Event Counter value identifies the number of the triggers sent (but the event number sequence is lost); if the function is not enabled, the Event Counter value coincides with the sequence of buffers saved and readout.

3.3.3.1. Custom size events

It is possible to make events with a number of Samples per block, which depends on Buffer Organization register setting (see § 4.13), smaller than the default value. Such "Custom Size" events can be programmed through Custom Size (0x8020) register, § 4.14.

3.3.4. Event structure

An event is structured as follows:

- Header (four 32-bit words)
- Data (variable size and format)

The event can be readout either via VME or Optical Link; data format is 32 bit word.

3.3.4.1. Header

It is composed by four words, namely:

- Size of the event (number of 32 bit words)

- Board ID (GEO); 16 bit pattern, latched on the LVDS I/O as one trigger arrives; Group Mask (=1: Groups participating to event; ex GR5 and GR7 participating → Gr_Mask: 0xA0, this information must be used by the software to acknowledge what Group the samples are coming from; the first event contains the samples from the Group with the lowest number)
- Event Counter: It is the trigger counter; it can count either accepted triggers only, or all triggers (see § 4.14).
- Trigger Time Tag: It is a 32 bit counter (31 bit count + 1 overflow bit), which is reset either as acquisition starts or via front panel Reset signal (see § 3.6), and is incremented at each sampling clock hit. It is the trigger time reference.

3.3.4.2. Samples

Stored samples; data from masked channels are not read.

3.3.4.3. Event format examples

An event is structured as follows:

- identifier (Trigger Time Tag, Event Counter)
- samples caught in the acquisition windows

The event can be stored in the board memories (and can be readout via VME/Optical Link), data format is 32 bit word (SxCy means "Sample x of Channel y" etc.).

The event format is therefore the following:

N.B.: data transfer starts from Channel 0 of Group 0; once all the data from one Group are transferred, data transfer from the subsequent Group (from 0 to 7) begins.

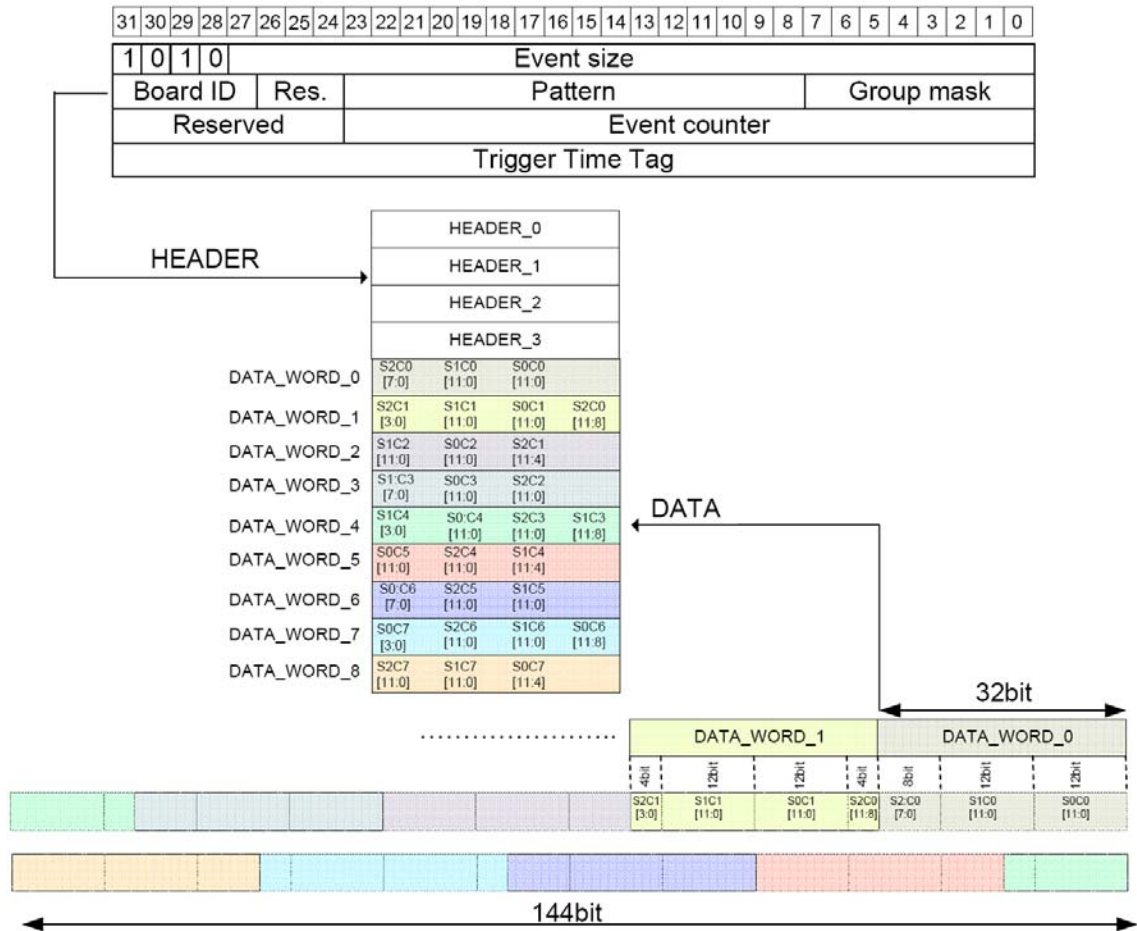


Fig. 3.7: Event Organization

3.3.5. Memory FULL management

Bit5 of Acquisition Control register (see § 4.14), allows to select Memory FULL management mode:

In Normal Mode the board becomes full, whenever all buffers are full (see § 4.13); otherwise (“Always one buffer free” mode) it is possible to always keep one buffer free: board becomes full, whenever N-1 buffers are full; with N = nr. of blocks (see § 4.13).

In Normal Mode, the board waits until one buffer is filled since FULL status is exited (whether the trigger is overlapped or not). The board exits FULL status at the moment which the last datum from the last channel participating to the event is read.

In “Always one buffer free” mode, one buffer cannot be used (therefore it is NOT POSSIBLE, with this mode, to set Buffer Code to 0000; see § 4.13), but this allows to eliminate dead time when FULL status is exited.

3.4. Trigger management

All the channels in a board share the same trigger: this means that all the channels store an event at the same time and in the same way (same number of samples and same position with respect to the trigger); several trigger sources are available.

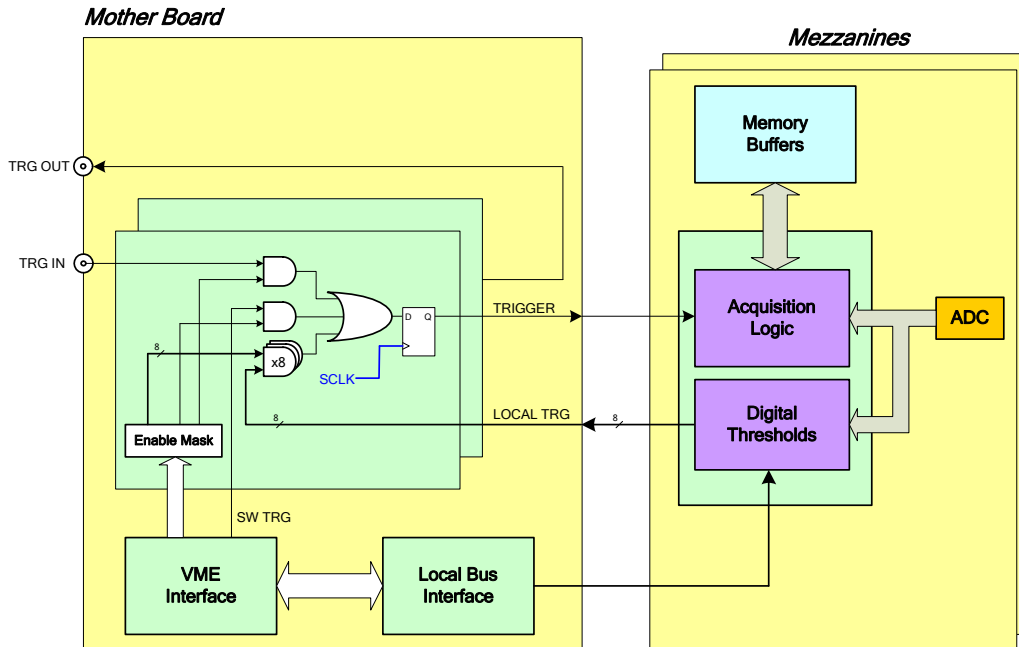


Fig. 3.8: Block diagram of Trigger management

3.4.1. External trigger

External trigger can be NIM/TTL signal on LEMO front panel connector, 50 Ohm impedance. The external trigger is synchronized with the internal clock (see § 3.2.3); if External trigger is not synchronized with the internal clock, a one clock period jitter occurs.

3.4.2. Software trigger

Software trigger are generated via VME bus (write access in the relevant register, see § 4.17).

3.4.3. Local channel auto-trigger

Each "channel group" (0÷7, 8÷15,...56÷63) can generate a local trigger as the digitized signal on one of the enabled channels (see § 4.9), exceeds the V_{th} threshold (ramping up or down, depending on VME settings). The V_{th} digital threshold and the edge type are programmable via VME register accesses, see § 4.3.

N.B.: the local trigger signal does not start directly the event acquisition on the "group" that generated it; such signal is propagated to the central logic which produces the global trigger, which is distributed to all groups (see § 3.4.4).

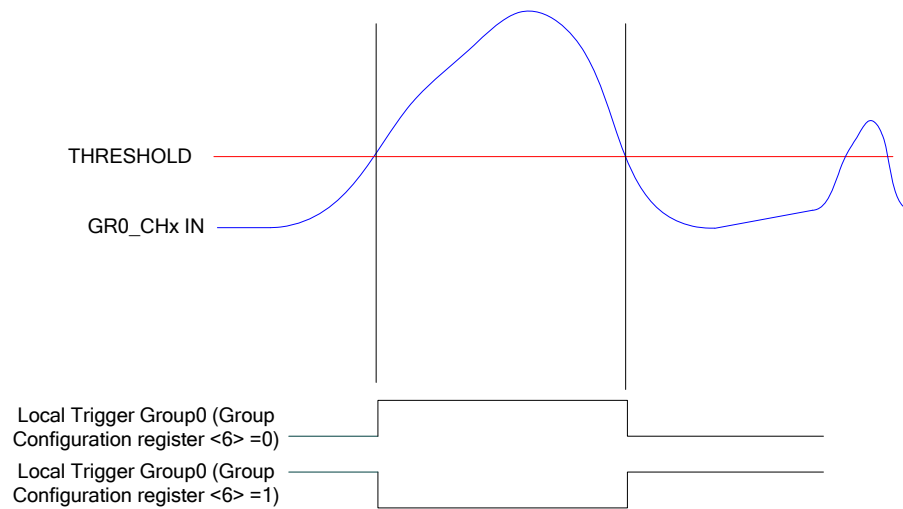


Fig. 3.9: Local trigger generation

3.4.3.1. Trigger coincidence level

It is possible to set the minimum number of groups with at least one channel that must be over threshold (beyond the triggering group), in order to actually generate the local trigger signal. If, for example, Trigger Source Enable Mask (see § 4.18) bits[7:0]=FF (all groups enabled) and Local trigger coincidence level = 1 (bits [26:24]), whenever an enabled channel exceeds the threshold, the trigger will be generated only if at least another channel is over threshold at that moment. Local trigger coincidence level must be smaller than the number of channels enabled via bit[7:0] mask. The following figure shows examples with Local trigger coincidence level = 1 and = 0.

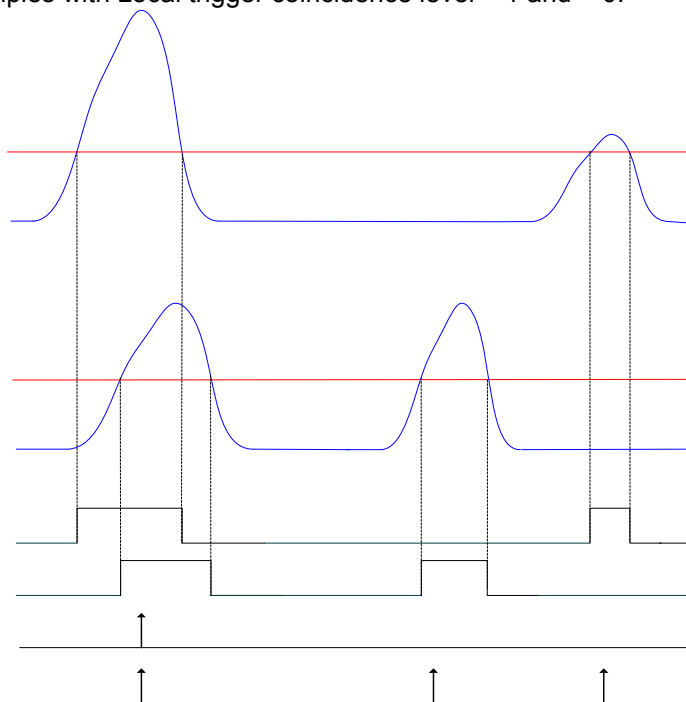


Fig. 3.10: Local trigger relationship with Coincidence level

3.4.4. Trigger distribution

The OR of all the enabled trigger sources, after being synchronized with the internal clock, becomes the global trigger of the board and is fed in parallel to all the channels, which store an event.

A Trigger Out is also generated on the relevant front panel TRG_OUT connector (NIM or TTL), and allows to extend the trigger signal to other boards.

For example, in order to start the acquisition on all the channels in the crate, as one of the channels ramps over threshold, the Local Trigger must be enabled as Trigger Out, the Trigger Out must then be fed to a Fan Out unit; the obtained signal has to be fed to the External Trigger Input of all the boards in the crate (including the board which generated the Trigger Out signal); see also the following figure.

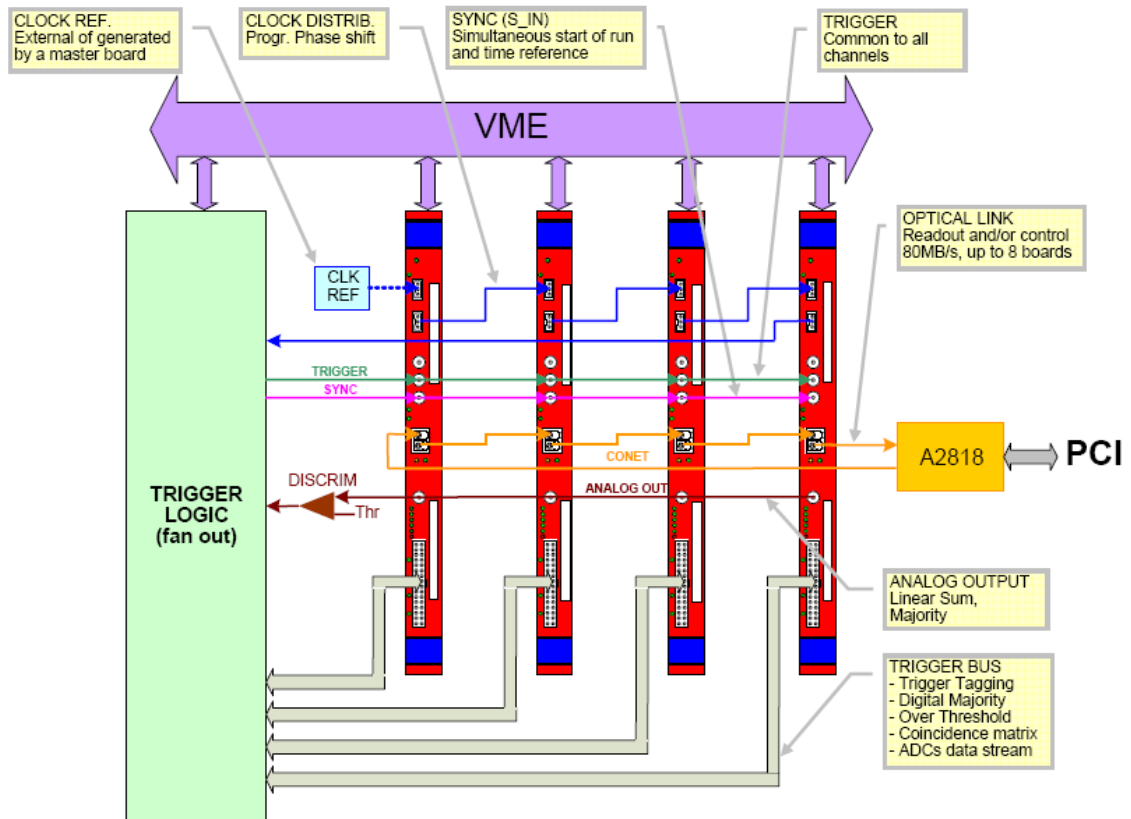


Fig. 3.11: Trigger integration

3.5. Front Panel I/Os

The V1740 is provided with 16 programmable general purpose LVDS I/O signals. Signals can be programmed via VME (see § 4.21 and § 4.22).

Default configuration is:

Table 3.1 : Front Panel I/Os default setting

Nr.	Direction	Description
0	out	Group 0 Trigger Request
1	out	Group 1 Trigger Request
2	out	Group 2 Trigger Request
3	out	Group 3 Trigger Request
4	out	Group 4 Trigger Request
5	out	Group 5 Trigger Request
6	out	Group 6 Trigger Request
7	out	Group 7 Trigger Request
8	out	Memory Full
9	out	Event Data Ready
10	out	Channels Trigger
11	out	RUN Status
12	in	Trigger Time Tag Reset (active low)
13	in	Memory Clear (active low)
14	-	RESERVED
15	-	RESERVED

3.6. Test pattern generator

The FPGA AMC can emulate the ADC and write into memory a ramp (0, 1, 2, 3,...3FFF, 3FFF, 3FFE..., 0) for test purposes. It can be enabled via Channel Configuration register, see § 4.9.

3.7. Analog Monitor

The board houses a 12bit (100MHz) DAC with 0÷1 V dynamics on a 50 Ohm load (see Fig. 1.1), whose input is controlled by the ROC FPGA and the signal output (driving 50 Ohm) is available on the MON/Σ output connector. MON output of more boards can be summed by an external Linear Fan In. This output is delivered by a 12 bit DAC.

The DAC control logic implements four operating modes:

- Trigger Majority Mode (Monitor Mode = 0)
- Test Mode (Monitor Mode = 1)
- Buffer Occupancy Mode (Monitor Mode = 3)
- Voltage Level Mode (Monitor Mode = 4)

Operating mode is selected via Monitor Mode register (see § 4.28); Monitor Mode = 2 is reserved for future implementation.

3.7.1. Trigger Majority Mode (Monitor Mode = 0)

It is possible to generate a Majority signal with the DAC: the MON output provides a signal whose amplitude is proportional to the number of “triggering groups” (the groups enabled to generate the local trigger, where at least one of the enabled channels in the

group has exceeded the programmed threshold; see § 4.3, § 4.9 and § 4.18), 1 step = 1.25mV. This allows, via an external discriminator, to produce a global trigger signal, as the resulting “majority” has exceeded a particular threshold.

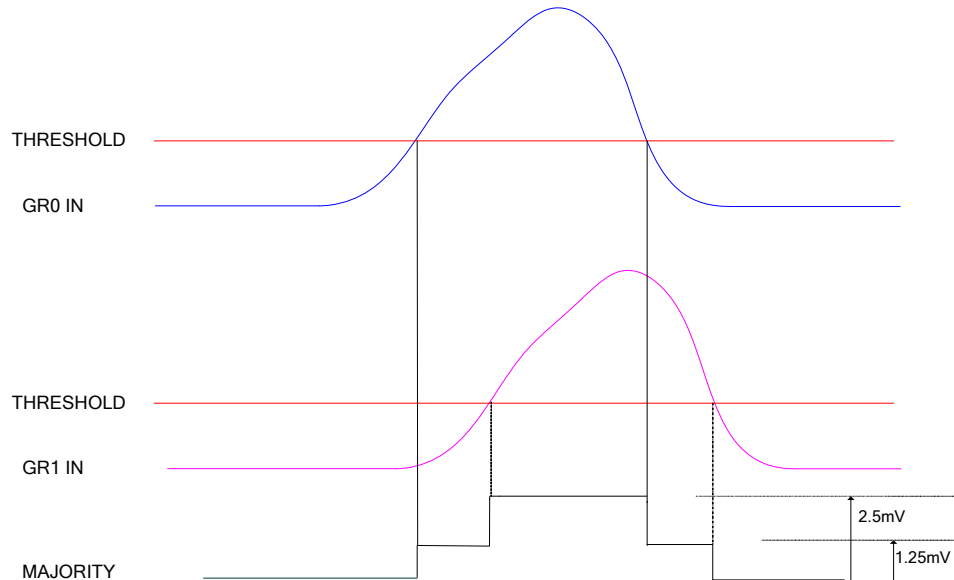


Fig. 3.12: Majority logic (2 triggering groups; “polarity” bit[6] of Gr. Config. Reg. =0)

3.7.2. Test Mode (Monitor Mode = 1)

In this mode the MON output provides a sawtooth signal with 1 V amplitude and 30.518 Hz frequency.

3.7.3. Buffer Occupancy Mode (Monitor Mode = 3)

In this mode, MON out provides a voltage value proportional to the number of buffers filled with events; step: 1 buffer = 0.976 mV. .

This mode allows to test the readout efficiency: in fact if the average event readout throughput is as fast as trigger rate, then MON out value remains constant; otherwise if MON out value grows in time, this means that readout rate is slower than trigger rate.

3.7.4. Voltage Level Mode (Monitor Mode = 4)

In this mode, MON out provides a voltage value programmable via the 'N' parameter written in the SET MONITOR DAC register, with: $V_{mon} = 1/4096 * N$ (Volt).

3.8. Reset, Clear and Default Configuration

3.8.1. Global Reset

Global Reset is performed at Power ON of the module or via a VME RESET (SYS_RES), see § 4.39. It allows to clear the data off the Output Buffer, the event counter and

performs a FPGAs global reset, which restores the FPGAs to the default configuration. It initializes all counters to their initial state and clears all detected error conditions.

3.8.2. Memory Reset

The Memory Reset clears the data off the Output Buffer.

The Memory Reset can be forwarded via either a write access to Software Clear Register (see § 4.40) or with a pulse sent to the front panel Memory Clear input (see § 3.5).

3.8.3. Timer Reset

The Timer Reset allows to initialize the timer which allows to tag an event. The Timer Reset can be forwarded with a pulse sent to Trigger Time Tag Reset input (see § 3.5).

3.9. VMEBus interface

The module is provided with a fully compliant VME64/VME64X interface (see § 1.1), whose main features are:

- EUROCARD 9U Format
- J1/P1 and J2/P2 with either 160 pins (5 rows) or 96 (3 rows) connectors
- A24, A32 and CR-CSR address modes
- D32, BLT/MBLT, 2eVME, 2eSST data modes
- MCST write capability
- CBLT data transfers
- RORA interrupter
- Configuration ROM

3.9.1. Addressing capabilities

3.9.1.1. Base address

The module works in A24/A32 mode. The Base Address of the module can be fixed through four rotary switches (see § 2.6) and is written into a word of 24 or 32 bit.

The Base Address can be selected in the range:

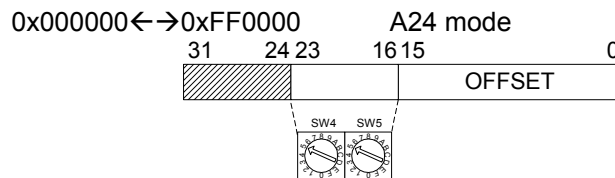


Fig. 3.13: A24 addressing

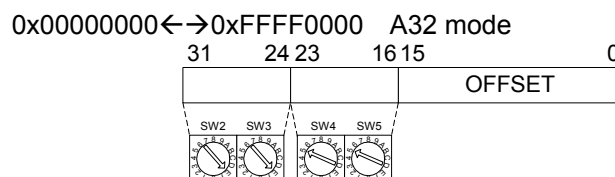


Fig. 3.14: A32 addressing

The Base Address of the module is selected through four rotary switches (see § 2.6), then it is validated only with either a Power ON cycle or a System Reset (see § 3.6).

3.9.1.2. CR/CSR address

GEO address is picked up from relevant backplane lines and written onto bit 23..19 of CR/CSR space, indicating the slot number in the crate; the recognized Address Modifier for this cycle is 2F. *This feature is implemented only on versions with 160pin connectors.*

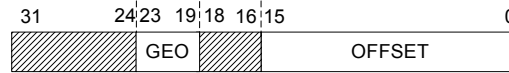


Fig. 3.15: CR/CSR addressing

3.9.1.3. Address relocation

Relocation Address register (see § 4.34) allows to set via software the board Base Address (valid values $\neq 0$). Such register allows to overwrite the rotary switches settings; its setting is enabled via VME Control Register (see § 4.26). The used addresses are:

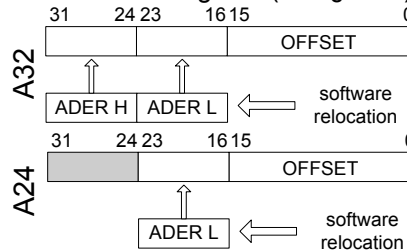


Fig. 3.16: Software relocation of base address

3.10. Data transfer capabilities

The board supports D32 single data readout, Block Transfer BLT32 and MBLT64, 2eVME and 2eSST cycles. Sustained readout rate is up to 60 MB/s with MBLT64, up to 100 MB/s with 2eVME and up to 160 MB/s with 2eSST.

3.11. Events readout

3.11.1. Sequential readout

The events, once written in the SRAMs (Memory Event Buffers), become available for readout via VME. During the memory readout, the board can continue to store more events (independently from the readout) on the free buffers. The acquisition process is therefore “deadtimeless”, until the memory becomes full.

Although the memories are SRAMs, VMEBus does not handle directly the addresses, but takes them from a FIFO. Therefore, data are read from the memories sequentially, according to the selected Readout Logic, from a memory space mapped on 4Kbytes (0x0000÷0x0FFC).

The events are readout sequentially and completely, starting from the Header of the first available event, followed by the Trigger Time Tag, the Event Counter and all the samples of the channels (from 0 to 7). Once an event is completed, the relevant memory buffer

becomes free and ready to be written again (old data are lost). After the last word in an event, the first word (Header) of the subsequent event is readout. It is not possible to readout an event partially.

3.11.1.1. SINGLE D32

This mode allows to readout a word per time, from the header (actually 4 words) of the first available event, followed by all the words until the end of the event, then the second event is transferred. The exact sequence of the transferred words is shown in § 3.3.4. We suggest, after the 1st word is transferred, to check the Event Size information and then do as many D32 cycles as necessary (actually Event Size -1) in order to read completely the event.

3.11.1.2. BLOCK TRANSFER D32/D64, 2eVME

BLT32 allows, via a single channel access, to read N events in sequence, N is set via the BLT Event Number register (see § 4.37).

The event size depends on the Buffer Organization Register setting (§ 4.13); namely:

$$[\text{Event Size}] = [8 * (\text{Block Size})] + [16 \text{ bytes}]$$

Smaller event size can be achieved via Custom Size setting (see § 4.14).

Then it is necessary to perform as many cycles as required in order to readout the programmed number of events.

We suggest to enable BERR signal during BLT32 cycles, in order to end the cycle avoiding filler readout. The last BLT32 cycle will not be completed, it will be ended by BERR after the #N event in memory is transferred (see example in the figure below).

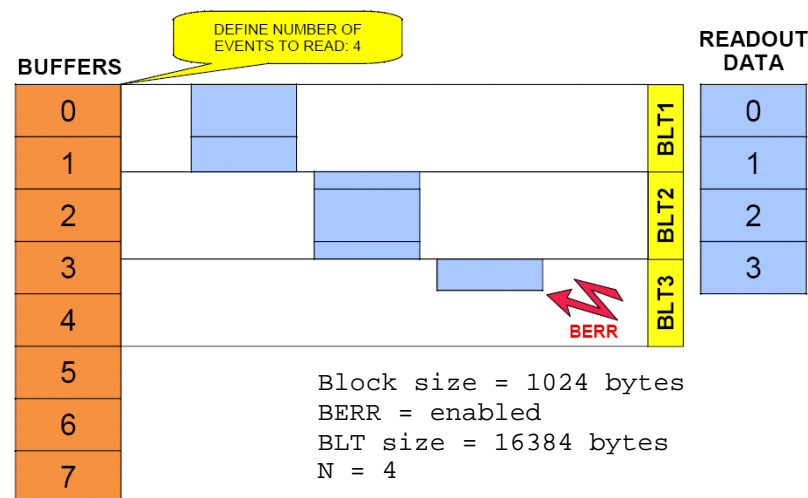


Fig. 3.17: Example of BLT readout

Since some 64 bit CPU's cut off the last 32 bit word of a transferred block, if the number of words composing such block is odd, it is necessary to add a dummy word (which has then to be removed via software) in order to avoid data loss. This can be achieved by setting the ALIGN64 bit in the VME Control register (see § 4.26).

MBLT64 cycle is similar to the BLT32 cycle, except that the address and data lines are multiplexed to form 64 bit address and data buses.

The 2eVME allows to achieve higher transfer rates thanks to the requirement of only two edges of the two control signals (DS and DTACK) to complete a data cycle.

3.11.1.3. CHAINED BLOCK TRANSFER D32/D64

The V1740 allows to readout events from more daisy chained boards (Chained Block Transfer mode).

The technique which handles the CBLT is based on the passing of a token between the boards; it is necessary to verify that the used VME crate supports such cycles.

Several contiguous boards, in order to be daisy chained, must be configured as "first", "intermediate" or "last" via MCST Base Address and Control Register (see § 4.33□□). A common Base Address is then defined via the same register; when a BLT cycle is executed at the address $CBLT_Base + 0x0000 \div 0x0FFC$, the "first" board starts to transfer its data, driving DTACK properly; once the transfer is completed, the token is passed to the second board via the IACKIN-IACKOUT lines of the crate, and so on until the "last" board, which completes the data transfer and asserts BERR (which has to be enabled): the Master then ends the cycle and the slave boards are rearmed for a new acquisition.

If the size of the BLT cycle is smaller than the events size, the board which has the token waits for another BLT cycle to begin (from the point where the previous cycle has ended).

3.11.2. Event Polling

A read access to Event Size register (see § 4.28) allows "polling" the number of 32 bit words composing the next event to be read: this permits to perform a properly sized (according to the Event Size information) BLT readout from the Memory Event Buffer.

3.12. Optical Link

The board houses a daisy chainable Optical Link (communication path which uses optical fiber cables as physical transmission line) able to transfer data at 80 MB/s, therefore it is possible to connect up to eight V1740 to a single Optical Link Controller: for more information, see www.caen.it (path: Products / Front End / PCI/PCIe / Optical Controller)

The parameters for read/write accesses via optical link are the same used by VME cycles (Address Modifier, Base Address, data Width, etc); wrong parameter settings cause Bus Error.

VME Control Register bit 3 allows to enable the module to broadcast an interrupt request on the Optical Link; the enabled Optical Link Controllers propagate the interrupt on the PCI bus as a request from the Optical Link is sensed.

VME and Optical Link accesses take place on independent paths and are handled by board internal controller, with VME having higher priority; anyway it is better to avoid accessing the board via VME and Optical Link simultaneously.

3.13. Software tools

CAEN provides a library designed to control all kind of digitizer models: the CAENDigitizer, available for both Linux and Windows platform (32 and 64Bits).

The library is oriented to C/C++ programmers and for Labview developers.

The CAENDigitizer is in its turn implemented on a lower-level library, the CAENComm as described in the picture below:

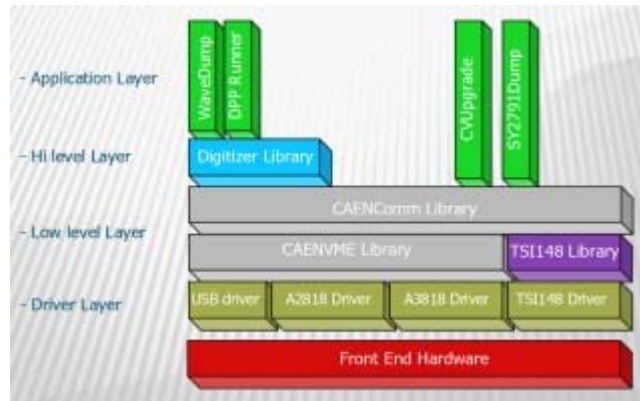



Fig. 3.18: Block diagram of the software tools

Demo software applications that use CAENDigitizer library and tools to upgrade the digitizers firmware (based on the CAENComm library) are also available; all demos and high-level programs are provided with their source code and can be used as a starting point for the development of User-specific applications. For more information about the CAENDigitizer, the CAENComm and all the high-level software for this digitizer, please see www.caen.it website (Software download section).

4. VME Interface

The following sections will describe in detail the board's VME-accessible registers content.

 N.B.: bit fields that are not described in the register bit map are reserved and must not be over written by the User.

4.1. Registers address map

Table 4.1: Address Map for the Model V1740

REGISTER NAME	ADDRESS	ASIZE	DSIZE	MODE	H_RES	S_RES	CLR
EVENT READOUT BUFFER	0x0000-0x0FFC	A24/A32/A64	D32	R	X	X	X
Group n THRESHOLD	0x1n80	A24/A32	D32	R/W	X	X	
<i>Reserved</i>	0x1n84						
Group n STATUS	0x1n88	A24/A32	D32	R	X	X	
Group n AMC FPGA FIRMWARE REVISION	0x1n8C	A24/A32	D32	R			
Group n BUFFER OCCUPANCY	0x1n94	A24/A32	D32	R	X	X	X
Group n DAC	0x1n98	A24/A32	D32	R/W	X	X	
Group n ADC CONFIGURATION	0x1n9C	A24/A32	D32	R/W	X	X	
Group n CHANNEL TRIGGER ENABLE MASK	0x1nA8	A24/A32	D32	R/W	X	X	
Group CONFIGURATION	0x8000	A24/A32	D32	R/W	X	X	
Group CONFIGURATION BIT SET	0x8004	A24/A32	D32	W	X	X	
Group CONFIGURATION BIT CLEAR	0x8008	A24/A32	D32	W	X	X	
BUFFER ORGANIZATION	0x800C	A24/A32	D32	R/W	X	X	
CUSTOM SIZE	0x8020	A24/A32	D32	R/W	X	X	
ACQUISITION CONTROL	0x8100	A24/A32	D32	R/W	X	X	
ACQUISITION STATUS	0x8104	A24/A32	D32	R			
SW TRIGGER	0x8108	A24/A32	D32	W			
TRIGGER SOURCE ENABLE MASK	0x810C	A24/A32	D32	R/W	X	X	
FRONT PANEL TRIGGER OUT ENABLE MASK	0x8110	A24/A32	D32	R/W	X	X	
POST TRIGGER SETTING	0x8114	A24/A32	D32	R/W	X	X	
FRONT PANEL I/O DATA	0x8118	A24/A32	D32	R/W	X	X	
FRONT PANEL I/O CONTROL	0x811C	A24/A32	D32	R/W	X	X	
Group ENABLE MASK	0x8120	A24/A32	D32	R/W	X	X	

REGISTER NAME	ADDRESS	ASIZE	DSIZE	MODE	H_RES	S_RES	CLR
ROC FPGA FIRMWARE REVISION	0x8124	A24/A32	D32	R			
EVENT STORED	0x812C	A24/A32	D32	R	X	X	X
SET MONITOR DAC	0x8138	A24/A32	D32	R/W	X	X	
BOARD INFO	0x8140	A24/A32	D32	R			
MONITOR MODE	0x8144	A24/A32	D32	R/W	X	X	
EVENT SIZE	0x814C	A24/A32	D32	R	X	X	X
VME CONTROL	0xEF00	A24/A32	D32	R/W	X		
VME STATUS	0xEF04	A24/A32	D32	R			
BOARD ID	0xEF08	A24/A32	D32	R/W	X	X	
MULTICAST BASE ADDRESS & CONTROL	0xEF0C	A24/A32	D32	R/W	X		
RELOCATION ADDRESS	0xEF10	A24/A32	D32	R/W	X		
INTERRUPT STATUS ID	0xEF14	A24/A32	D32	R/W	X		
INTERRUPT EVENT NUMBER	0xEF18	A24/A32	D32	R/W	X	X	
BLT EVENT NUMBER	0xEF1C	A24/A32	D32	R/W	X	X	
SCRATCH	0xEF20	A24/A32	D32	R/W	X	X	
SW RESET	0xEF24	A24/A32	D32	W			
SW CLEAR	0xEF28	A24/A32	D32	W			
FLASH ENABLE	0xEF2C	A24/A32	D32	R/W	X		
FLASH DATA	0xEF30	A24/A32	D32	R/W	X		
CONFIGURATION RELOAD	0xEF34	A24/A32	D32	W			
CONFIGURATION ROM	0xF000-0xF3FC	A24/A32	D32	R			

4.2. Configuration ROM (0xF000-0xF084; r)

The following registers contain some module's information, they are D32 accessible (read only):

- **OUI:** manufacturer identifier (IEEE OUI)
- **Version:** purchased version
- **Board ID:** Board identifier
- **Revision:** hardware revision identifier
- **Serial MSB:** serial number (MSB)
- **Serial LSB:** serial number (LSB)

Table 4.2: ROM Address Map for the Model V1740

Description	Address	Content
checksum	0xF000	0xA4
checksum_length2	0xF004	0x00
checksum_length1	0xF008	0x00
checksum_length0	0xF00C	0x20
constant2	0xF010	0x83
constant1	0xF014	0x84
constant0	0xF018	0x01
c_code	0xF01C	0x43
r_code	0xF020	0x52
oui2	0xF024	0x00
oui1	0xF028	0x40
oui0	0xF02C	0xE6
vers	0xF030	V1740, VX1740: 0x11 V1740B, VX1740B: 0x40
board2	0xF034	V1740: 0x00 VX1740: 0x01
board1	0xF038	0x06
board0	0xF03C	0xCC
revis3	0xF040	0x00
revis2	0xF044	0x00
revis1	0xF048	0x00
revis0	0xF04C	0x01
sernum1	0xF080	0x00
sernum0	0xF084	0x16

These data are written into one Flash page; at Power ON the Flash content is loaded into the Configuration RAM, where it is available for readout.

4.3. Group n Threshold (0x1n80; r/w)

Bit	Function
[11:0]	Threshold Value for Trigger Generation

Each Group of channels (Group 0 = Ch0..7, Group 1 = Ch8..15, etc.) can generate a local trigger as the digitized signal exceeds the Vth threshold. This register allows to set Vth (LSB=input range/12bit); see also § 3.4.3.

4.4. Group n Status (0x1n88; r)

Bit	Function
[5]	Buffer free error: 1 = trying to free a number of buffers too large
[4]	GROUPn+1 enabled
[3]	GROUPn enabled
[2]	GROUPn DAC (see § 4.7) Busy 1 = Busy 0 = DC offset updated
[1]	Memory empty
[0]	Memory full

4.5. Group n AMC FPGA Firmware (0x1n8C; r)

Bit	Function
[31:16]	Revision date in Y/M/DD format
[15:8]	Firmware Revision (X)
[7:0]	Firmware Revision (Y)

Bits [31:16] contain the Revision date in Y/M/DD format.

Bits [15:0] contain the firmware revision number coded on 16 bit (X.Y format).

Example: revision 1.3 of 12th June 2007 is: 0x760C0103

4.6. Group n Buffer Occupancy (0x1n94; r)

Bit	Function
[10:0]	Occupied buffers (0..1024)

4.7. Group n DAC (0x1m98; r/w)

Bit	Function
[15:0]	DAC Data

Bits [15:0] allow to define a DC offset to be added the input signal in the $\pm 1V$ range (low range) or in the $\pm 5V$ range (high range), see also § 3.1. There is a DAC serving eight 8-channel groups. Group 0 = Ch0..7, Group 1 = Ch8..15, etc.

When Group n Status bit 2 is set to 0, DC offset is updated (see § 4.4).

4.8. Group n ADC Configuration (0x1n9C; r/w)

Bit	Function
[31:0]	<i>Reserved</i>

4.9. Group n Channel Trigger Mask (0x1nA8; r/w)

Bit	Function
[7]	0 = Channel 7 trigger disabled 1 = Channel 7 trigger enabled
[6]	0 = Channel 6 trigger disabled 1 = Channel 6 trigger enabled
[5]	0 = Channel 5 trigger disabled 1 = Channel 5 trigger enabled
[4]	0 = Channel 4 trigger disabled 1 = Channel 4 trigger enabled
[3]	0 = Channel 3 trigger disabled 1 = Channel 3 trigger enabled
[2]	0 = Channel 2 trigger disabled 1 = Channel 2 trigger enabled
[1]	0 = Channel 1 trigger disabled 1 = Channel 1 trigger enabled
[0]	0 = Channel 0 trigger disabled 1 = Channel 0 trigger enabled

This register bits[0,7] enable the channels, within Group n, to generate a local trigger as the digitized signal exceeds the Vth threshold (see § 3.4.3). Bit0 enables Ch0 to generate the trigger, bit1 enables Ch1 to generate the trigger and so on. In order to generate the trigger, the Group n itself must be enabled via Group Trigger Source Enable Mask (see § 4.18).

4.10. Group Configuration (0x8000; r/w)

Bit	Function
[7]	<i>reserved</i>
[6]	0 = Trigger Output on Input Over Threshold 1 = Trigger Output on Input Under Threshold allows to generate local trigger either on channel over or under threshold (see § 4.3 and § 3.4)
[5]	<i>reserved</i>
[4]	<i>reserved</i> (MUST ALWAYS BE SET TO 1)
[3]	0 = Test Pattern Generation Disabled 1 = Test Pattern Generation Enabled
[2]	<i>reserved</i>
[1]	0 = Trigger Overlapping Not Enabled 1 = Trigger Overlapping Enabled Allows to handle trigger overlap (see § 3.3.3)
[0]	0 = "Window" Gate 1 = "Single Shot" Gate Allows to handle samples validation (see § 3.3.1)

This register allows to perform settings which apply to all groups.

It is possible to perform selective set/clear of the Group Configuration register bits writing to 1 the corresponding set and clear bit at address 0x8004 (set) or 0x8008 (clear) see the following § 4.11 and § 4.12. Default value is 0x10.

4.11. Group Configuration Bit Set (0x8004; w)

Bit	Function
[7..0]	Bits set to 1 means that the corresponding bits in the Group Configuration register are set to 1.

4.12. Group Configuration Bit Clear (0x8008; w)

Bit	Function
[7..0]	Bits set to 1 means that the corresponding bits in the Group Configuration register are set to 0.

4.13. Buffer Organization (0x800C; r/w)

Bit	Function
[3:0]	BUFFER CODE

The BUFFER CODE allows to divide the available Output Buffer Memory into a certain number of blocks, according to the following table:

Table 4.3: Output Buffer Memory block division

CODE	Nr. of blocks	Samples per Block (1 ch.)
0000	1	192K
0001	2	96K
0010	4	48K
0011	8	24K
0100	16	12K
0101	32	6K
0110	64	3K
0111	128	1536
1000	256	768
1001	512	384
1010	1024	192

A write access to this register causes a Software Clear, see § 3.7. This register must not be written while acquisition is running. In order to obtain a number of Samples per Block (from one channel) different from the Table above, it is necessary to use the Custom Size register (0x8020); in this case, the CODE must be set larger than the Custom Size, corresponding to the smallest possible value (for example, set 0111 code, if the desired number of Samples per Block is 900).

4.14. Custom Size (0x8020; r/w)

Bit	Function
[31:0]	0= Custom Size disabled N _{CUS} (≠0) = Allows to set a "Custom" Number of Samples per Block (from one channel); relationship is $N_{CUS} = NSAMPLES * (2/3)$, therefore if the desired number of Samples per Block is 900, this register must be set to 0x258 (only values multiple of 3 are allowed)

This register must not be written while acquisition is running (see § 3.3.3.1).

4.15. Acquisition Control (0x8100; r/w)

Bit	Function
[5]	0 = Normal Mode (default): board becomes full, whenever all buffers are full (see § 4.13) 1 = Always keep one buffer free: board becomes full, whenever N-1 buffers are full; N = nr. of blocks (see § 4.13)
[4]	reserved
[3]	0 = COUNT ACCEPTED TRIGGERS 1 = COUNT ALL TRIGGERS allows to reject overlapping triggers (see § 3.3.3)
[2]	0 = Acquisition STOP 1 = Acquisition RUN allows to RUN/STOP Acquisition
[1:0]	00 = REGISTER-CONTROLLED RUN MODE 01 = S-IN CONTROLLED RUN MODE 10 = S-IN GATE MODE 11 = MULTI-BOARD SYNC MODE

Bit [2] allows to Run and Stop data acquisition; when such bit is set to 1 the board enters Run mode and a Memory Reset (see § 3.8.2) is automatically performed. When bit [2] is reset to 0 the stored data are kept available for readout. In Stop Mode all triggers are neglected.

Bits [1:0] description:

- 00 = REGISTER-CONTROLLED RUN MODE: multiboard synchronization via S_IN front panel signal
- RUN control: start/stop via set/clear of bit[2]
 - GATE always active (Continuous Gate Mode)
 - Continuous Gate Mode can be used only if Gate mode (see § 4.9) is set in Window Mode
- 01 = S-IN CONTROLLED RUN MODE: Multiboard synchronization via S-IN front panel signal
- S-IN works both as SYNC and RUN_START command
 - GATE always active (Continuous Gate Mode):
 - Continuous Gate Mode: Gate always active; to be used only if Gate Mode (GROUP Configuration Register) is set to Window Mode
- 10 = S-IN GATE MODE
- Multiboard synchronization is disabled
 - S-IN works as Gate signal set/clear of RUN/STOP bit
- 11 = MULTI-BOARD SYNC MODE
- Used only for Multiboard synchronization

4.16. Acquisition Status (0x8104; r)

Bit	Function
[8]	Board ready for acquisition (PLL and ADCs are synchronized correctly) 0 = not ready 1 = ready This bit should be checked after software reset to ensure that the board will enter immediately run mode after RUN mode setting; otherwise a latency between RUN mode setting and Acquisition start might occur.
[7]	PLL Status Flag (see § 2.5.1): 0 = PLL loss of lock 1 = no PLL loss of lock NOTE: flag can be restored to 1 via read access to Status Register (see § 4.31)
[6]	PLL Bypass mode (see § 2.5.1): 0 = No bypass mode 1 = Bypass mode
[5]	Clock source (see § 2.6): 0 = Internal 1 = External
[4]	EVENT FULL: it is set to 1 as the maximum nr. of events to be read is reached
[3]	EVENT READY: it is set to 1 as at least one event is available to readout
[2]	0 = RUN off 1 = RUN on
[1:0]	reserved

4.17. Software Trigger (0x8108; w)

Bit	Function
[31:0]	A write access to this location generates a trigger via software

4.18. Trigger Source Enable Mask (0x810C; r/w)

Bit	Function
[31]	0 = Software Trigger Disabled 1 = Software Trigger Enabled
[30]	0 = External Trigger Disabled 1 = External Trigger Enabled
[29:27]	<i>reserved</i>
[26:24]	Local trigger coincidence level (default = 0)
[23:8]	<i>reserved</i>
[7]	0 = Group 7 trigger disabled 1 = Group 7 trigger enabled
[6]	0 = Group 6 trigger disabled 1 = Group 6 trigger enabled
[5]	0 = Group 5 trigger disabled 1 = Group 5 trigger enabled
[4]	0 = Group 4 trigger disabled 1 = Group 4 trigger enabled
[3]	0 = Group 3 trigger disabled 1 = Group 3 trigger enabled
[2]	0 = Group 2 trigger disabled 1 = Group 2 trigger enabled
[1]	0 = Group 1 trigger disabled 1 = Group 1 trigger enabled
[0]	0 = Group 0 trigger disabled 1 = Group 0 trigger enabled

This register bits[0,7] enable the channels to generate a local trigger as the digitized signal exceeds the Vth threshold (see § 3.4.3). Bit0 enables Group0 to generate the trigger, bit1 enables Group1 to generate the trigger and so on.

Bits [26:24] allows to set minimum number of groups with at least one channel over threshold, beyond the triggering group, in order to actually generate the local trigger signal; for example if bit[7:0]=FF (all groups enabled) and Local trigger coincidence level = 1, whenever at least one channel in a group exceeds the threshold, the trigger will be generated only if at least another channel in another group is over threshold at that moment. Local trigger coincidence level must be smaller than the number of groups enabled via bit[7:0] mask.

EXTERNAL TRIGGER ENABLE (bit30) enables the board to sense TRG-IN signals
SW TRIGGER ENABLE (bit 31) enables the board to sense software trigger (see § 4.17).

4.19. Front Panel Trigger Out Enable Mask (0x8110; r/w)

Bit	Function
[31]	0 = Software Trigger Disabled 1 = Software Trigger Enabled
[30]	0 = External Trigger Disabled 1 = External Trigger Enabled
[7]	0 = Group 7 trigger disabled 1 = Group 7 trigger enabled
[6]	0 = Group 6 trigger disabled 1 = Group 6 trigger enabled
[5]	0 = Group 5 trigger disabled 1 = Group 5 trigger enabled
[4]	0 = Group 4 trigger disabled 1 = Group 4 trigger enabled
[3]	0 = Group 3 trigger disabled 1 = Group 3 trigger enabled

Bit	Function
[2]	0 = Group 2 trigger disabled 1 = Group 2 trigger enabled
[1]	0 = Group 1 trigger disabled 1 = Group 1 trigger enabled
[0]	0 = Group 0 trigger disabled 1 = Group 0 trigger enabled

This register bits[0,7] enable the groups to generate a TRG_OUT front panel signal as the digitised signal exceeds the Vth threshold (see § 3.4.3).

Bit0 enables Group0 to generate the TRG_OUT, bit1 enables Group1 to generate the TRG_OUT and so on.

EXTERNAL TRIGGER ENABLE (bit30) enables the board to generate the TRG_OUT
SW TRIGGER ENABLE (bit 31) enables the board to generate TRG_OUT (see § 4.17).

4.20. Post Trigger Setting (0x8114; r/w)

Bit	Function
[31:0]	Post trigger value

The register value sets the number of post trigger samples. The number of post trigger samples is :

$$N_{post} = \text{PostTriggerValue} * 3 + \text{ConstantLatency}$$

where:

N_{post} = number of post trigger samples.

PostTriggerValue = Content of this register.

ConstantLatency = constant number of samples added due to the latency associated to the trigger processing logic in the ROC FPGA.

This value is constant, but the exact value may change between different firmware revisions.

4.21. Front Panel I/O Data (0x8118; r/w)

Bit	Function
[15:0]	Front Panel I/O Data

Allows to Readout the logic level of LVDS I/Os and set the logic level of LVDS Outputs.

4.22. Front Panel I/O Control (0x811C; r/w)

Bit	Function
[15]	0 = I/O Normal operations: TRG-OUT signals outside trigger presence (trigger are generated according to Front Panel Trigger Out Enable Mask setting, see § 4.19) 1 = I/O Test Mode: TRG-OUT is a logic level set via bit 14
[14]	1 = TRG-OUT Test Mode set to 1 0 = TRG-OUT Test Mode set to 0
[9]	PATTERN_LATCH_MODE = 0: PATTERN field into event headers is the status of 16 LVDS Front Panel Inputs latched with board internal trigger (if a post trigger value is set, the internal trigger is delayed respect to external one). = 1: PATTERN field into event headers is the status of 16 LVDS Front Panel Inputs latched with external trigger rising edge.
[7:6]	00 = General Purpose I/O

Bit	Function
	01 = Programmed I/O 10 = Pattern mode: LVDS signals are input and their value is written into header PATTERN field (see § 3.3.4.1)
[5]	0 = LVDS I/O 15..12 are inputs 1 = LVDS I/O 15..12 are outputs
[4]	0 = LVDS I/O 11..8 are inputs 1 = LVDS I/O 11..8 are outputs
[3]	0 = LVDS I/O 7..4 are inputs 1 = LVDS I/O 7..4 are outputs
[2]	0 = LVDS I/O 3..0 are inputs 1 = LVDS I/O 3..0 are outputs
[1]	0 = panel output signals (TRG-OUT/CLKOUT) enabled 1 = panel output signals (TRG-OUT/CLKOUT) enabled in high impedance
[0]	0 = TRG/CLK are NIM I/O Levels 1 = TRG/CLK are TTL I/O Levels

Bits [5:2] are meaningful for General Purpose I/O use only

4.23. Group Enable Mask (0x8120; r/w)

Bit	Function
[7]	0 = Group 7 disabled 1 = Group 7 enabled
[6]	0 = Group 6 disabled 1 = Group 6 enabled
[5]	0 = Group 5 disabled 1 = Group 5 enabled
[4]	0 = Group 4 disabled 1 = Group 4 enabled
[3]	0 = Group 3 disabled 1 = Group 3 enabled
[2]	0 = Group 2 disabled 1 = Group 2 enabled
[1]	0 = Group 1 disabled 1 = Group 1 enabled
[0]	0 = Group 0 disabled 1 = Group 0 enabled

Enabled groups provide the samples which are stored into the events (and not erased). The mask cannot be changed while acquisition is running.

4.24. ROC FPGA Firmware Revision (0x8124; r)

Bit	Function
[31:16]	Revision date in Y/M/DD format
[15:8]	Firmware Revision (X)
[7:0]	Firmware Revision (Y)

Bits [31:16] contain the Revision date in Y/M/DD format.

Bits [15:0] contain the firmware revision number coded on 16 bit (X.Y format).

4.25. Event Stored (0x812C; r)

Bit	Function
[31:0]	This register contains the number of events currently stored in the Output Buffer

This register value cannot exceed the maximum number of available buffers according to setting of buffer size register.

4.26. Set Monitor DAC (0x8138; r/w)

Bit	Function
[11:0]	This register allows to set the DAC value (12bit)

This register allows to set the DAC value in Voltage level mode (see § 2.7).
LSB = 0.244 mV, terminated on 50 Ohm.

4.27. Board Info (0x8140; r)

Bit	Function
[15:8]	Memory size (Mbyte/Group)
[7:0]	Board Type: 0 = V1740

4.28. Monitor Mode (0x8144; r/w)

Bit	Function
[2:0]	This register allows to encode the Analog Monitor (see § 3.7) operation: 000 = majority 001 = waveform generator (saw tooth ramp) 010 = <i>reserved</i> 011 = buffer occupancy 100 = voltage level

4.29. Event Size (0x814C; r)

Bit	Function
[31:0]	Nr. of 32 bit words in the next event

4.30. VME Control (0xEF00; r/w)

Bit	Function
[7]	0 = Release On Register Access (RORA) Interrupt mode (default) 1 = Release On AcKnowledge (ROAK) Interrupt mode
[6]	0 = RELOC Disabled (BA is selected via Rotary Switch; see § 2.6) 1 = RELOC Enabled (BA is selected via RELOC register; see § 4.34)
[5]	0 = ALIGN64 Disabled

	1 = ALIGN64 Enabled (see § 3.11.1.2)
[4]	0 = BERR Not Enabled; the module sends a DTACK signal until the CPU inquires the module 1 = BERR Enabled; the module is enabled either to generate a Bus error to finish a block transfer or during the empty buffer read out in D32
[3]	0 = Optical Link interrupt disabled 1 = Optical Link interrupt enabled
[2 :0]	Interrupt level (0= interrupt disabled)

Bit [7]: this setting is valid only for interrupts broadcasted on VMEbus; interrupts broadcasted on optical link feature RORA mode only.

- In RORA mode, interrupt status can be removed by accessing VME Control register (see § 4.30) and disabling the active interrupt level.
- In ROAK mode, interrupt status is automatically removed via an interrupt acknowledge cycle. Interrupt generation is restored by setting an Interrupt level > 0 via VME Control register.

4.31. VME Status (0xEF04; r)

Bit	Function
[3]	0 = VME FIFO not empty; 1 = VME FIFO empty
[2]	0 = BERR FLAG: no Bus Error has occurred 1 = BERR FLAG: a Bus Error has occurred (this bit is re-set after a status register read out)
[1]	Reserved
[0]	0 = No Data Ready; 1 = Event Ready

4.32. Board ID (0xEF08; r/w)

Bit	Function
[4 :0]	GEO

- VME64X versions: this register can be accessed in read mode only and contains the GEO address of the module picked from the backplane connectors; when CBLT is performed, the GEO address will be contained in the EVENT HEADER Board ID field (see § 3.3.4.1).
- Other versions: this register can be accessed both in read and write mode; it allows to write the correct GEO address (default setting = 0) of the module before CBLT operation. GEO address will be contained in the EVENT HEADER Board ID field.

4.33. MCST Base Address and Control (0xEF0C; r/w)

Bit	Function
[7:0]	These bits contain the most significant bits of the MCST/CBLT address of the module set via VME, i.e. the address used in MCST/CBLT operations.
[9:8]	Allows to set up the board for daisy chaining: 00 = disabled board 01 = last board 10 = first board 11 = intermediate

4.34. Relocation Address (0xEF10; r/w)

Bit	Function
[15..0]	These bits contains the A31...A16 bits of the address of the module: it can be set via VME for a relocation of the Base Address of the module.

4.35. Interrupt Status ID (0xEF14; r/w)

Bit	Function
[31..0]	This register contains the STATUS/ID that the module places on the VME data bus during the Interrupt Acknowledge cycle

4.36. Interrupt Event Number (0xEF18; r/w)

Bit	Function
[9..0]	INTERRUPT EVENT NUMBER

If interrupts are enabled, the module generates a request whenever it has stored in memory a Number of events > INTERRUPT EVENT NUMBER

4.37. BLT Event Number (0xEF1C; r/w)

Bit	Function
[7:0]	This register contains the number of complete events which has to be transferred via BLT/CBLT (see § 3.11.1.2).

4.38. Scratch (0xEF20; r/w)

Bit	Function
[31:0]	Scratch (<i>to be used to write/read words for VME test purposes</i>)

4.39. Software Reset (0xEF24; w)

Bit	Function
[31:0]	A write access to this location allows to perform a software reset

4.40. Software Clear (0xEF28; w)

Bit	Function
[31:0]	A write access to this location clears all the memories

4.41. Flash Enable (0xEF2C; r/w)

Bit	Function
0	0 = Flash write ENABLED 1 = Flash write DISABLED

This register is handled by the Firmware upgrade tool.

4.42. Flash Data (0xEF30; r/w)

Bit	Function
[7:0]	Data to be serialized towards the SPI On board Flash

This register is handled by the Firmware upgrade tool.

4.43. Configuration Reload (0xEF34; w)

Bit	Function
[31:0]	A write access to this register causes a software reset (see § 3.6), a reload of Configuration ROM parameters and a PLL reconfiguration.

5. Installation

- The Mod. V1740 fits into 6U VME crates.
- **The V1740 cannot be operated with CAEN crates VME8001/8002/8004/8004A**
- VX1740 versions require VME64X compliant crates
- Use only crates with forced cooling air flow
- Turn the crate OFF before board insertion/removal
- Remove all cables connected to the front panel before board insertion/removal



CAUTION

**USE ONLY CRATES WITH FORCED COOLING AIR FLOW SINCE OVERHEAT MAY
DAMAGE THE MODULE!**



CAUTION

**ALL CABLES MUST BE REMOVED FROM THE FRONT PANEL
BEFORE EXTRACTING THE BOARD FROM THE CRATE!**

5.1. Power ON sequence

To power ON the board follow this procedure:

1. insert the V1740 board into the crate
2. power up the crate

5.2. Power ON status

At power ON the module is in the following status:

- the Output Buffer is cleared;
- registers are set to their default configuration (see § 3.12)

5.3. Firmware upgrade

The board can store two firmware versions, called STD and BKP respectively; at Power On, a microcontroller reads the Flash Memory and programs the module with the firmware version selected via the JP2 jumper (see § 2.6), which can be placed either on the STD position (left), or in the BKP position (right). It is possible to upgrade the board

firmware via VME, by writing the Flash; for this purpose, download the software package available at www.caen.it/ website

The package includes the new firmware release file:

- v1740_revX.Y_W.Z..rbf

and the V1740 firmware upgrade tool:

- CVUpgrade.exe (windows executable)
- CVUpgrade tool (source code and VC++ project)

For upgrading the firmware, utilizing CVUpgrade.exe, open a DOS shell, then launch
CVUpgrade FileName BaseAdd [image] [/fast] [/nover]

where:

- **FileName** is the RBF file
- **BaseAdd** is the Base Address (Hex 32 bit) of the V1740
- **image** is 'standard' (default) or 'backup'
- **'fast'** enables fast programming (MultiRead/Write with CAEN Bridge)
- **'nover'** disables programming check

N.B.: it is strongly suggested to upgrade **ONLY** one of the stored firmware revisions (generally the **STD** one): if both revision are simultaneously updated, and a failure occurs, it will not be possible to upload the firmware via VME again!

5.3.1. V1740 Upgrade files description

The board hosts one FPGA on the mainboard and one FPGA for each of the eight "channel groups". The channel group FPGAs firmware is identical. A unique file is provided that will updated all the FPGA at the same time.

ROC FPGA MAINBOARD FPGA (Readout Controller + VME interface)
FPGA Altera Cyclone EP1C20.

AMC FPGA GROUP FPGA (ADC readout/Memory Controller):
FPGA Altera Cyclone EP3C16

All FPGAs can be upgraded via VMEBUS;

CVUpgrade utility program must be used for this purpose.

The programming file has the extension RBF and its name follows this general scheme:

v1740_revX.Y_W.Z.RBF

where:

- X.Y is the major/minor revision number of the mainboard FPGA
- W.Z is the major/minor revision number of the channel group FPGA

WARNING: the previous FW revision can be restored in case there is a failure when the upgrading program runs. There is a jumper on the mainboard that allows to select the

"backup" copy of the firmware. All the FPGAs must be upgraded and the revisions kept aligned; it is not guaranteed that the latest revision of one FPGA is compatible with an older revision.

Upgrade examples:

1) Upgrade to Rev 1.0(main FPGA)/Rev 0.2 (channel group FPGA) of the standard page of the V1740:

```
CVUpgrade v1740_rev1.0_0.2.rbf 32100000 /standard
```

2) Upgrade to Rev 1.0(main FPGA)/Rev 0.2 (channel group FPGA) of the backup page of the V1740:

```
CVUpgrade v1740_rev1.0_0.2.rbf 32100000 /backup
```

3) Upgrade to Rev 1.0(main FPGA)/Rev 1.1 (channel group FPGA) of the standard page of the V1740:

```
CVUpgrade v1740_rev1.0_1.1.rbf 32100000 /standard
```