TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1. DESCRIPTION

1.1. FUNCTIONAL DESCRIPTION

The CAEN Model V258B is a 16 CHANNEL PROGRAMMABLE DISCRIMINATOR housed in a 1-unit wide VME module (a functional block diagram is shown in Fig. 1.1).

The module accepts 16 negative inputs via 16 front panel LEMO 00 type connectors (INPUTS 0 to 15) and produces 32 differential ECL outputs (with a FAN-OUT of two for each channel) that are available on four front panel flat cable connectors (OUTPUTS 0 to 7 A and B, OUTPUTS 8 to 15 A and B. The B outputs are buffered, the A outputs are not buffered).

Each channel consists of a discriminator on a hybrid circuit and an 8-bit DAC for the threshold setting.

The Timing Stage of the discriminator works in UPDATING mode. It produces an output pulse whose width is independent from the input signal time over threshold and adjustable in two ranges via the front panel common trimmer WDT (16 internal jumpers, one per channel, allow the range setting).

Each channel has its own discriminating threshold programmable via VME, and can be turned on or off via VME. The thresholds can be set in a range from 0 mV to -510 mV (-2 mV step), though for proper functioning a minimum threshold of -6 mV is required.

The module operations are fully controlled via VME. Some operations can be also performed using two external NIM or TTL signals (indicated on the front panel connectors with "VETO" and "TEST"):

- VETO: an input signal sent through this connector allows vetoing of all channels simultaneously. A veto pulse of width T will veto the input during this time T.

- TEST: a pulse sent through this connector triggers all the enabled channels at once. This useful feature allows a complete test of the module without removing any input cable as well as it allows generation of a pattern of pulses suitable to test any following electronics. Veto has no effect on the TEST pulse, i.e. the enabled channels will provide an output pulse also when a VETO is provided.

These two inputs are at high impedance and each one is provided with two bridged connectors for daisy chaining.

On the front panel there is also available a Current Sum output that generates a current proportional to the input multiplicity, i. e. to the number of channels over threshold, at a rate of -1.5 mA per hit (-75 mV per hit into a 50Ω load) ±10%.

The Model V258B is an A32 D16 VME slave; its Base address is fixed by 6 internal rotary switches. A front panel LED (DTACK) lights up each time the module generates the VME signal DTACK.

The V258B Model uses the P1 and P2 connector of VME and the auxiliary connector for the CERN V430[1] VMEbus crate (Jaux Dataway).

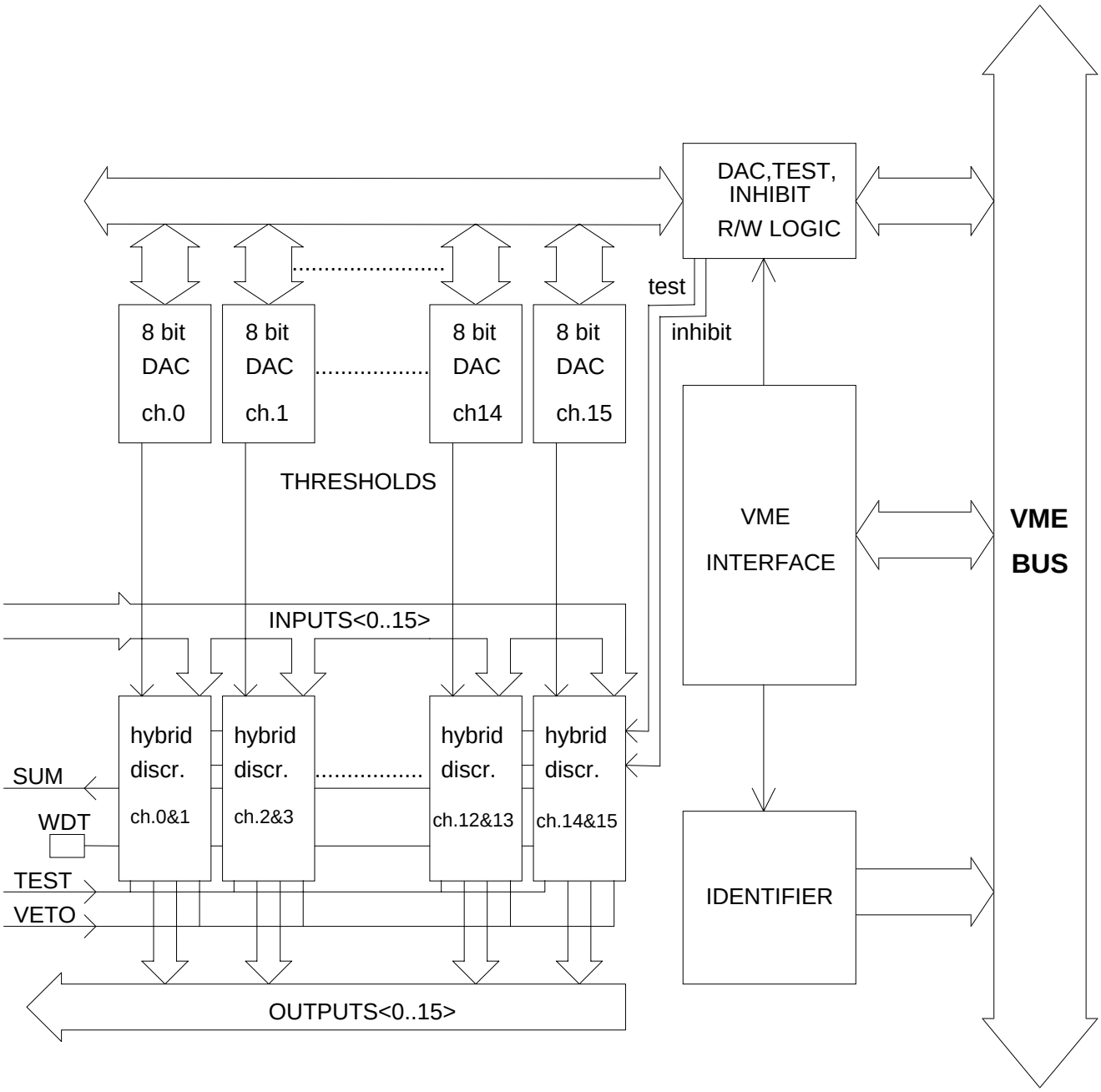


Fig. 1.1: V258B Block Diagram

2. SPECIFICATIONS

2.1. EXTERNAL COMPONENTS

CONNECTORS

- Nr. 16, "INPUTS 0..15", LEMO 00 type. These are the connectors for the input signals.

- Nr. 2, "VETO INPUTS", LEMO 00 type. These are the connectors for the veto input signal that can be daisy chained.

- Nr. 2, "TEST INPUTS", LEMO 00 type. These are the connectors for the test input signal that can be daisy chained.

- Nr. 4, "OUTPUTS 0..7 A & B", "OUTPUTS 8..15 A & B, 16 pin lead flat cable connectors. These connectors deliver the output signals.

- Nr. 1, "SUM OUTPUT", LEMO 00 type. It delivers a current proportional to the input multiplicity, i. e. to the number of channels over threshold, at the rate of -1.5 mA per hit (75 mV per hit into 50 Ω load) ±10%.

DISPLAYS

- Nr. 1, "DTACK", green LED, VME Selected; it lights up during a VME access.

TRIMMERS

- Nr. 1, "WDT", screw-driver trimmer, for the common output signals width adjustment.

2.2. INTERNAL COMPONENTS

JUMPERS

- Nr. 16, two position jumpers JP2..JP5, JP14..JP21, JP30..JP33. These jumpers are dedicated to the range selection of the output signals width, one for each channel.

SWITCHES

- Nr. 6, rotary switches for the module VME BASE address selection.

TRIMMERS (FACTORY SETTINGS)

- Nr. 32, two trimmers per channel to calibrate the two ranges of duration of the output pulse.

- Nr. 16, one trimmer per channel to calibrate an offset for each channel.

- Nr. 1, trimmer T1, to calibrate the reference voltage (512 mV).

2.3. POWER REQUIREMENTS

+ 12 V	0.025 A
- 12 V	0.16 A
+ 5 V	0.6 A
- 5 V	2.5 A

2.4. CHARACTERISTICS OF THE SIGNALS

INPUTS:

- INPUT CHANNELS: negative polarity, 50 Ω impedance;
  minimum pulse width: 3 ns;
  double pulse resolution: 10 ns;
  maximum absolute ratings: ± 5 Volts;
  maximum frequency: 100 MHz.

- VETO(*): std. NIM/TTL level, high impedance;
  minimum width: 15 ns.

- TEST(*): std. NIM/TTL level, high impedance;
  maximum frequency: 30 MHz;
  minimum width: 15 ns.

(*) These inputs are at high impedance and each one is provided with two bridged connectors for daisy chaining. Note that the high impedance makes these inputs sensitive to noise, so the chains have to be terminated on 50 Ω on the last module; the same is needed also if one module only is used, whose inputs have thus to be properly matched.

OUTPUTS:

- CHANNELS: differential ECL level into 100 Ω twisted-pair;
  pulse width continuously adjustable in two ranges: ≅ 5 ÷ 40 ns ;
  ≅ 40 ÷ 300 ns;
  Input/Output delay for group A: 9.2 ns ±10%;
  Input/Output delay for group B: 7.2 ns ± 10%;
  Test/Output delay: 14.2 ns ± 10%;
  Risetimes and Falltimes: < 3 ns.

- CURRENT SUM: high impedance current source;
  current proportional to the input multiplicity;
  rate: -1.5 mA per hit (-75 mV/hit into a 50 Ω load) ±10%;
  maximum rate: 70 MHz (5 ns pulse width).

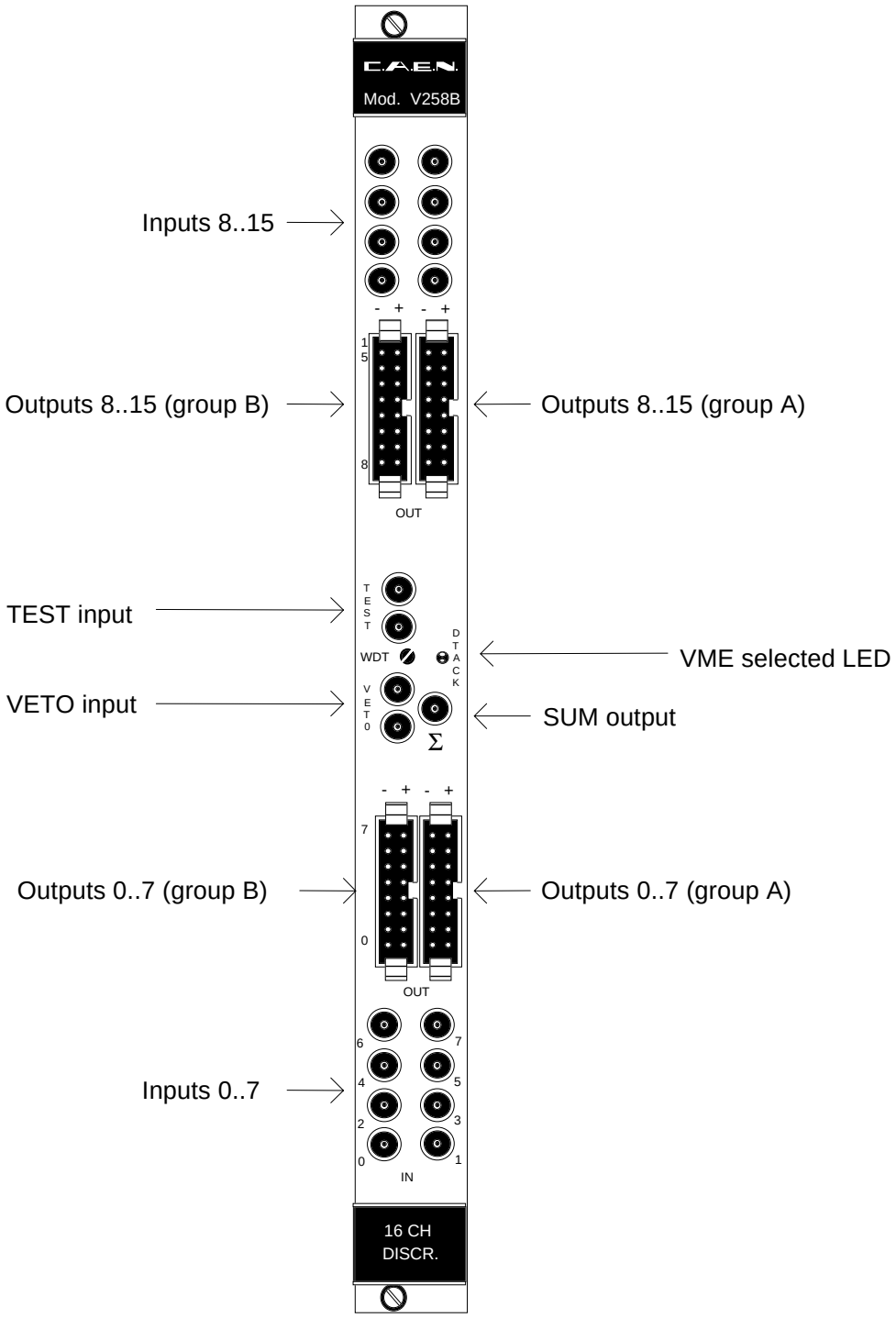
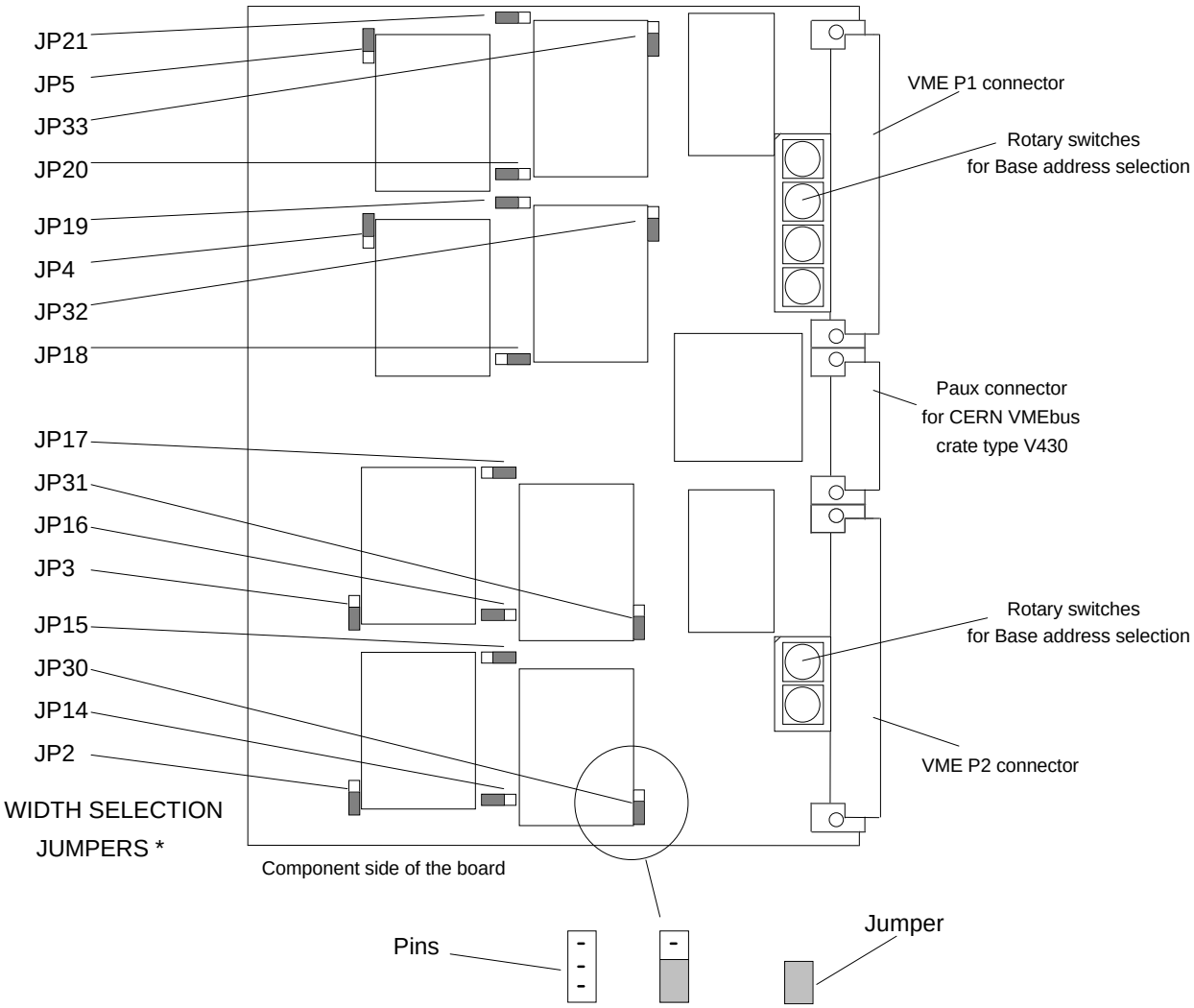


Fig. 2.1: Mod. V258B Front Panel



NB: All these jumpers are located on the soldering side of the PCB

* Short Time selection for the shown jumpers

Fig. 2.2: Mod. V258B Components Locations

3. OPERATING MODES

3.1. ENABLING/DISABLING OF THE CHANNELS

The user can enable or disable each of the 16 channels via VME by writing a 16 bit mask into the address Base + %30 (Pattern of Inhibit). A channel is enabled if the corresponding bit of the mask is high (e. g., bin. 0000000000001100, or hex 000C, enables channels 2 and 3 of the discriminator).

3.2. THRESHOLDS SETTING

The discriminating thresholds can be programmed in a range from 0 mV to -510 mV in -2 mV steps, though for proper functioning a minimum threshold of -6 mV is required. It is possible to set, via VME, independent thresholds for each channel; eight 16 bit registers (T0..T7 for channels 0 to 7 (n, with n = 0..7), T8..T15 for channels 8 to 15 (n+8, with n = 0..7)) are accessible from the VME for the thresholds setting and monitoring. The structure of these registers is shown in the following figure.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Threshold channel n+8								Threshold channel n							

Fig. 3.1: Organization of the threshold registers T0..T15

The bits <7..0> show the actual threshold absolute value of the corresponding channels (n, with n = 0..7), the bits <15..8> show the actual threshold absolute value of the corresponding channels (n+8, with n = 0..7); the weight of the LSB is -2 mV.

The Threshold Registers' addresses range from Base + %10 to Base + %1E.

3.3. OUTPUT PULSES

The width of the output signals does not depend on the time over threshold of the input signals. The front panel trimmer "WDT" allows a common manual adjustment of the output pulses. It is possible, for each channel, to have two adjustment ranges by setting the corresponding jumpers (JP2..JP5, JP14..JP21, JP30..JP33) as previously shown in Fig 2.2 for the short range setting.

The two selectable ranges are:

$\cong$ 5 ns ÷ 40 ns;
$\cong$ 40 ns ÷ 300 ns.

The position of the jumpers can also be deducted from the solderings side of the board: the layout of the board contains a printed pattern with indications on Short Time (ST) or Long Time (LT) setting for the i-th channel (see fig. 3.2). The jumper has to short circuit the middle pin with the desired external pin in the figure 3.2.

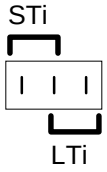


Fig. 3.2: Pattern for the Time Range setting of the i-th channel

3.4. FRONT PANEL SIGNALS

Some operations can be performed by two external NIM signals (indicated on the front panel connectors with "VETO", "TEST"):

- TEST: an input signal sent through this connector triggers all the enabled channels at once. This useful feature allows a complete test of the module without removing any input cable as well as it allows generation of a pattern of pulses suitable to test any following electronics. Veto has no effect on the TEST pulse, i.e. the enabled channels will provide an output pulse also when a VETO is provided.

- VETO: an input signal sent through this connector allows vetoing of all channels simultaneously. A veto pulse of width T will veto the input during this time T.

These inputs are at high impedance and each one is provided with two bridged connectors for daisy chaining.

Note that the high impedance makes these inputs sensitive to noise, so the chain has to be terminated on 50 Ω on the last module; the same is needed also if one module only is used, whose inputs have thus to be properly matched.

On the front panel there is also available a Current Sum output connector that generates a current proportional to the input signal multiplicity, i. e. to the number of channels over threshold, at a rate of -1.5 mA per hit (-75 mV per hit into a 50 Ω load) ±10%.

3.5. CHANNELS TEST

It is possible to obtain pulses on all channels:

- by sending a NIM pulse through one of the two "TEST" connectors located on the front panel.

- by accessing via VME the address Base + %32 (Test: see § 4.1).

N.B.: VETO has no effect on the TEST pulse, i.e. the enabled channels will provide an output pulse also when a VETO is provided.

4. VME INTERFACE

4.1. ADDRESSING CAPABILITY

The V258B module works in A32/A24 mode. This means that the module address must be specified in a field of 32 or 24 bits. The Address Modifiers codes recognized by the module are:

AM=%39:	standard user data access
AM=%3D:	standard supervisor data access
AM=%09:	extended user data access
AM=%0D:	extended supervisor data access

The module's Base Address is fixed by 6 internal rotary switches housed on two piggy-back boards plugged into the main printed circuit board (see Fig. 4.1).

The Base Address can be selected in the range:

% 00 0000 <-> % FF FF00	A24 mode
% 0000 0000 <->% FFFF FF00	A32 mode

The Base Address reserves in this way a page of 256 bytes for the module. The address map of the page is shown in table 4.1.

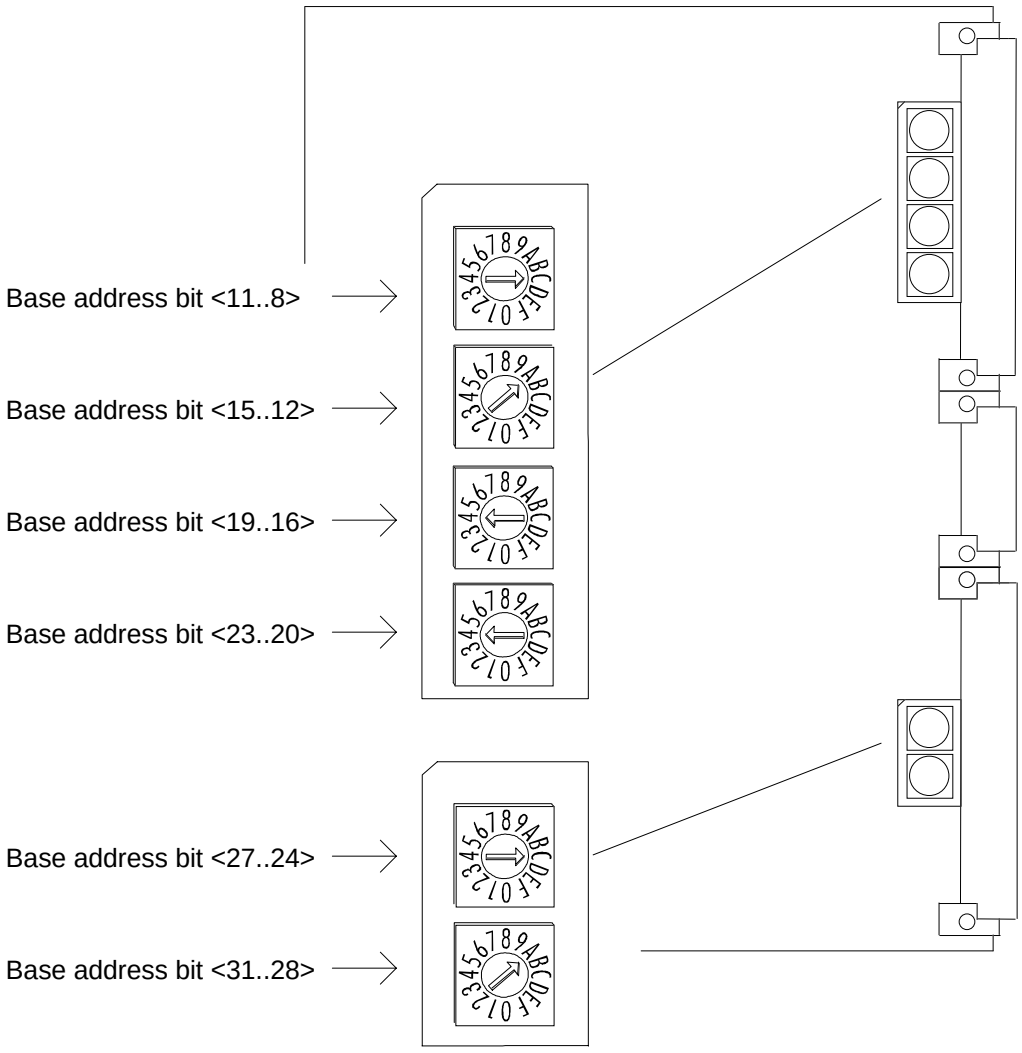


Fig. 4.1: Mod. V258B Base address setting

Table 4.1: Address Map for the Mod. V258B

ADDRESS	REGISTER/CONTENT	TYPE
Base + %FE Base + %FC Base + %FA	Version & Series Manufacturer & Module Type Fixed code	read only read only read only
Base + %F8 . . . Base + %F0	Reserved . . . Reserved	
Base + %EE . . . Base + %40	Not used . . . Not used	
Base + %3E . . . Base + %34	Reserved . . . Reserved	
Base + %32 Base + %30	Test Pattern of Inhibit	write only write only
Base + %2E . . . Base + %20	Not used . . . Not used	
Base + %1E Base + %1C Base + %1A Base + %18 Base + %16 Base + %14 Base + %12 Base + %10	Threshold Register Chan. 15-7 Threshold Register Chan. 14-6 Threshold Register Chan. 13-5 Threshold Register Chan. 12-4 Threshold Register Chan. 11-3 Threshold Register Chan. 10-2 Threshold Register Chan. 9-1 Threshold Register Chan. 8-0	read/write read/write read/write read/write read/write read/write read/write read/write
Base + %0E . . . Base + %00	Not used . . . Not used	

4.2. MODULE IDENTIFIER WORDS

(Base address + %FA ,+%FC, +%FE read only)

The Three words located at the highest address on the page are used to identify the module as shown in figure 4.1:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
Version				Module's serial number												Base + % FE
Manufacturer number						Module type										Base + % FC
%FA Fixed code								%F5 Fixed code								Base + % FA

Fig. 4.2: Module Identifier words

At the address Base + % FA the two particular bytes allow the automatic localization of the module.

For the Mod. V258B the word at address Base + % FC has the following configuration:

Manufacturer N°= 000010 b

Type of module = 0000010110 b

The word located at the address Base + %FE identifies the single module through the module's serial number and any change in the hardware will be shown by the Version number.

5. REFERENCES

[1] G. Bianchetti et al., Specification for VMEbus CRATE Type V430, CERN-EP, January 1990.

APPENDIX A: ELECTRICAL DIAGRAMS

APPENDIX B: COMPONENT LOCATIONS