The Embedded I/O Company

TEWS TECHNOLOGIES

TPMC810

Isolated 2x CAN Bus

Version 1.1

User Manual

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TPMC810-10

Isolated 2x CAN bus, 2x DB9 front panel connector, P14 Back I/O

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0	First Issue	January 2003
1.1	Correction "Configuration EEPROM"	April 2003
1.2	Correction "Configuration EEPROM"	September 2003
1.3	Weight Added and Version	April 2004
1.4	Corrected PCI Base Address Number in Fig. 3-2	October 2005

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1 Product Description

The TPMC810 is a standard single-width 32 bit PMC with two independent CAN bus channels, isolated from system logic and from each other.

Two Philips SJA1000 CAN controllers (CAN specification 2.0B supported) are used.

CAN High Speed transceivers are used for the CAN bus I/O interface. An on board termination option (DIP switch) is provided for each CAN bus channel to configure on board termination and pass through mode for the CAN bus.

Each channel can generate an interrupt on INTA.

The TPMC810 provides front panel I/O via two DB9 male connectors and rear panel I/O via P14.

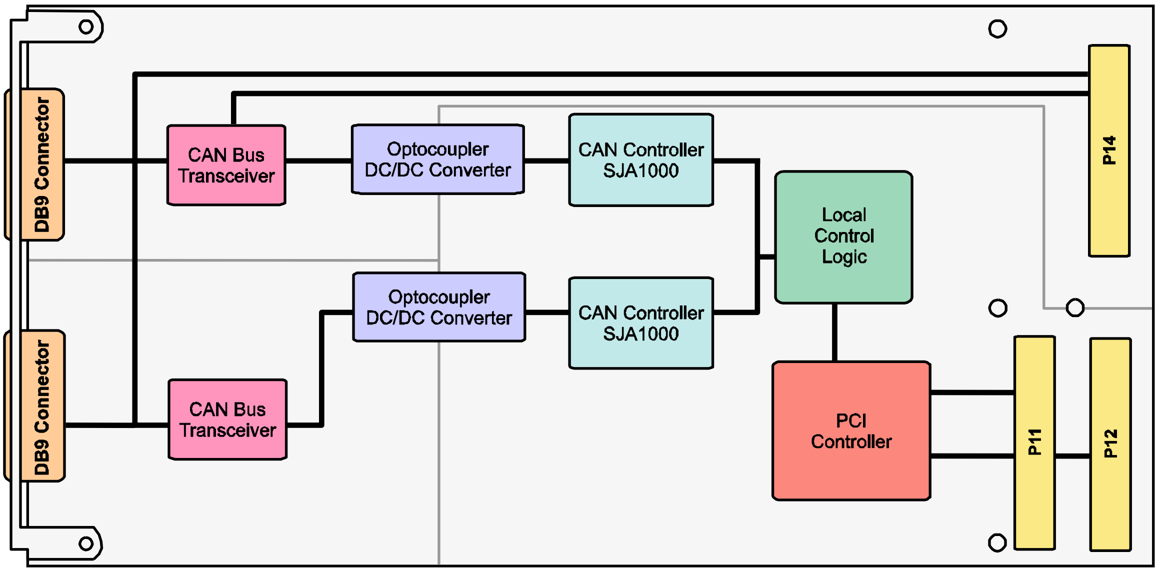

Figure 1-1 : Block Diagram

2 Technical Specification

PMC Interface		
Mechanical Interface	PCI Mezzanine Card (PMC) Interface Single Size	
Electrical Interface	PCI Rev. 2.1 compliant 33 MHz / 32 bit PCI 3.3V and 5V PCI Signaling Voltage	
On Board Devices		
PCI Target Chip	PCI9030 (PLX Technology)	
CAN Controller	2 x SJA1000 @ 16MHz (Philips)	
CAN Transceiver	2 x TJA1050 (Philips)	
I/O Interface		
Number of CAN Bus Channels	2 (Isolated against each other)	
CAN Bus Interface	CAN High Speed (11898-2)	
I/O Connector	PMC P14 I/O (64 pin Mezzanine Connector) 2 x DB9 front panel connector	
Physical Data		
Power Requirements	150mA typical @ +3.3V DC 330mA typical @ +5V DC	
Temperature Range	Operating Storage	-40°C to +85°C -40°C to +125°C
MTBF	404276h	
Humidity	5 – 95 % non-condensing	
Weight	76g	

Figure 2-1 : Technical Specification

3 Local Space Addressing

3.1 PCI9030 Local Space Configuration

The local on board addressable regions are accessed from the PCI side by using the PCI9030 local spaces.

PCI9030 Local Space	PCI9030 PCI Base Address (Offset in PCI Configuration Space)	PCI Space Mapping	Size (Byte)	Port Width (Bit)	Endian Mode	Description
0	2 (0x18)	MEM	512	8	BIG	CAN Controller Address Space
1	3 (0x1C)	-	-	-	-	Not Used
2	4 (0x20)	-	-	-	-	Not Used
3	5 (0x24)	-	-	-	-	Not Used

Figure 3-1 : PCI9030 Local Space Configuration

3.2 CAN Controller Register Address Space

PCI Base Address: PCI9030 PCI Base Address 2 (Offset 0x18 in PCI Configuration Space)

CAN CONTROLLER REGISTER SPACE		
Offset to PCI Base Address 2	**Register Name**	**Size (Bit)**
	CAN Controller Channel 1	
0x000	CAN Controller CH1 Address 0	8
0x001	CAN Controller CH1 Address 1	8
0x002	CAN Controller CH1 Address 2	8
…	…	…
0x07F	CAN Controller CH1 Address 127	8
0x080 … 0x0FF	Reserved	-
	CAN Controller Channel 2	
0x100	CAN Controller CH2 Address 0	8
0x101	CAN Controller CH2 Address 1	8
0x102	CAN Controller CH2 Address 2	8
…	…	…
0x17F	CAN Controller CH2 Address 127	8
0x180 … 0x1FF	Reserved	-

Figure 3-2 : CAN Controller Register Space

3.2.1 SJA1000 CAN Controller Registers

The SJA1000 is controlled via a set of registers (control segment) and a RAM (message buffer).

The following table “Registers of the SJA1000” lists these registers grouped according to their usage in a system, the addresses are decimal values.

Note that some registers are available in PeliCAN Mode only and that the Control Register is available in BasicCAN Mode only. Furthermore some registers are read only or write only and some can be accessed during Reset Mode only.

More information about the registers with respect to read and/or write access, bit definition and reset values, can be found in the data sheet SJA1000 (http://www.semiconductors.philips.com). See also chapter “Programming Hints” for some general register settings.

Type of Usage	Register Name	(Symbol)	Register Address: (decimal)		Functionality
			PeliCAN Mode	BasicCAN Mode	
Elements for selecting different operation modes	Mode	(MOD)	0	—	Sleep-, Acceptance Filter-, Self Test-, Listen Only- and Reset Mode selection
	Control	(CR)	—	0	Reset Mode selection in BasicCAN Mode
	Command	(CMR)	—	1	Sleep Mode command in BasicCAN Mode
	Clock Divider	(CDR)	31	31	Set-up of clock signal at CLKOUT (pin 7) selection of PeliCAN Mode, Comparator Bypass Mode, TX1 (pin 14) Output Mode
Elements for setting up the CAN communication	Acceptance Code, Mask	(ACR) (AMR)	16-19 20-23	4, 5	Selection of bit patterns for Acceptance Filtering
	Bus Timing 0 1	(BTR0) (BTR1)	6 7	6 7	Set-up of Bit Timing Parameters
	Output Control	(OCR)	8	8	Selection of Output Driver properties
Basic elements for the CAN communication	Command	(CMR)	1	1	Commands for Self Reception, Clear Data Overrun, Release Receive Buffer, Abort Transmission and Transmission Request
	Status	(SR)	2	2	Status of message buffers, status of CAN Core Block
	Interrupt	(IR)	3	3	CAN Interrupt flags
	Interrupt Enable	(IER)	4	—	Enable/disable of interrupt events in PeliCAN Mode
	Control	(CR)	—	0	Enable/disable of interrupt events in BasicCAN Mode

Figure 3-3 : Registers of SJA1000

Type of Usage	Register Name (Symbol)	Register Address: (decimal) PeliCAN Mode	Register Address: (decimal) BasicCAN Mode	Functionality
Elements for a comprehensive error detection and analyzing	Arbitration Lost Capture (ALC)	11	—	Shows bit position, where arbitration was lost
	Error Code Capture (ECC)	12	—	Shows last error type and location
	Error Warning Limit (EWLR)	13	—	Selection of threshold for generating an Error Warning Interrupt
	RX Error Counter (RXERR)	14	—	Reflects the current value of the Receive Error Counter
	TX Error Counter (TXERR)	14, 15	—	Reflects the current value of the Transmit Error Counter
	Rx Message Counter (RMC)	29	—	Number of messages in the Receive FIFO
	Rx Buffer Start Addr. (RBSA)	30	—	Shows the current internal RAM address of the message available in the Receive Buffer
Message buffers	Transmit Buffer (TXBUF)	16-28	10-19	
	Receive Buffer (RXBUF)	16-28	20-29	

Figure 3-3 : Registers of the SJA1000 (cont.)

4 PCI9030 Target Chip

4.1 PCI Configuration Registers (PCR)

4.1.1 PCI9030 Header

PCI CFG Register Address	Write '0' to all unused (Reserved) bits				PCI writeable	Initial Values (Hex Values)
	31 24	23 16	15 8	7 0		
0x00	Device ID		Vendor ID		N	032A 1498
0x04	Status		Command		Y	0280 0000
0x08	Class Code			Revision ID	N	028000 00
0x0C	BIST	Header Type	PCI Latency Timer	Cache Line Size	Y[7:0]	00 00 00 00
0x10	PCI Base Address 0 for MEM Mapped Config. Registers				Y	FFFFFF80
0x14	PCI Base Address 1 for I/O Mapped Config. Registers				Y	FFFFFF81
0x18	PCI Base Address 2 for Local Address Space 0				Y	FFFFFE00
0x1C	PCI Base Address 3 for Local Address Space 1				Y	00000000
0x20	PCI Base Address 4 for Local Address Space 2				Y	00000000
0x24	PCI Base Address 5 for Local Address Space 3				Y	00000000
0x28	PCI Cardbus Information Structure Pointer				N	00000000
0x2C	Subsystem ID		Subsystem Vendor ID		N	000A 1498
0x30	PCI Base Address for Local Expansion ROM				Y	00000000
0x34	Reserved			New Cap. Ptr.	N	000000 40
0x38	Reserved				N	00000000
0x3C	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	Y[7:0]	00 00 01 00
0x40	PM Cap.		PM Nxt Cap.	PM Cap. ID	N	4801 00 01
0x44	PM Data	PM CSR EXT	PM CSR		Y	00 00 0000
0x48	Reserved	HS CSR	HS Nxt Cap.	HS Cap. ID	Y[23:16]	00 00 00 06
0x4C	VPD Address		VPD Nxt Cap.	VPD Cap. ID	Y[31:16]	0000 00 03
0x50	VPD Data				Y	00000000

Figure 4-1 : PCI9030 Header

4.1.2 PCI Base Address Initialization

PCI Base Address Initialization is scope of the PCI host software.

PCI9030 PCI Base Address Initialization:

1. Write 0xFFFF_FFFF to the PCI9030 PCI Base Address Register.
2. Read back the PCI9030 PCI Base Address Register.
3. For PCI Base Address Registers 0:5, check bit 0 for PCI Address Space.

   Bit 0 = '0' requires PCI Memory Space mapping

   Bit 0 = '1' requires PCI I/O Space mapping

   For the PCI Expansion ROM Base Address Register, check bit 0 for usage.

   Bit 0 = ‘0’: Expansion ROM not used

   Bit 0 = ‘1’: Expansion ROM used
4. For PCI I/O Space mapping, starting at bit location 2, the first bit set determines the size of the required PCI I/O Space size.

   For PCI Memory Space mapping, starting at bit location 4, the first bit set to '1' determines the size of the required PCI Memory Space size.

   For PCI Expansion ROM mapping, starting at bit location 11, the first bit set to '1' determines the required PCI Expansion ROM size.

   For example, if bit 5 of a PCI Base Address Register is detected as the first bit set to ‘1’, the PCI9030 is requesting a 32 byte space (address bits 4:0 are not part of base address decoding).
5. Determine the base address and write the base address to the PCI9030 PCI Base Address Register. For PCI Memory Space mapping the mapped address region must comply with the definition of bits 3:1 of the PCI9030 PCI Base Address Register.

After programming the PCI9030 PCI Base Address Registers, the software must enable the PCI9030 for PCI I/O and/or PCI Memory Space access in the PCI9030 PCI Command Register (Offset 0x04). To enable PCI I/O Space access to the PCI9030, set bit 0 to '1'. To enable PCI Memory Space access to the PCI9030, set bit 1 to '1'.

Offset in Config.	Description	Usage
0x10	PCI9030 LCR’s MEM	Used
0x14	PCI9030 LCR’s I/O	Used
0x18	PCI9030 Local Space 0	Used
0x1C	PCI9030 Local Space 1	Not used
0x30	Expansion ROM	Not used

Figure 4-2 : PCI9030 PLD Base Address Usage

4.2 Local Configuration Register (LCR)

After reset, the PCI9030 Local Configuration Registers are loaded from the on board serial configuration EEPROM.

The PCI base address for the PCI9030 Local Configuration Registers is PCI9030 PCI Base Address 0 (PCI Memory Space) (Offset 0x10 in the PCI9030 PCI Configuration Register Space) or PCI9030 PCI Base Address 1 (PCI I/O Space) (Offset 0x14 in the PCI9030 PCI Configuration Register Space).

Do not change hardware dependent bit settings in the PCI9030 Local Configuration Registers.

Offset from PCI Base Address	Register	Value	Description
0x00	Local Address Space 0 Range	0x0FFF_FE00	CAN Controller Address Space
0x04	Local Address Space 1 Range	0x0000_0000	
0x08	Local Address Space 2 Range	0x0000_0000	
0x0C	Local Address Space 3 Range	0x0000_0000	
0x10	Local Exp. ROM Range	0x0000_0000	
0x14	Local Re-map Register Space 0	0x0000_0001	
0x18	Local Re-map Register Space 1	0x0000_0000	
0x1C	Local Re-map Register Space 2	0x0000_0000	
0x20	Local Re-map Register Space 3	0x0000_0000	
0x24	Local Re-map Register ROM	0x0000_0000	
0x28	Local Address Space 0 Descriptor	0x1502_4120	
0x2C	Local Address Space 1 Descriptor	0x0000_0000	
0x30	Local Address Space 2 Descriptor	0x0000_0000	
0x34	Local Address Space 3 Descriptor	0x0000_0000	
0x38	Local Exp. ROM Descriptor	0x0000_0000	
0x3C	Chip Select 0 Base Address	0x0000_0081	
0x40	Chip Select 1 Base Address	0x0000_0181	
0x44	Chip Select 2 Base Address	0x0000_0000	
0x48	Chip Select 3 Base Address	0x0000_0000	
0x4C	Interrupt Control/Status	0x0041	
0x4E	EEPROM Write Protect Boundary	0x0030	
0x50	Miscellaneous Control Register	0x0078_0000	
0x54	General Purpose I/O Control	0x0224_96D0	
0x70	Hidden1 Power Management data select	0x0000_0000	
0x74	Hidden 2 Power Management data scale	0x0000_0000	

Figure 4-3 : PCI9030 Local Configuration Register

4.3 Configuration EEPROM

After power-on or PCI reset, the PCI9030 loads initial configuration register data from the on board configuration EEPROM.

The configuration EEPROM contains the following configuration data:

- Address 0x00 to 0x27 : PCI9030 PCI Configuration Register Values
- Address 0x28 to 0x87 : PCI9030 Local Configuration Register Values
- Address 0x88 to 0xFF : Reserved

See the PCI9030 manual for more information.

Address	**Offset**							
	0x00	0x02	0x04	0x06	0x08	0x0A	0x0C	0x0E
0x00	0x032A	0x1498	0x0280	0x0000	0x0280	0x0000	0x000A	0x1498
0x10	0x0000	0x0040	0x0000	0x0100	0x4801	0x0001	0x0000	0x0000
0x20	0x0000	0x0006	0x0000	0x0003	0x0FFF	0xFE00	0x0000	0x0000
0x30	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0001
0x40	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
0x50	0x1502	0x4120	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
0x60	0x0000	0x0000	0x0000	0x0081	0x0000	0x0181	0x0000	0x0000
0x70	0x0000	0x0000	0x0030	0x0041	0x0078	0x0000	0x0224	0x96D0
0x80	0x0000	0x0000	0x0000	0x0000	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0x90	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xA0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xB0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xC0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xD0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xE0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xF0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF

Figure 4-4 : Configuration EEPROM TPMC810-10

4.4 Local Software Reset

The PCI9030 Local Reset output LRESETo# is used to reset the on board local logic.

The PCI9030 local reset is active during PCI reset or if the PCI adapter software reset bit is set in the PCI9030 local configuration register CNTRL (offset 0x50).

CNTRL[30] PCI Adapter Software Reset:

Value of ‘1’ resets the PCI9030 and issues a reset to the local bus (LRESETo# asserted). The PCI9030 remains in this reset condition until the PCI host clears this bit. The contents of the PCI9030 PCI and Local Configuration Registers are not reset. The PCI9030 PCI interface is not reset.

5 Programming Hints

5.1 SJA1000 CAN Controller

The SJA1000 clock input frequency is 16 MHz (for both SJA1000 controllers).

See chapter "SJA1000 CAN Controller Registers" for an overview of all registers in the different modes. Note that some registers are available in PeliCAN Mode only and that the Control Register is available in BasicCAN Mode only. Furthermore some registers are read only or write only and some can be accessed during Reset Mode only.

A message, which should be transmitted, has to be written to the transmit buffer. After a successful reception the microprocessor may read the received message from the receive buffer and then release it for further use.

For register access, two different modes have to be distinguished:

- Reset Mode
- Operating Mode

The Reset Mode (see SJA1000 Control Register (CR; 0x0) for BasicCAN or Mode Register (MOD; 0x0) for PeliCAN, bit Reset Request) is entered automatically after a hardware-reset or when the controller enters the bus-off state (see Status Register, bit Bus Status). The operating mode is activated by resetting of the reset request bit in the control register.

More information about the registers with respect to read and/or write access, bit definition and reset values, can be found in the data sheet SJA1000 (http://www.semiconductors.philips.com).

The SJA1000 Output Control Register and Clock Divider Register have to be programmed as follows. SJA1000 controllers must be in Reset Mode:

Bit	Symbol	Description
7	OCTP1	11 : Push-Pull output stage
6	OCTN1	
5	OCPOL1	0 : Normal polarity
4	OCTP0	11 : Push-Pull output stage
3	OCTN0	
2	OCPOL0	0 : Normal polarity
1	OCMODE1	01 : Test output mode (bit reflection)
0	OCMODE0	10 : Normal output mode

Figure 5-1 : Output Control Register (OCR; 0x08)

Bit	Symbol	Description
7	CAN Mode	0 : BasicCAN Mode 1 : PeliCAN Mode
6	CBP	1 : Bypass input comparator, use RX0 only
5	RXINTEN	0 : Disable interrupts on TX1 output
4	-	0
3	clock off	1 : Disable clock output (not used)
2	CD.2	0
1	CD.1	0
0	CD.0	0

Figure 5-2 : Clock Divider Register (CDR; 0x1F)

The data to be transmitted on the CAN bus is loaded into the memory area of the SJA1000, called "Transmit Buffer". The data received from the CAN bus is stored in the memory area of the SJA1000, called "Receive Buffer". These buffers contain 2, 3 or 5 bytes for the identifier and frame information (dependent on mode and frame type) and up to 8 data bytes.

- BasicCAN Mode: The buffers are 10 bytes deep (see figure "Rx- and Tx-buffer in BasicCAN Mode").
  - 2 identifier bytes
  - up to 8 data bytes
- PeliCAN Mode: The buffers are 13 bytes deep (see figure "Rx- and Tx-buffer in PeliCAN Mode").
  - 1 byte for frame information
  - 2 or 4 identifier bytes (Standard Frame or Extended Frame)
  - up to 8 data bytes

Address	Name	Composition and Remarks
Tx-buffer: 0x0A Rx-buffer: 0x14	Identifier Byte 1	8 Identifier bits
Tx-buffer: 0x0B Rx-buffer: 0x15	Identifier Byte 2	3 Identifier bits, 1 Remote Transmission Request bit, 4 bits for the Data Length Code, indicating the amount of data bytes
Tx-buffer: 0x0C-0x13 Rx-buffer: 0x16-0x1D	Data Byte 1 - 8	Up to 8 data bytes as indicated by the Data Length Code

Figure 5-3 : Rx- and Tx-buffer in BasicCAN Mode

Address	Name	Composition and Remarks
0x10	Frame Information	1 bit indicating, if the message contains a Standard or Extended frame 1 Remote Transmission Request bit 4 bits for the Data Length Code, indicating the amount of data bytes
0x11, 0x12	Identifier Byte 1, 2	Standard Frame: 11 Identifier bits Extended Frame: 16 Identifier bits
0x13, 0x14	Identifier Byte 3, 4	Extended Frame only: 13 Identifier bits
Frame type Standard: 0x13 – 0x1A Extended: 0x15 – 0x1C	Data Byte 1 - 8	Up to 8 data bytes as indicated by the Data Length Code

Figure 5-4 : Rx- and Tx-buffer in PeliCAN Mode

The whole Receive FIFO (64 bytes) can be accessed using the CAN addresses 32 to 95.

A read access of the Tx-buffer can be done using the CAN addresses 96 to 108.

6 Configuration Hints

6.1 Transceiver Silent Mode

The CAN transceivers can be switched to Silent Mode, in this mode the transmitter is disabled. Pin S of the TJA1050 CAN transceivers is directly controlled by a GPIO output of the PCI9030, GPIO1 for channel 1 and GPIO8 for channel 2. The level on the GPIO lines can be changed by setting bit 5 (GPIO1) or bit 26 (GPIO8) in the GPIO Control Register (offset 0x54):

Value of GPIO1/8 Data	Function
0	Transceiver is in high-speed mode, which is the normal operating mode
1	Transceiver is in silent mode, transmitter is disabled

Figure 6-1 : Transceiver Silent Mode Settings

Default value after power on is ‘0’ (operating mode).

6.2 DIP Switch Settings

The following two figures show the DIP switch settings for one CAN channel. Possible line configuration options for each channel are:

- On board Line Termination: on / off
- P14 Bus Mode : connected / not connected and pass through on / off

The on board termination option for a CAN channel node input (see P14 I/O pin assignment) is a 120 ohms split termination network.

For the pass through option, the I/O lines are passed through from the node input pins to the node output pins of the P14 I/O connector (see P14 Back I/O pin assignment).

Switch-Numbers	Function	Description
1,2	Line Termination	ON: 120 R line termination enabled OFF: Line termination disabled
3,4	P14 Connection	ON: Incoming CAN bus connection enabled OFF: Incoming CAN bus connection disabled
5,6	P14 Pass Through	ON: Outgoing CAN bus connection enabled OFF: Outgoing CAN bus connection disabled

Figure 6-2 : DIP Switch Settings

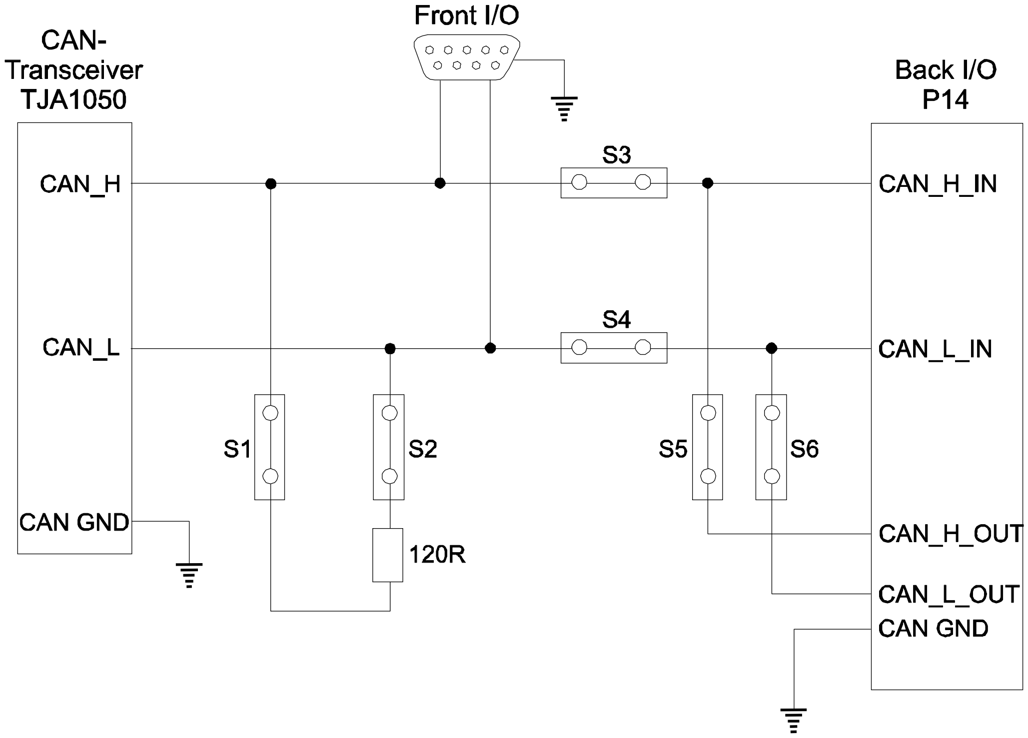

Figure 6-3 : CAN Channel Interface

7 Pin Assignment – I/O Connector

7.1 Front Panel I/O

Pin	Signal
1	N.C.
2	LOW level CAN bus signal
3	Ground channel 1
4	N.C.
5	N.C.
6	Ground channel 1
7	HIGH level CAN bus signal
8	N.C.
9	N.C.

Figure 7-1 : DB9 Male Connector X1 Channel 1

Pin	Signal
1	N.C.
2	LOW level CAN bus signal
3	Ground channel 2
4	N.C.
5	N.C.
6	Ground channel 2
7	HIGH level CAN bus signal
8	N.C.
9	N.C.

Figure 7-2 : DB9 Male Connector X2 Channel 2

7.2 Back I/O P14

Pin	Signal
1	N.C.
2	Ground channel 1
3	LOW level CAN bus signal IN channel 1
4	HIGH level CAN bus signal IN channel 1
5	Ground channel 1
6	Ground channel 1
7	LOW level CAN bus signal OUT channel 1
8	HIGH level CAN bus signal OUT channel 1
9	N.C.
10	N.C.
11	N.C.
12	N.C.
13	N.C.
14	N.C.
15	N.C.
16	Ground channel 2
17	LOW level CAN bus signal IN channel 2
18	HIGH level CAN bus signal IN channel 2
19	Ground channel 2
20	Ground channel 2
21	LOW level CAN bus signal OUT channel 2
22	HIGH level CAN bus signal OUT channel 2
23	Ground channel 2
24 ... 64	N.C.

Figure 7-3 : Pin Assignment P14 Back I/O Connector