Technical Information Manual

Revision n. 2
9 April 2002

MOD. A 128 HS

SY 127
H.S. CAENET
COMMUNICATION
CONTROLLER

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CAEN declines all responsibility for damages or injuries caused by an improper use of the Modules due to negligence on behalf of the User. It is strongly recommended to read thoroughly the CAEN User's Manual before any kind of operation.

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CAEN reserves the right to change partially or entirely the contents of this Manual at any time and without giving any notice

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1. DESCRIPTION

1.1. FUNCTIONAL DESCRIPTION

The CAEN Model A128HS is a COMMUNICATION CONTROLLER for the SY127 High Voltage System. The unit can replace the old A128 Communication Controller that uses the H. V. CAENET in any SY127 Crate, thus allowing to use H. S. CAENET to control an SY127 System and maintain compatibility with newer High Voltage Systems.

Each module houses a HIGH SPEED (H. S.) CAENET node for the remote control; it allows to link one or more SY127 or SY527 Systems to a H. S. CAENET controller which acts as a System control unit.

Available controllers are

- A303A, H. S. CAENET PC Controller;
- C117B, H. S. CAENET CAMAC Controller;
- V288, H. S. CAENET VME Controller.

Moreover, the Model A128HS allows to configure the SY127 System as a H. S. CAENET Controller itself: in this way it allows the control of a multicrate system from a single video terminal plugged in one of the crates. The communication software needed for the operation of multicrate system is built in every unit.

N.B.: This User's Manual describes the operations that can be performed to control the SY127 System via H. S. CAENET: for the SY127 complete description please refer to the SY127 User's Manual.

2. SPECIFICATIONS

2.1. EXTERNAL COMPONENTS

(refer to Fig. 2.1)

CONNECTORS

- N. 2, "HIGH SPEED CAENET IN/OUT", LEMO 00 type, high impedance. Connectors for the HIGH SPEED CAENET operations.

- N. 1, "RS 232C", 25 pin D-type female connector.

DISPLAYS

- N. 1, "CRATE N.", 2-Digit red LED, to indicate the H. S. CAENET node number.

- N. 1, "TERM 50 Ω", red LED, indicates when lit the insertion of a 50 Ω termination on the H.S. CAENET connector.

- N. 1, red LED, to indicate the activity of the H. S. CAENET node.

SWITCHES

- N. 1, "TERM 50 Ω", 2-position lever switch, allows to insert a 50 Ω termination on the H.S. CAENET connector.

2.2. INTERNAL COMPONENTS

(refer to Fig. 2.2)

SWITCHES

- N. 8, "CR NUM SW2", 2-position DIP switches, allow to select the A128HS Crate Number.

- N. 8, "RS232 SW3", 2-position DIP switches, allow to select the RS232 Configuration of the A128HS Communication Controller.

- N. 2, "PASS. SW4", 2-position DIP switches, allow to disable the Password protection on the SY127 System.

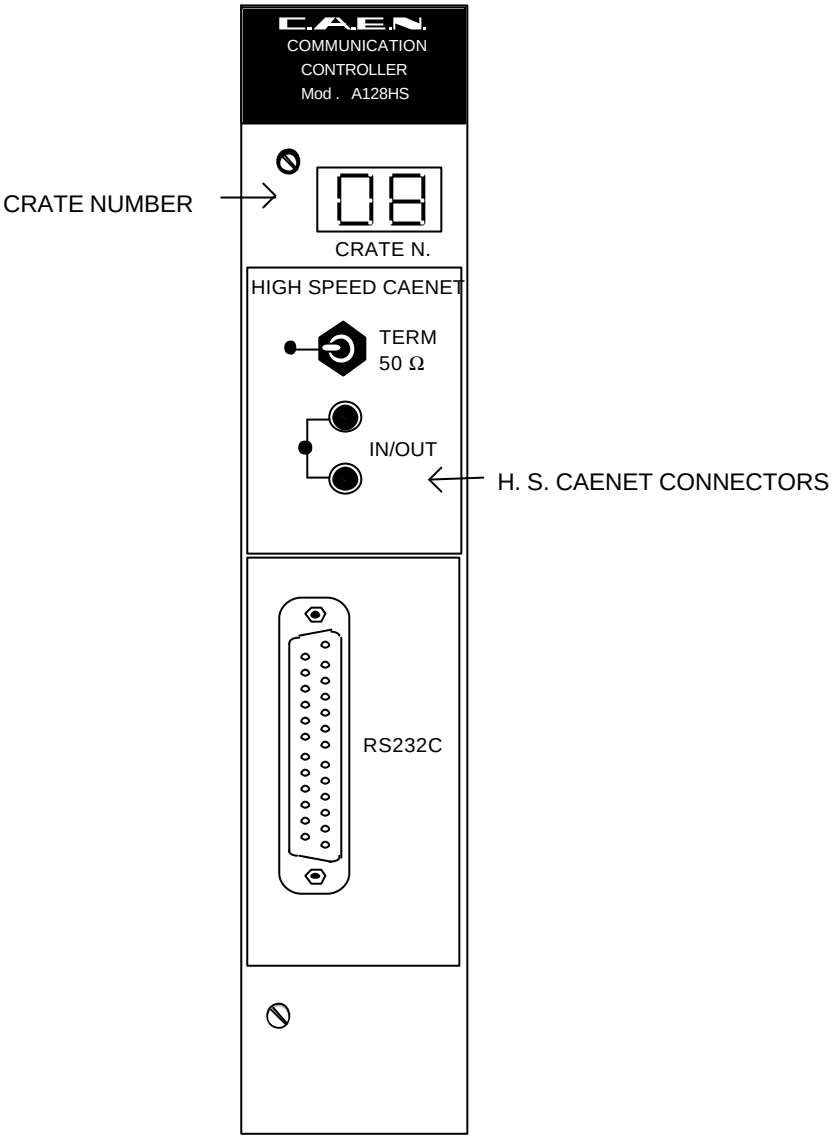

Fig. 2.1: Mod. A128HS Front Panel

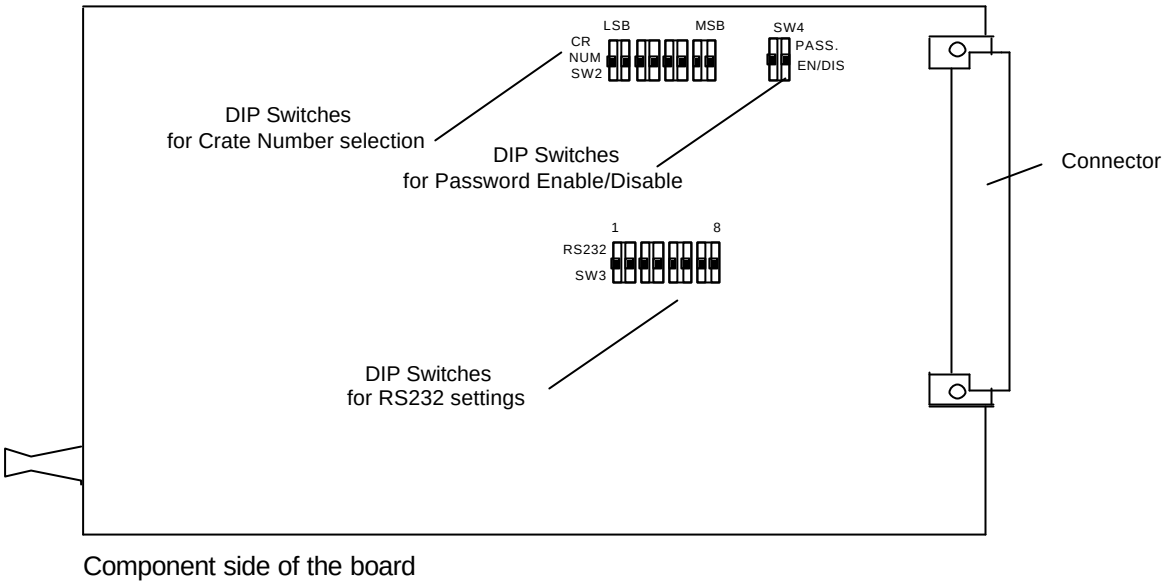

Fig. 2.2: Mod. A128HS Components Locations

3. OPERATING MODES

3.1. GENERAL INFORMATION

The Model A128HS is a Communication Controller for the SY127 High Voltage System, designed to allow the use of HIGH SPEED CAENET to control the SY127 System.

3.2. MANUAL SETTINGS

3.2.1. FRONT PANEL SETTINGS

A two-position lever switch allows the insertion of a 50 Ω termination on the H. S. CAENET connector. This must be done both on the first and on the last System in a chain, to avoid line reflections.

3.2.2. CRATE NUMBER SETTING

A group of 8 internal two-position DIP switches (SW2 on Fig. 2.2) allows to set the Crate Number (H.S. CAENET address code, see §3.3) of the A128HS Controller. This number is used as an address during inter-crate communication and is BCD coded via the SW2 switches. It may range from 0 to 99. In a multicrate configuration, a different crate number must be assigned to each crate. For appropriate settings, refer to Fig. 3.1 here below.

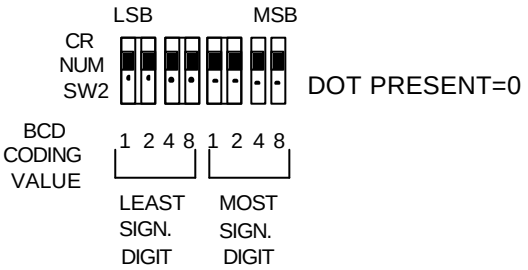

Fig. 3.1: Mod. A128HS Crate Number Setting

3.2.3. RS232 CONFIGURATION

A group of 8 two-position DIP switches (SW3 on Fig. 2.2) allows to set the RS232 configuration of the A128HS Controller. Switches 1 to 4 control the Baud Rate, bits 5 to 8 control the protocol parameters. For appropriate settings, refer to Fig. 3.2 and Tables 3.1, 3.2 here below.

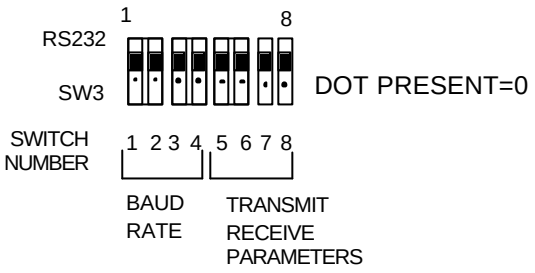

Fig. 3.2: Mod. A128HS RS232 Settings

Table 3.1: Mod. A128HS Baud Rate Settings

Switch N. 4 3 2 1	**Baud Rate**
0 0 0 0	50
0 0 0 1	75
0 0 1 0	110
0 0 1 1	134.5
0 1 0 0	150
0 1 0 1	300
0 1 1 0	600
0 1 1 1	1200
1 0 0 0	1800
1 0 0 1	2000
1 0 1 0	2400
1 0 1 1	3600
1 1 0 0	4800
1 1 0 1	7200
1 1 1 0	9600
1 1 1 1	NOT VALID

Table 3.2: Mod. A128HS Transmit/Receive Settings

SWITCH N. 5 =0	Parity Disabled
SWITCH N. 5 =1	Parity Enabled
SWITCH N. 6 =0	Odd Parity
SWITCH N. 6 =1	Even Parity
SWITCH N. 7 =0	7 Bit Character
SWITCH N. 7 =1	8 Bit Character
SWITCH N. 8 =0	1 Stop Bit
SWITCH N. 8 =1	2 Stop Bits

3.2.4. PASSWORD ENABLE/DISABLE

A password may be set via software in order to protect the System from improper use (see §3.3.8 of SY127 User's Manual). The use of this password may however be qualified or disqualified via hardware through the SW4 located on the A128HS Controller (see Fig. 2.2). For appropriate settings, refer to Fig. 3.3 here below.

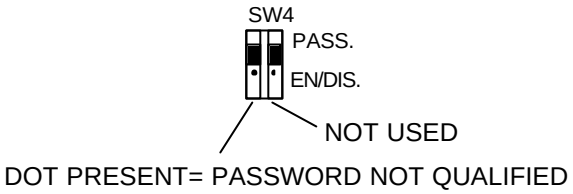

Fig. 3.3: Mod. A128HS Password Enable Setting

3.3. H. S. CAENET

The H. S. CAENET Network is a send and receive half duplex system; It enables the asynchronous serial transmission (1 MBaud rate) of data packets along a simple 50 Ω coaxial cable. Several devices (H. S. CAENET nodes) are able to share the same media to transmit and receive data. Each node is able to receive the serial data packet and store it automatically in a FIFO (RX FIFO) and transmit the data contained in another FIFO (TX FIFO). Both FIFOs are 512 byte deep.

Usually transfers between H. S. CAENET nodes take place according to the typical Master/Slaves communication:

- There is a single Master : H. S. CAENET controller

- The Slaves are daisy chained on the network, and are identified by an address code (from 1 to 99);

- the H. S. CAENET Master initiates the transmission, all the Slaves receive the data, and only the Slave addressed then accesses the serial line to transmit the data requested by the Master.

- The maximum data packet length is 512 bytes.

The address of the H. S. CAENET node of the A128HS (Station #) is selectable from 1 to 99. In this way up to 99 modules may be controlled from a single point via one of the following CAEN H. S. CAENET Controllers:

- A303A H. S. CAENET PC Controller;
- C117B H. S. CAENET CAMAC Controller;
- V288 H. S. CAENET VME Controller.

4. H. S. CAENET OPERATION

The Model SY127 is provided with a H. S. CAENET node through which it can be controlled by the following H. S. CAENET Controllers:

Mod. C117B - H. S. CAENET CAMAC Controller;
Mod. V288 - H. S. CAENET VME Controller;
Mod. A303A - H. S. CAENET PC Controller.

NOTE: the Address Number of the SY127 (Crate #) must be the only one in the line in which you wish to insert the module. It can be any number between 1 and 99. Due to high transmission speed of the data in line it is necessary to terminate this line on a 50 W impedance at the end to avoid reflections.

Via H. S. CAENET it is possible to modify all the channel parameters regardless of its Password Protection Status (enabled/disabled) selected via Terminal (see § 5.2 and 5.4). In particular it is possible to modify the status of its Password Parameter.

4.1. USING THE H. S. CAENET VME CONTROLLER

The Mod. SY127 can be controlled remotely via VME through the Mod. V 288 H. S. CAENET VME Controller.

The Model V288 has been designed to control a H. S. CAENET node through the VME bus. It is composed of a collection of registers, for the operation control, and two memory buffers for the transmitted and received data packets, arranged in a FIFO logic 16 bit wide 256 word deep.

In the memory buffer for the received data are also stored some error messages generated by the V288 itself when the H. S. CAENET operation has failed (see Table 4.15).

Standard VME cycles allow the User to perform the required control and setting operations on each Mod. SY127 in the network, according to the typical MASTER/SLAVE communication protocol, where the VME controller assumes the MASTER function.

The module operations can be software controlled in polling mode or can be handled via interrupt facility. It houses a VME ROAK INTERRUPTER that generates a VME interrupt (if enabled) as soon as the data packet (or the error message) is stored in the receive buffer.

The Mod. V288 registers are described in Table 4.1

Table 4.1: Mod. V288 Registers

NAME	TYPE	ADDRESS	FUNCTION
Transmit Data Buffer	Write only	Base Address + 00	Transmit data storage
Receive Data Buffer	Read only	Base Address + 00	Receive data storage
Status Register	Read only	Base Address + 02	After a H. S. CAENET operation has been performed, this register indicates whether the operation is valid or not; FFFE= valid operation FFFF= no valid operation
Transmission Register	Write only	Base Address + 04	By writing into this register the Transmit Data buffer content is transmitted on the cable
Reset Register	Write only	Base Address + 06	Module's Reset
Interrupt Vector Register	Write only	Base Address + 08	Interrupt vector programming register

4.1.1. TRANSMIT DATA BUFFER

(Base Address + 0, write access)

This is the buffer which is loaded with the data packet to transmit. It is arranged in a FIFO logic 16 bit wide (the transmitted data packet is composed of 16 bit words as shown in Tab. 4.2).

4.1.2. RECEIVE DATA BUFFER

(Base Address + 0, read access)

This is the buffer where the Mod.V288 automatically stores the data packet received from the SY127 or, if the H. S. CAENET operation has failed, stores an error code. It is arranged in a FIFO logic 16 bit wide (the data packet received is composed of 16 bit words as shown in Tab. 4.3).

4.1.3. STATUS REGISTER

(Base Address + 2, read only)

The content of this register indicates if the previous H. S. CAENET operation is valid or not.

Status Register = %FFFF $\Rightarrow$ No valid operation;
Status Register = %FFFE $\Rightarrow$ Valid operation.

After one of the following operations the User is recommended to read the Status Register:

- **write data in the Transmit Data buffer**: it indicates if the datum written has been stored or not in the Transmit Data Buffer; a "No valid operation" means that the Transmit Data Buffer is not available for data storage. This may happen in these cases:

- if the H. S. CAENET node is active (it is transmitting a previous data packet or it is receiving the Slave response data packet);
- if the Transmit Data Buffer is full (the max. number of stored data is 256);

- **write in the Transmission Register** (Start data packet transmission): it indicates if the Start Transmission command has been recognized by the Mod. V288; a "No valid operation" means that the H. S. CAENET node is not able to transmit data. This may happen if the H. S. CAENET node is active (it is transmitting a previous data packet or it is receiving the Slave response);

- **read data from the Receive Data Buffer:** it indicates if the data read is valid or not.

4.1.4. TRANSMISSION REGISTER

(Base Address + 4, write only)

By writing at this location the H. S. CAENET node enters in the transmit mode: the data stored in the Transmit Data Buffer are transmitted on the cable. If this operation is performed with the Transmit Data Buffer empty, an error message is stored in the Receive Data Buffer (error %FFFD, see Table 4.15).

4.1.5. RESET REGISTER

(Base address + 6, write only)

A write access to this location causes the V288 to enter in restart mode; this causes the following operations:

- the buffers are cleared;
- every pending interrupt is cleared;
- every data transfer is aborted;
- the V288 does not accept any command.

It remains in this status for about 3 msec. The module can be reset also by pressing the Front Panel Push button.

4.1.6. INTERRUPT VECTOR REGISTER

(Base address + 8, write only)

The value written in this 8 bit register is the STATUS/ID that the V288 INTERRUPTER places on the VME data bus during the Interrupt Acknowledge Cycle.

4.1.7. V288 ADDRESSING CAPABILITY

The module works in A24 mode; this implies that the module address must be specified in a field of 24 bits.

The Address Modifiers used by the module are:

AM	= %39 :	Standard User data access
AM	= %3A :	Standard User program access
AM	= %3D :	Standard supervisor data access
AM	= %3E :	Standard supervisor program access

The module's Base Address is fixed by dip switches located on the board (see *V288 Technical Information Manual Fig. 4.1)*

4.1.8. V288 DATA TRANSFER AND INTERRUPTER CAPABILITY

The registers and the buffers are accessible in D16 mode.

The V288 module houses a VME ROAK INTERRUPTER D08(o) type. This implies the following:

- it responds to 8 bit, 16 bit and 32 bit interrupt acknowledge cycles providing an 8-bit STATUS/ID on the VME data lines D00..D07.

- it removes its interrupt request when the VME MASTER reads the V288 STATUS/ID during the Interrupt Acknowledge Cycle (ROAK: Release On Acknowledge).

4.1.9. V288 INTERRUPT LEVEL

The interrupt level corresponds to the value set on the two dip-switches SW4, SW3 as described in the *V288 Technical Information Manual .*

4.1.10. MASTER-TO-SLAVE DATA COMPOSITION (V288 CASE)

The Master-to-Slave data have to be written in the Transmit Data Buffer, by performing subsequent write accesses as follows.

Table 4.2: Master-to-Slave Data Composition

Order	Operation	Address	Datum (HEX)	Meaning
1	Write	Base Ad. + 0	%0001	H. S. CAENET Controller identified code
2	Write	Base Ad + 0	%00XX	Crate Number
3	Write	Base Ad + 0	Code	First word of the operation Code(*) to be performed
4 to 256	Write	Base Ad + 0	Code/Set	Eventual subsequent words of the Code or Set values

(*) The operation Codes may be some words in length and eventually followed by several set values. In the SY127 case the Code may be one or two words in length.

As soon as the data packet has been stored in the Transmit Data Buffer, it can be transmitted on the cable by performing a Write operation on the Transmission Register. The operation codes are shown in Tab. 4.8.

After any transmission, in the V288 Receive Data Buffer the User reads the Slave response or a V288 error message (for example if the V288 does not receive any Slave response within a period of 500 msec it stores the code %FFFF in the Receive Data Buffer, see Table 4.15).

4.1.11. SLAVE-TO-MASTER DATA COMPOSITION (V288 CASE)

The answer data coming from the Mod. SY127 or a Mod. V288 error message is automatically stored into the V288 Receive Data buffer and therefore is available to the User. As soon as the data pack is stored in this buffer, a VME interrupt (if enabled) is generated.

The following Table shows the structure of the SY127 data packet:

Table 4.3: Slave-to-Master Data Composition

Order	Operation	Address	Datum	Meaning
1	Read	Base Ad + 0	Error Code	Error code
2 to 255(*)	Read	Base Ad + 0	value	Eventual Parameter value

(*) The first data of the packet is read and checked by the V288 Control Logic (see *V288 Tecnical Information Manual)*.

The Error Codes are described in Tab. 4.14.

4.1.12. V288 - SY127 COMMUNICATION SEQUENCE

- write the data packet in the Transmit Data Buffer; in the packet is contained the H. S. CAENET address of the SY127 (Crate #) (see Tab. 4.2 for the data structure).
For each data:

- write the data in the Transmit Data Buffer;
- read the Status Register;
- if Status Register =%FFFE
  {
  the data is stored in the buffer
  }
- else
  {
  error
  }

- Transmit the data packet:

- Access in write the Transmission Register;
- read the Status Register;
- if Status Register = %FFFE
  {
  the V288 H. S. CAENET Node enters in the transmit mode and the data packet stored is transmitted on the cable
  }
- else
  {
  error
  }

- Wait for the SY127 response

- if the Interrupt is enabled
  {
  wait for V288 interrupt
  }
- else
  {
  - read the Receive data buffer;
  - read the Status Register;
  - if Status Register = %FFFF discard the data and repeat the two read operations;
  - if Status Register = %FFFE accept the data read: it may be the first data of the SY127 response data packet or a V288 error message; go to the Read Response section;
  }

- Read response

- read the Receive data buffer;
- read the Status Register;
- if Status Register = %FFFE accept the data read and repeat the two read operation;
- if Status Register = %FFFF discard the data read and exit: the Receive Data Buffer is empty.

4.2. USING THE H. S. CAENET CAMAC CONTROLLER

The Mod. SY127 can be controlled remotely via CAMAC through the Mod. C 117B, H. S. CAENET CAMAC Controller.

The Model C 117B has been designed to control a H. S. CAENET node through the CAMAC bus. It houses two memory buffers for the transmitted and received data packets, arranged in a FIFO logic 16 bit wide 256 word deep.

In the memory buffer for the received data are also stored some error messages generated by the C117B itself when the H. S. CAENET operation has failed (see Table 4.15).

The standard CAMAC functions listed in Table 4.4 allow the User to perform the required control and setting operations on each Mod. SY127 in the network according to the typical MASTER/SLAVE communication protocol, where the CAMAC controller assumes the MASTER function.

As soon as the data packet (or the error message) is stored in the receive buffer, a LAM signal is generated (if enabled).

X response is generated for all valid function.
Q response is generated for each valid function unless is otherwise specified (see Table below).

Table 4.4: Mod. C 117 B CAMAC Functions

F(0) N	Reads the data stored in the Mod. C117B Receive Data buffer. Q response while the buffer contains data.
F(8) N	Tests the LAM line. Q response if LAM is true.
F(9) N	Resets the module (clears buffer and LAM; disables the LAM line).
F(16) N	Stores the data into the Mod. C117B Transmit Data buffer. Q response until the buffer is full (256 16-bit words).
F(17) N	Transfers data to the serial line.
F(24) N	Disables the LAM line.
F(26) N	Enables the LAM line.
C, Z	Same as F(9) N.

4.2.1. TRANSMIT DATA BUFFER [F(16) N FUNCTION]

This is the buffer which is loaded with the data packet to transmit; it is arranged in a FIFO logic 16 bit wide (the transmitted data packet is composed of 16 bit words as shown in Tab. 4.5). The data are stored in this buffer by performing one or more F(16) N Functions with the data to be written asserted on the WRITE lines W<1..16>.

The Q response to the F(16) N Function indicates if the datum has been stored or not in the Transmit Data Buffer;

- Q=1 means that the data has been stored in the Transmit Data Buffer;
- Q=0 means that the Transmit Data Buffer is not available for data storage. This may happen in these cases:
    - if the H. S. CAENET node is active (it is transmitting a previous data packet or it is receiving the Slave response data packet);
    - if the Transmit Data Buffer is full (the maximum number of data stored is 256)

4.2.2. RECEIVE DATA BUFFER [F(0) N FUNCTION]

This is the buffer where the Mod. C117B automatically stores the data packet received from the SY127 or, if the H. S. CAENET operation has failed, stores an error code. It is arranged in a FIFO logic 16 bit wide (the received data packet is composed of 16 bit words as shown in Tab. 4.6). The data contained in the Receive Data buffer are read by performing F(0) N Functions. The required data are present on the READ lines R<1..16>.

The Q response indicates if if the data read is valid or not:

- Q=1 $\Rightarrow$ valid data;
- Q=0 $\Rightarrow$ no valid data.

4.2.3. START TRANSMISSION [F(17) N FUNCTION]

By performing an F(17) N Function the H. S. CAENET node enters in the transmit mode: the data stored in the Transmit Data Buffer are transmitted on the cable. If this operation is performed with the Transmit Data Buffer empty, an error message is stored in the Receive Data Buffer (error %FFFD see Table 4.15).

The Q response indicates if the Start Transmission command has been recognized or not by the Mod. C117B;

- Q=1 $\Rightarrow$ the Transmit command has been successfully recognized and that a valid response can be read in the Receive Data Buffer within a period of 500 msec.(the C117 waits up to 500 msec for a Slave response, after this it stores in the Receive Data Buffer the error code %FFFF, see Table 4.15)

- Q=0 $\Rightarrow$ the H.S CAENET node is not able to transmit data. This may happen if the H. S. CAENET node is active (it is transmitting a previous data packet or it is receiving the Slave response).

4.2.4. C117B RESET

The C117 B can be resetted in the following ways:

- by performing an F(9) N Function;
- by performing a C Command;
- by performing a Z Command;
- by pushing the Front Panel push button.

After one of these operations the C117B enters in restart mode; this causes the following:

- the buffers are cleared;
- the LAM is cleared;
- the LAM is disabled;
- every data transfer is aborted;
- the C117B does not accept commands.

It remains in this status for about 3 msec.

4.2.5. MASTER-TO-SLAVE DATA COMPOSITION (C117B CASE)

The MASTER-to-SLAVE data have to be written into the Transmit Data buffer by performing subsequent F(16) N functions as follows:

Table 4.5: Master-to-Slave Data Composition

Order	CAMAC Function	W16 to W1 (HEX)	Meaning
1	F(16) N	%0001	H. S. CAENET Controller identified code
2	F(16) N	%00XX	Crate Number
3	F(16) N	Code	First word of the operation Code(*) to be performed
4 to 256	F(16) N	Code/Set	Eventual subsequent words of the Code or Set values

(*) The operation Codes may be some words in length and eventually followed by several set values. In the SY127 case the Code may be one or two words in length.

After the required F(16) N functions have been performed, it is necessary to carry out an F(17) N function in order to transfer the stored data to the addressed module. The operation codes are shown in Tab. 4.8.

As soon as the response data packet is stored into the C117B Receive Data Buffer a LAM signal is generated (if enabled). The LAM is cleared whenever the last datum has been read.

If the LAM has not been enabled after the F(17) N function the F(0) N function must be repeated until a Q=1 response is obtained. The readout is over when Q=0 (Q STOP readout operation).

In the C117 B Receive Data Buffer the User reads the SY127 response or a C117 B error message (for example if the C117 B does not receive any Slave response within a period of 500 msec it stores the code %FFFF in the Buffer, see Tab. 4.15).

4.2.6. SLAVE-TO-MASTER DATA COMPOSITION (C117B CASE)

The answer data coming from the Mod. SY127 or a Mod. C 117 B error message is automatically stored into the C117 B Data buffer and therefore is available to the User. As soon as the data pack is stored in this buffer, a LAM (if enabled) is generated.
The following Table shows the structure of the SY127 data packet:

Table 4.6: Slave-to-Master Data Composition

Order	CAMAC Function	Datum	Meaning
1	F(0) N	Error Code	Error code
2 to 255(*)	F(0) N	value	Eventual Parameter value

(*) The first data of the packet is read and checked by the C117B Control Logic (see *C117B Technical Information Manual)*.

The Error codes are described in Tab. 4.14.

4.2.7. C117B - SY127 COMMUNICATION SEQUENCE

- write the data packet in the Transmit Data Buffer; in the packet is contained the H. S. CAENET address of the SY127 (Crate #) (see Tab. 4.5 for the data structure).

For each data:

- perform an F(16) N Function;
- if Q=1
  {
  the data is stored in the buffer
  }
- else
  {
  error
  }

- Transmit the data packet:

- perform an F(17) N Function;
- if Q=1
  {
  the C117B H. S. CAENET Node enters in the transmit mode and the data packet stored is transmitted on the cable
  }
- else
  {
  error
  }

- Wait for the SY127 response

- if LAM is enabled
  {
  wait for C117B LAM: when LAM is asserted go to the Read response section
  }
- else
  {
  - perform an F(0) N Function;
  - if Q=0 discard the data and repeat the operation;
  - if Q=1 accept the data read: it may be the first data of the SY127 response data packet or a C117B error message; go to the Read Response section
  }

- Read response

- perform an F(0) N Function;
- if Q=1 accept the data read and repeat the operation;
- if Q=0 discard the data read and exit: the Receive Data Buffer is empty.

4.3. MASTER-TO-SLAVE DATA PACKET DESCRIPTION

The MASTER-to-SLAVE data packet described in the § 4.1.1 and 4.2.5 has the following structure:

Table 4.7: Master-to-Slave Data Composition

Order	Datum (Hex)	Meaning
1	%0001	H. S. CAENET Controller identified code
2	%00XX	Crate Number
3	Code	First word of the operation Code to be performed
4 to 256	Code/Set	Eventual subsequent words of the Code or set values

In the following Table are shown the various Data packets available.

Table 4.8: Data Packets

word 3	word 4	Meaning
%0	==	Mainframe identifier
%3	==	Read Boards characteristics
%4	==	Read Protection Bits characteristics
%5	==	Read Streamer Tubes Conditioning (STC) Parameters
%30	==	Format CPU EEPROM
%31	==	Confirm Format CPU EEPROM
%32	==	Clear Alarm
%39	Protection Word	Set Protection Bits
%40	==	Read Channel to Group Assignment Bits
%n01	==	Read Channel n parameters values
%n10	V0set value	Set Channel n V0set value
%n11	V1set value	Set Channel n V1set value
%n12	I0set value	Set Channel n I0set value
%n13	I1set value	Set Channel n I1set value
%n15	Rup value	Set Channel n Ramp-up value (Rup)
%n16	Rdwn value	Set Channel n Ramp-down value (Rdwn)
%n17	Trip value	Set Channel n Trip value
%n18	On/Off value	Set Channel n On/Off
%n19	Channel Name	Set Channel n name
%n50	Group Ass. Word	Channel to Group Assignment
%g41	==	Read Vmon, Imon, Status, STC phase, STC time of Channels in a Group
%g42	==	Read V0set, V1set, I0set, I1set of Channels in a Group
%g43	==	Read Ramp-up, Ramp-down, Trip of Channels in a Group
%g52	V0set value	Set Group g V0set absolute value
%g53	V1set value	Set Group g V1set absolute value
%g54	I0set value	Set Group g I0set absolute value
%g55	I1set value	Set Group g I1set absolute value
%g57	Rup value	Set Group g Ramp-up absolute value (Rup)
%g58	Rdwn value	Set Group g Ramp-down absolute value (Rdwn)
%g59	Trip value	Set Group g Trip absolute value
%g5A	On/Off value	Set Group g On/Off
%g60	V0set value	Set Group g V0set relative value
%g61	V1set value	Set Group g V1set relative value
%g62	I0set value	Set Group g I0set relative value
%g63	I1set value	Set Group g I1set relative value
%g65	Rup value	Set Group g Ramp-up relative value (Rup)
%g66	Rdwn value	Set Group g Ramp-down relative value (Rdwn)
%g67	Trip value	Set Group g Trip relative value

- n = Channel's physical number on the Board (n = %00..%27, corresponding to channels 0 to 39).

- g = Group number (n = %0..%7, corresponding to groups 0 to 7)

4.3.1. PARAMETERS SETTING

The following parameters (V0set, V1set, I0set, I1set, Ramp-Up, Ramp-Down, Trip) can be set in three different ways:

a) on a single channel basis (codes %n10 to %n17);

b) on a group basis in "absolute" value (codes %g52 to %g59);

c) on a group basis in "relative" value (codes %g60 to %g67).

The word containing the set value (word 4, see Table 4.8) has the following structure:

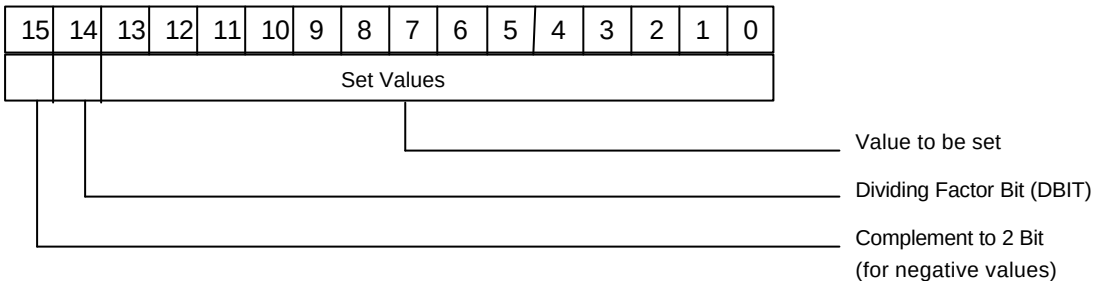

Fig. 4.1: Set Values Word 4 Structure

Bit 14 of the data field (DBIT) has a specific meaning (note that no H.V. value can be high enough to affect this bit): bit 14 ON means that the H.V. value has to be divided by 10 (i.e a value is set in tenths of a Volt or in hundredths of a Volt instead of Volts.)

Bit 15 is the sign bit: when set to 1, the Set Value bits (0 to 13), representing the H.V. value, are coded in a binary two-complement.

Caution: bit 14 is not affected by the value of bit 15, i.e. it is never complemented to 2.

The set values are also different if a relative set operation is performed: the value to be written in the Set Value word has to be coded in binary complement to two, thus involving the bit 15 in the coding.

The relative value set is a signed offset value that can be added algebraically to the absolute value set.

The set values for the different parameters must be expressed as explained by the following examples.

HV and RAMP setting

a) The following HV modules feature a 1/10 Volt resolution:

200 V - 200 µA
800 V - 500 µA

For these modules, the voltage unit implied depends on the performed set operation (Single Channel or Group) as well as on the setting of bit 14, according to the following:

a.1) Single Channel Operation

bit 14 OFF unit = 1/10 Volt

e.g.	SET VALUE. = 32	==>	V0 = 3.2 Volts
	V0 = 3.2 Volts	==>	MON VALUE. = 32

bit 14 ON unit = 1/100 Volt

(the H.V. set value is rounded to the highest 1/10 V value below,

e.g.	SET VALUE= 64	==>	V0 = 0.6 Volts
	V0 = 0.6 Volts	==>	MON VALUE. = 6

a.2) Group (Absolute or Relative) Operation

bit 14 OFF unit = 1 Volt

(e.g.	SET VALUE = 17	==>	V0 = 17 Volts
	V0 = 17 Volts	==>	MON VALUE = 170)

bit 14 ON unit = 1/10 Volt

(e.g.	SET VALUE= 17	==>	V0 = 1.7 Volts
	V0 = 1.7 Volts	==>	MON VALUE = 17)

b) The following HV modules feature a 1/2 Volt resolution:

2 KV - 200 µA
2 KV - 3 mA

For these modules, the Monitoring always reports a value in half-volts, i.e. the actual voltage in Volts is the number encoded in the MON VALUE divided by 2.

The conversion table is the following:

b.1) Single Channel Operation

bit 14 OFF unit = 1/2 Volt

e.g.	SET VALUE= 16	==>	V0 = 8 Volts
	V0 = 8 Volts	==>	MON VALUE = 16

bit 14 ON unit = 1/20 Volt

the H.V. value set is rounded to the highest 1/2 V value below,

e.g.	SET VALUE= 22	==>	V0 = 1.0 Volts
	V0 = 1.0 Volts	==>	MON VALUE = 2
	SET VALUE= 17	==>	V0 = 0.5 Volts
	V0 = 0.5 Volts	==>	MON VALUE = 1

b.2) Group (Absolute or Relative) Operation

bit 14 OFF unit = 1 Volt

(e.g.	SET VALUE= 100	==>	V0 = 100 Volts
	V0 = 100 Volts	==>	MON VALUE = 200)

bit 14 ON unit = 1/10 Volt

(the H.V. value set is rounded to the highest 1/2 V value below,

e.g.	W.L = 32	==>	V0 = 3.0 Volts
	V0 = 3.0 Volts	==>	MON VALUE = 6
	SET VALUE= 37	==>	V0 = 3.5 Volts
	V0 = 3.5 Volts	==>	MON VALUE = 7)

Note: when selected in an Absolute Group, the Voltage resolution of the 2 KV-200µA modules depends on the H.V. value itself, namely:

for	0 V	< H.V. <	1639.0	V	resolution = 1/2 Volt
for	1638 V	< H.V. <	2000.0	V	resolution = 1 Volt

In the range 1638 - 2000 Volts, a 1/2 Volt resolution can still be obtained if a Relative Group operation is performed.

c) The following HV modules feature a one-Volt resolution:

8 KV - 200 µA	**8 KV - 500µA**
6 KV - 200 µA	**6 KV - 1 mA**
4 KV - 200 µA	**3/4 KV 2/3 mA**

For these modules, the monitored value is always to be interpreted as Volts.

For these modules, the voltage unit implied does not depend on the performed set operation (Single Channel or Group) , but there is only a dependence on the setting of bit 14, according to the following table:

bit 14 OFF unit = 1 Volt

(e.g.	SET VALUE= 50	==>	V0 = 50 Volts
	V0 = 50 Volts	==>	MON VALUE = 50)

bit 14 ON unit = 1/10 Volt

(the H.V. value set is rounded to the highest integer value below,

e.g.	SET VALUE= 105	==>	V0 = 10 Volts
	V0 = 1- Volts	==>	MON VALUE = 10)

SETTING of the currents

The HV modules with a 1/10 of a µA current resolution follow the same rules as stated for the modules with a 1/10 voltage resolution and those with 1 µA follow the rules for 1 Volt.

SETTING of the Trip value

The trip value is the same for all boards and can be set between 0 and 9999. If a Group relative operation is performed and if the User wants to decrease the trip value, a two-complement value must be written with a %g67 operation.

4.3.2. CHANNEL NAME SETTING

(Code %n19)

To be implemented.

4.3.3. PROTECTION SETTINGS

(Code %39)

Three bits allow to set the following:

a) Power ON status (On/Off), i.e. when set, at Power ON switches automatically ON channels that were previously ON before Power-OFF.

b) Password enable; allows to enable/disable the password protection (1= enabled, 0=disabled);

c) Keyboard enable, allows to enable/disable the front panel keyboard (1= enabled, 0=disabled).

These bits are the first three in the Protection word, and are the only bits that can be accessed in write mode. The structure of the Protection Word in read mode is described in § 4.4.4.

4.3.4. CHANNEL TO GROUP ASSIGNMENT
(Code %n50)

This command allows to assign a Channel to one of 7 groups. By writing a "1" in the appropriate bit, a channel is assigned to a chosen group. As a matter of fact, every channel belongs to group ALL, so only bits 1 to 7 of the Group Assignment Word can be modified, while bit 0 is always set to 1.

The structure of the Group Assignment Word is the following:

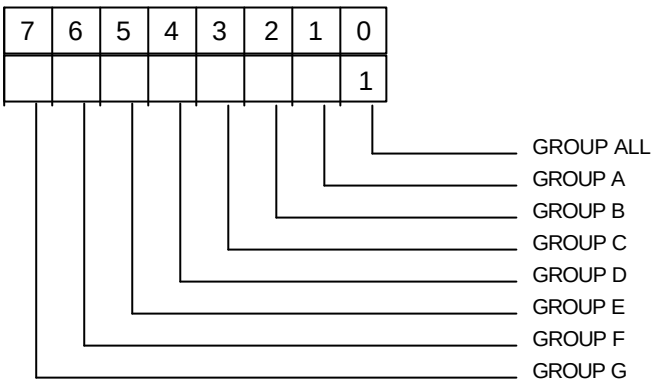

Fig. 4.2: Channel To Group Assignment Word Structure

4.3.5. SYSTEM OPERATIONS

Codes %30, %31 (Format CPU E^2PROM)

The CAENET operating codes %30, %31 allow to format the CPU EEPROM. In order to do this a CAENET command %30 must be performed, followed by a %31 command to confirm the operation. If only a %31 is performed, the response is an error code %FF01.

Code %32 (Clear Alarm)

The CAENET operating code %32 clears the Alarms occurred in the System.

4.4. SLAVE-TO-MASTER DATA PACKET DESCRIPTION

The answer data coming from the Mod. SY127 or from the H. S. CAENET Controller has the following structure.

Table 4.12: Slave-to-Master Data Composition

Order	Datum (HEX)	Meaning
1	Error Code	Error code
2 to 256	value	Eventual Parameter value

4.4.1. ERROR CODES DESCRIPTION

The Error codes are described in the following Table.

Table 4.13: Error Codes

Datum (Hex)	Meaning
%0	Successful operation.
%FF00	Module Busy; it has tried to effect an operation while the module is performing a previous operation.
%FF01	Code not recognized or message incorrect.
%FF02	Value out of range.
%FF03	Channel or Board not present.
%FFFD	No data to be transmitted; it has tried to start a transmission with the Transmit data Buffer empty (H. S. CAENET Controller error message).
%FFFE	The H. S. CAENET Controller identifier is incorrect (H. S. CAENET Controller error message).
%FFFF	The addressed module does not exist. This message are generated after a period of 500 msec (H. S. CAENET Controller error message).

4.4.2. MAINFRAME IDENTIFIER PACKET
(Response To Code %0)

The response contains in the low byte the ASCII code of the string of characters identified by the name of the Mainframe plus the version of the software running on the Communication Controller. On Systems with Software version 6.6 or higher, a software version for the Main Controller is also provided in brackets.

Table 4.14: Module Identifier Data Packet Structure

Word	Contents	
	db15..8	db7..0
2	0	"S"
3	0	"Y"
4	0	"1"
5	0	"2"
6	0	"7"
7	0	" "
8	0	"V"
9	0	"x"
10	0	"."
11	0	"x"
12	0	" "
13	0	"("
14	0	"M"
15	0	"a"
16	0	"i"
17	0	"n"
18	0	" "
19	0	"V"
20	0	"x"
21	0	"."
22	0	"x"
23	0	")"

4.4.3. BOARD CHARACTERISTICS PACKET
(Response To Code %3)

The Response consists in 5 words, containing in the lower and higher bytes the number identifier of the 10 Boards inserted in the relevant slots.

Table 4.15: Board ID Packet Structure

Word	Contents	
	db15..8	db7..0
2	Board ID slot 1	Board ID slot 0
3	Board ID slot 3	Board ID slot 2
4	Board ID slot 5	Board ID slot 4
5	Board ID slot 7	Board ID slot 6
6	Board ID slot 9	Board ID slot 8

Board ID slot n:

These 10 bytes represent a field that contains the Board ID number and the Board Channels' polarity.

The structure of each byte is the following:

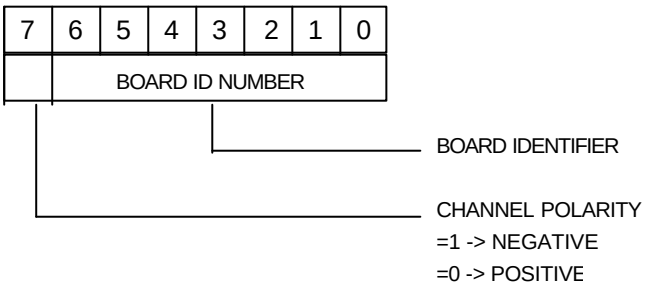

Fig. 4.3: Board ID Byte Structure

The Board Identifier Number is different for each SY127 board and its values are displayed in Table 4.16.

Table 4.16: Board Identifier Number

Board ID (Hex)	Vmax	Imax	Vres	Ires
1	2KV	3mA	500mV	1uA
2	3KV	3mA	1V	1uA
3	4KV	2mA	1V	1uA
4	8KV	500uA	2V	1uA
5	6KV	1mA	2V	1uA
6	800.0V	500.0uA	200mV	200nA
7	8KV	200.0uA	2V	100nA
8	6KV	200.0uA	2V	100nA
9	200.0V	200.0uA	100mV	100nA
A	2KV	200.0uA	500mV	100nA
B	4KV	200.0uA	1V	100nA
C	6KV	1mA	2V	1uA
D	Not Imp.			
E	3KV	3mA	1V	1uA
F	4KV	2mA	1V	1uA
10	800.0V	200.0uA	200mV	100nA
11	Not Imp.			
12	8KV	200.0uA	2V	100nA
13	10KV	1mA	3V	1uA
14	Not Imp.			
15	Not Imp.			
16	10KV	200.0uA	3V	100nA
17	15KV	200.0uA	4V	100nA
18	15KV	1mA	4V	1uA
19	20KV	200.0uA	4V	100nA
1A	2.5KV	5mA	1V	2uA
1B	1KV	10mA	250mV	5uA
1C	Not Imp.			
1D	20KV	500uA	4V	1uA
1E	10KV	2mA	3V	1uA
1F	I/O Mod.			
20	200.0V	40uA	100mV	10nA
21	800.0V	40uA	200mV	10nA
22	2KV	40uA	500mV	10nA
23	4KV	40uA	1V	10nA
24	6KV	40uA	2V	10nA
25	8KV	40uA	2V	10nA
26	10KV	40uA	3V	10nA
27	15KV	40uA	4V	10nA
28	20KV	40uA	4V	10nA
29	Not Imp.			
2A	Not Imp.			
2B	Not Imp.			
2C	Not Imp.			
2D	Sp. Mod.			
2E	Not Imp.			
2F	Not Imp.			

For all the boards but those with ID 20-28 the following holds:

- If Vres < 1 Volt then the voltage has a decimal figure on the RS232 terminal display but only integer values are displayed via CAENET and on the front panel which correspond to the true value multiplied by 2 (if Vres = 500 mV), or by 10 (if Vres = 200 mV or if Vres = 100 mV).

- If Vres ≥ 1 Volt then on the RS232 terminal display the voltage is an integer number, integer values are displayed via CAENET and on the front panel also, which correspond to the true value.

- If Ires = 100nA or 200nA then on the RS232 terminal display the current has a decimal figure but only integer values are displayed via CAENET and on the front panel which correspond to the true value multiplied by 10.

- If Ires = 1uA then on the RS232 terminal display the current is an integer number, integer values are displayed via CAENET and on the front panel also, which correspond to the true value

For boards with ID 20-28 the following holds:

- For the voltage see points above.

- For the current, these are boards with Imax = 40uA and Ires = 10nA, that is they would need two decimal figures, if expressed in uA. They are expressed instead in 10th of nA, with values ranging from 1 = 10nA to 4000 = 40000nA, and this is what happens on the RS232 terminal display, via CAENET and on the panel display.

4.4.4. READ PROTECTION BIT CHARACTERISTICS
(Response To Code %4)

The response content is shown in Fig. 4.4.

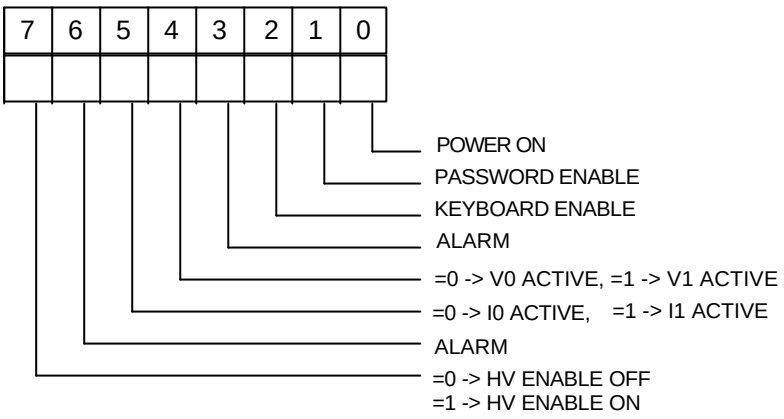

Fig. 4.4: Protection Word Structure

Protection Status word bit pattern:

bit **0** **Power ON**
bit **1** **Password enabled**
bit **2** **Keyboard enabled**
bit **3** **Alarm ***
bit **4** **if 0, V0 active - if 1, V1 active**
bit **5** **if 0, I0 active - if 1, I1 active**
bit **6** **Alarm ***
bit **7** **if 0, HV-ENABLE is OFF - if 1, HV-ENABLE is ON**

***** They both have the same meaning: Alarm signal for OVV, UNV, TRIP in any of the channels of the system SY 127 which has been called.

Note on the Alarm bit:

If during a READ operation this bit is set to 1, then an Alarm condition has taken place, which could be due to a Trip-off, an Over-voltage or an Under-voltage status of the channel. An Alarm condition can be reset (Clear Alarm operation) with a %32 code: then the bit should toggle to zero if it was set, or remain zero if no alarm condition was present.

Warning: If, following a Clear Alarm operation, bit 3 is still set to 1, then the Alarm condition persists, and it is caused either by an Over-voltage or by an Under-voltage status of the HV channel.

4.4.5. READ STREAMER TUBES CONDITIONING PARAMETERS
(Response To Code %5)

The response content is shown in the following.

Streamer tubes conditioning phase: bit pattern

bit **0-3** sequential number of the phase (0 to 15 max);
bit **5** if = 1 , means that the conditioning process was terminated by time-out occurrence;
bit **6** if = 1 , means that the channel is undergoing a "recovery" at zero voltage (this lasts Time-Low(N) seconds, where N = phase number as given by bits 0-3);
bit **7** if = 1 , means that the conditioning process is active

4.4.6. READ CHANNEL TO GROUP ASSIGNMENT WORD
(Response To Code %40)

The response is a group of 20 words containing in the lower and higher bytes the group assignment words (code %n50) of all channels in the mainframe.

Table 4.17: Channel To Group Assignment Packet Structure

Word	Contents	
	db15..8	db7..0
2	Assign. Word Channel 1	Assign. Word Channel 0
3	Assign. Word Channel 3	Assign. Word Channel 2
4	Assign. Word Channel 5	Assign. Word Channel 4
..	...	...
21	Assign. Word Channel 39	Assign. Word Channel 38

The Assignment to Channel Word is described in § 4.3.4.

4.4.7. READ CHANNEL PARAMETERS PACKET
(Response To Code %n01)

The response content is shown in the following Table.

Table 4.18: Channel Parameters Packet Structure

Word	**Contents**
2	V0set<15..0>
3	V1set<15..0>
4	I0set<15..0>
5	I1set<15..0>
6	Rup<15..0>
7	Rdwn<15..0>
8	Trip<15..0>
9	Status<7..0>
10	Group Assignment Word<7..0>
11	Vmon<15..0>
12	Imon<15..0>
13	Phase STC<7..0>
14	Time STC
15	Board ID<7..0>
16	Meaningless
17	Ch. Name <15..8><7..0>
18	Ch. Name <15..8><7..0>
19	Ch. Name <15..8><7..0>
20	Ch. Name <15..8><7..0>
21	Ch. Name <15..8><7..0>

The data contained in the parameters have the same structure of the set parameters word, see § 4.3.1. The Status Word (9th word in the packet) is available on 7 bits (see Fig. 4.5).

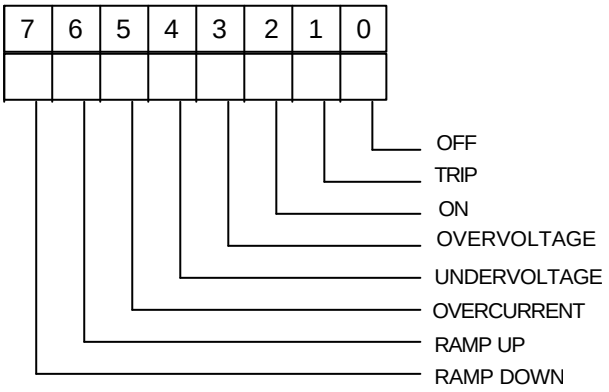

Fig. 4.5: Status Word Structure

Status Word bit pattern:

bit **0** **OFF** (if set to 1, channel is OFF and bit 2 goes to 0)
bit **1** **TRIP** (if set to 1, channel was switched OFF due to a TRIP)
bit **2** **ON** (if set to 1, channel is ON and bit 0 goes to 0)
bit **3** **OverVoltage** (if set to 1, channel is in OVV at the time of reading)
bit **4** **UnderVoltage** (if set to 1, channel is in UNV at the time of reading)
bit **5** **OverCurrent** (if set to 1, channel is in OVC at the time of reading)
bit **6** **Ramp UP** (if set to 1, channel is undergoing a Ramp-Up phase)
bit **7** **Ramp DOWN** (if set to 1, channel is undergoing a Ramp-Down phase)

4.4.8. READ VMON, IMON, STATUS, STCPHASE, STCTIME OF CHANNELS IN GROUP G

(Response To Code %g41)

The response is a group of 5 words containing the Vmon, Imon, Status, STC phase and STC time words for each channel in group G. If e.g. a group contains 16 channels, the response contains 16*5=80 words. Group ALL will respond with 200 words.

4.4.9. READ V0SET, V1SET, I0SET, I1SET OF CHANNELS IN GROUP G

(Response To Code %g42)

The response is a group of 4 words containing the V0set, V1set, I0set, I1set words for each channel in group G. If e.g. a group contains 16 channels, the response contains 16*4=64 words. Group ALL will respond with 160 words.

4.4.10. READ RAMP-UP, RAMP-DOWN, TRIP OF CHANNELS IN GROUP G

(Response To Code %g43)

The response is a group of 3 words containing Ramp-Up, Ramp-Down, Trip words for each channel in group G. If e.g. a group contains 12 channels, the response contains 12*3=36 words. Group ALL will respond with 120 words.

4.4.11. PARAMETERS SETTING SLAVE RESPONSE

After a Set Command the SY127 responds in the following way:

- If the Set operation is correct it responds with an error code = 0, and it is Busy for about 20msec;

- If it is Busy (for a preceding Set operation) it responds with an error Code = %FF00 Module Busy.

APPENDIX A: SOFTWARE EXAMPLES (V288 USERS)

The details of using the Mod. V288 to communicate with the Mod. SY127 are explained by means of examples:

- VMECAENET.H: Declaration for communication via VME with the Mod. V288;

- VMCAENET.C: Caenet Package for V288 Module.

These two listings describe the function and general design of a driver for the Mod V288; all the possible errors are handled, included the VME Buserror.

```
/************************************************************************/
/*                                                                      */
/*             ------       C . A . E . N .   SpA       ------          */
/*                                                                      */
/*    VMCAENET.H - Declarations for communication with V288 Module      */
/*                                                                      */
/************************************************************************/

#ifndef   uchar
#define   uchar                        unsigned char
#endif
#ifndef   ushort
#define   ushort                      unsigned short
#endif

/* Constants for vme_cycles routines */
#define   BYTE                                    1
#define   WORD                                    2
#define   LWORD                                   4

/* Errors returned by caenet_read and caenet_write; the positive ones
  are depending from V288 Module and not from CAENET network */

#define   TUTTOK                                  0
#define   E_NO_Q_IDENT                            1
#define   E_NO_Q_CRATE                            2
#define   E_NO_Q_CODE                             3
#define   E_NO_Q_DATA                             4
#define   E_NO_Q_TX                               5
#define   E_NO_Q_RX                               6
#define   E_LESSDATA                              7
#define   E_BUSERR                                8

/* Number of iterations before deciding that V288 does not answer */
#define   TIMEOUT                                -1

#define   Q                           (ushort)0xfffe
#define   V288                                    1

/* Registers of V288 Module */
#define   STATUS                     (v288addr+0x02)
#define   TXMIT                      (v288addr+0x04)

#define   LOBYTE(x)                (uchar)((x)&0xff)
#define   HIBYTE(x)       (uchar)(((x)&0xff00) >> 8)

/*
  Interface between the user program and V288; these functions are defined
  in file Vmcaenet.c
*/
int  caenet_read();
int  caenet_write();
int  read_caenet_buffer();

/* Declarations of Global Variables defined in the user program */
extern  unsigned       v288addr,craten;
extern  ushort                   code;
```

```
/*************************************************************************/
/*                                                                       */
/*             ------       C . A . E . N .   SpA       ------           */
/*                                                                       */
/*    VMCAENET.C - Caenet Package for V288 Module                        */
/*                                                                       */
/*************************************************************************/

#include "vmcaenet.h"


/***-----------------------------------------------------------------------

  Read_data

    ---------------------------------------------------------------------***/
int read_data(datovme)
ushort *datovme;
{
ushort q=0;
vme_read(v288addr,datovme,WORD);
vme_read(STATUS,&q,WORD);
return((q == Q) ? TUTTOK : TIMEOUT);
}

/***-----------------------------------------------------------------------

  Wait_resp

    ---------------------------------------------------------------------***/
int wait_resp(datovme)
ushort *datovme;
{
int i=0;
ushort q=0;
while(i!=TIMEOUT && q!=Q)
     {
      vme_read(v288addr,datovme,WORD);
      vme_read(STATUS,&q,WORD);
      i++;
     }
return((i == TIMEOUT) ? TIMEOUT : TUTTOK);
}

/***-----------------------------------------------------------------------

  Send_comm

    ---------------------------------------------------------------------***/
int send_comm(vmeaddress,datovme)
unsigned int vmeaddress;
ushort datovme;
{
int i=0;
ushort q=0;
while(i!=TIMEOUT && q!=Q)
```

```
     {
      if(!vme_write(vmeaddress,&datovme,WORD))
         return E_BUSERR;
      vme_read(STATUS,&q,WORD);
      i++;
     }
return((i == TIMEOUT) ? TIMEOUT : TUTTOK);
}

/***-------------------------------------------------------------------------

  Caenet_read: Called by user programs to load "byte_count" bytes from
               CAENET into the buffer pointed by "*dest_buff".

               The VME address of V288, the CAENET crate number and the
               CAENET code are found in global variables.

               Caenet_read returns TUTTOK = 0 if everything has worked;
               It returns one from seven different errors (defined as
               positive constants in Vmcaenet.h) if it has received one
               error which strictly depends from V288 Module;
               It returns a negative error (depending from the CAENET slave
               module) if the CAENET communication has not worked.

     Remember: Module V288 can return three "general" negative errors
               related to the CAENET network that this routine does not
               handle separately from the "slave specific" ones.

    ------------------------------------------------------------------------***/
int caenet_read(dest_buff,byte_count)
uchar *dest_buff;
int byte_count;
{
int i,esito;
ushort mstident=V288,datatemp;
short dato;

if((esito=send_comm(v288addr,mstident)) == TIMEOUT)
   return E_NO_Q_IDENT;
else if(esito == E_BUSERR)
   return esito;

/* Transmit Crate Number */
if((esito=send_comm(v288addr,(ushort)craten)) == TIMEOUT)
   return E_NO_Q_CRATE;
else if(esito == E_BUSERR)
   return esito;

/* Transmit Code       */
if((esito=send_comm(v288addr,(ushort)code)) == TIMEOUT)
   return E_NO_Q_CODE;
else if(esito == E_BUSERR)
   return esito;

/* Start Transmission        */
if((esito=send_comm(TXMIT,mstident)) == TIMEOUT)
   return E_NO_Q_TX;
```

```
else if(esito == E_BUSERR)
   return esito;

if(wait_resp(&dato) == TIMEOUT)
   return E_NO_Q_RX;

if(dato == TUTTOK)                          /* Test on the operation     */
   for(i=0;i<byte_count;i+=2)
      {
       if(read_data(&datatemp) == TIMEOUT && i<byte_count-1)
          return E_LESSDATA;
       dest_buff[i]   = HIBYTE(datatemp);
       dest_buff[i+1] = LOBYTE(datatemp);
      }
return dato;
}

/***-------------------------------------------------------------------------

 Caenet_write: Called by user programs to transfer "byte_count" bytes to
               CAENET from the buffer pointed by "*source_buff".

               The VME address of V288, the CAENET crate number and the
               CAENET code are found in global variables.

               Caenet_write returns TUTTOK = 0 if everything has worked;
               It returns one from seven different errors (defined as
               positive constants in Vmcaenet.h) if it has received one
               error which strictly depends from V288 Module;
               It returns a negative error (depending from the CAENET slave
               module) if the CAENET communication has not worked.

     Remember: Module V288 can return three "general" negative errors
               related to the CAENET network that this routine does not
               handle separately from the "slave specific" ones.

    -------------------------------------------------------------------------***/
int caenet_write(source_buff,byte_count)
uchar *source_buff;
int byte_count;
{
int i,esito;
ushort mstident=V288,datatemp;
short dato;

if((esito=send_comm(v288addr,mstident)) == TIMEOUT)
   return E_NO_Q_IDENT;
else if(esito == E_BUSERR)
   return esito;

/* Transmit Crate Number */
if((esito=send_comm(v288addr,(ushort)craten)) == TIMEOUT)
   return E_NO_Q_CRATE;
else if(esito == E_BUSERR)
   return esito;

/* Transmit Code       */
```

```
if((esito=send_comm(v288addr,(ushort)code)) == TIMEOUT)
   return E_NO_Q_CODE;
else if(esito == E_BUSERR)
   return esito;

/* Transmit data       */
for(i=0;i<byte_count;i+=2)
   {
    datatemp=(ushort)source_buff[i]<<8 | source_buff[i+1];
    if((esito=send_comm(v288addr,datatemp)) == TIMEOUT)
       return E_NO_Q_DATA;
    else if(esito == E_BUSERR)
       return esito;
   }

/* Start transmission                 */
if((esito=send_comm(TXMIT,mstident)) == TIMEOUT)
   return E_NO_Q_TX;
else if(esito == E_BUSERR)
   return esito;

if(wait_resp(&dato) == TIMEOUT)
   return E_NO_Q_RX;

return dato;
}

/***---------------------------------------------------------------------

  Read_caenet_buffer: Called by user programs to load "byte_count" bytes from
                      CAENET buffer into the buffer pointed by "*dest_buff".

    ---------------------------------------------------------------------***/
int read_caenet_buffer(dest_buff,byte_count)
uchar *dest_buff;
int byte_count;
{
int    i;
ushort datatemp;

for(i=0;i<byte_count;i+=2)
   {
    if(read_data(&datatemp) == TIMEOUT && i<byte_count-1)
       return E_LESSDATA;
    dest_buff[i]   = HIBYTE(datatemp);
    dest_buff[i+1] = LOBYTE(datatemp);
   }
return TUTTOK;
}
```