OPERATOR'S MANUAL

MODEL 1877S

96 CHANNEL FASTBUS TIME-TO-DIGITAL CONVERTER

CE

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(ECO 1202)

LeCroy

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CE CONFORMITY

CONDITIONS FOR CE CONFORMITY

Since this product is a subassembly, it is the responsibility of the end user, acting as the system integrator, to ensure that the overall system is CE compliant. This product was demonstrated to meet CE conformity using a CE compliant crate housed in an EMI/RFI shielded enclosure. It is strongly recommended that the system integrator establish these same conditions.

CAUTION

COOLING

It is imperative that the module 1877S TDC be well cooled. Be sure fans move sufficient air to maintain exhaust air temperature at less than 50° C.

INSTALLATION

“Hot” insertion (insertion with crate power turned on) of modules is supported in accordance with the FASTBUS specification.

SPECIFICATIONS

The information contained in this manual is subject to change without notice. The reference for product specification is the Technical Data Sheet effective at the time of purchase.

ELECTROSTATIC SENSITIVITY

While measures have been taken to protect the MTD133B ASIC from electrostatic damage, it is still imperative to follow anti static procedures when handling this CMOS device. Removal of the MTD133B from its socket will void the product warranty.

TABLE OF CONTENTS

1. General Information

Purpose 9
Unpacking and Inspection 9
Product Assistance 9
Maintenance Agreements 9
Documentation Discrepancies 10
Software Licensing Agreement 10
Service Procedure 10
Warranty 10

2. Product Description

Introduction 11
General Description 11
Specifications 12
Front Panel 12
- Displays 12
- Inputs 12
- Outputs 13

General Operation 14
- Setup 14

Control and Status Registers 14
- Control and Status Register 0 14
- Control and Status Register 1 17
- Control and Status Register 3 19
- Control and Status Register 5 19
- Control and Status Register 7 19
- Control and Status Register 16 19
- Control and Status Register 18 20

FASTBUS Operations 21
- FASTBUS Address cycle 21
  - Logical Addressing 21
  - Geographic Addressing 21
  - Broadcast Addressing 21

Data Space 21
- Header Word Format 22
- Data Word Format 23

Readout 23
- Single Read from Data Space 23
- Block Transfer Read from Data Space 24

FASTBUS Write to Data Memory 24
Tester 24
Fast Clears 24
Allocation of Restricted Use Lines 24
User CSR Space - Sparsification Memory 26
Example Code 26

3. Installation

General Installation 29
Cables 29

4. Theory of Operation
General Description of Buffer Architecture 31
Multi-Event Buffer Memory Organization 32
Buffer Memory Pointers 32
Buffer Full/Empty Conditions 32
Acquisition and Buffering 33
Readout of MTDs 33
Organization of Data in Events 33
FASTBUS Access to Module 34
Control and Status Registers 34
Secondary Addressing in Data Space 34
Default Addressing Mode 34
Memory Test Mode (MTM) 35
Mechanisms for FASTBUS Readout 36
Load Next Event 36
Block Transfers from Data Space 36
Multi-Module Data Transfers (Multi-Block) 37
Multi-Ranging ADC Compatibility 38
Configuration Considerations 38
Sparse Data Readout 38

5. Index 41

List of Figures

Figure 1 CSR 0 Read Bit Definition 15
Figure 2 CSR 0 Write Bit Definition 15
Figure 3 CSR1 Bit Definition 17
Figure 4 CSR 16 Bit Definition 20
Figure 5 CSR 18 Bit Definition 20
Figure 6 1877S Header Word 22
Figure 7 1877S Data Word 23
Figure 8 Simplified 1877S Interface/Buffer Block Diagram 31
Figure 9 1877S Circular Buffer 32
Figure 10 Example: MQT300 Low Range Data 39

GENERAL INFORMATION

PURPOSE

This manual is intended to provide instruction regarding the setup and operation of the covered instruments. In addition, it describes the theory of operation and presents other information regarding its functioning and application.

UNPACKING AND INSPECTION

It is recommended that the shipment be thoroughly inspected immediately upon delivery. All material in the container should be checked against the enclosed Packing List and shortages reported promptly. If the shipment is damaged in any way, please notify the Customer Service Department or the local field service office. If the damage is due to mishandling during shipment, you may be requested to assist in contacting the carrier in filing a damage claim.

WARRANTY

LeCroy warrants its instrument products to operate within specifications under normal use and service for a period of one year from the date of shipment. Component products, replacement parts, and repairs are warranted for 90 days. This warranty extends only to the original purchaser. Software is thoroughly tested, but is supplied "as is" with no warranty of any kind covering detailed performance. Accessory products not manufactured by LeCroy are covered by the original equipment manufacturers' warranty only.

In exercising this warranty, LeCroy will repair or, at its option, replace any product returned to the Customer Service Department or an authorized service facility within the warranty period, provided that the warrantor's examination discloses that the product is defective due to workmanship or materials and has not been caused by misuse, neglect, accident or abnormal conditions or operations.

The purchaser is responsible for the transportation and insurance charges arising from the return of products to the servicing facility. LeCroy will return all in-warranty products with transportation prepaid.

This warranty is in lieu of all other warranties, express or implied, including but not limited to any implied warranty of merchantability, fitness, or adequacy for any particular purpose or use. LeCroy shall not be liable for any special, incidental, or consequential damages, whether in contract, or otherwise.

PRODUCT ASSISTANCE

Answers to questions concerning installation, calibration, and use of LeCroy equipment are available from the Customer Service Department, 700 Chestnut Ridge Road, Chestnut Ridge, New York, 10977-6499, (914) 578-6030.

MAINTENANCE AGREEMENTS

LeCroy offers a selection of customer support services. For example, Maintenance Agreements provide extended warranty that allows the customer to budget maintenance costs after the initial warranty has expired. Other services such as installation, training, on-site repair, and addition of engineering improvements are available through specific Supplemental Support Agreements. Please contact the Customer Service Department for more information.

DOCUMENTATION DISCREPANCIES

LeCroy is committed to providing state-of-the-art instrumentation and is continually refining and improving the performance of its products. While physical modifications can be implemented quite rapidly, the corrected documentation frequently requires more time to produce. Consequently, this manual may not agree in every detail with the accompanying product and the schematics in the Service Documentation. There may be small discrepancies in the values of components for the purposes of pulse shape, timing, offset, etc., and, occasionally, minor logic changes. Where any such inconsistencies exist, please be assured that the unit is correct and incorporates the most up-to-date circuitry.

SOFTWARE LICENSING AGREEMENT

Software products are licensed for a single machine. Under this license you may:

- Copy the software for backup or modification purposes in support of your use of the software on a single machine.
- Modify the software and/or merge it into another program for your use on a single machine.
- Transfer the software and the license to another party if the other party accepts the terms of this agreement and you relinquish all copies, whether in printed or machine readable form, including all modified or merged versions.

SERVICE PROCEDURE

Products requiring maintenance should be returned to the Customer Service Department or authorized service facility. If under warranty, LeCroy will repair or replace the product at no charge. The purchaser is only responsible for the transportation charges arising from return of the goods to the service facility. For all LeCroy products in need of repair after the warranty period, the customer must provide a Purchase Order Number before any inoperative equipment can be repaired or replaced. The customer will be billed for the parts and labor for the repair as well as for shipping. All products returned for repair should be identified by the model and serial numbers and include a description of the defect or failure, name and phone number of the user. In the case of products returned, a Return Authorization Number is required and may be obtained by contacting the Customer Service Department at (914) 578-6030.

PRODUCT DESCRIPTION

INTRODUCTION

The LeCroy Model 1877S provides 96 channels of either Common Start or Common Stop multi-hit Time-to-Digital Conversion designed for elementary particle or nuclear physics experiments. All input time signals to be measured, “hits”, are received via differential ECL (dECL) front panel inputs. Each channel exhibits 500 psec LSB and can store up to 16 hits within a 32.768 μsec range. The time measurement is performed using the MTD133B, a full custom ASIC developed by LeCroy Corporation.

In addition to operation as a TDC, the 1877S includes several features which make it suitable for use with multi-ranging ADC front-ends such as the LeCroy MQT300.

GENERAL DESCRIPTION

The 1877S Time-to-Digital Converter offers all the flexibility of the 1870 Series Pipeline Time-to-Digital Converter with a 500 psec least count and can store up to 16 hits per channel within a 32.768 μsec full scale range. Time data relative to the common input is stored in a LIFO within the MTD133B until it is transferred to the 1877S’s buffer memory. The MTD133B’s internal LIFO depth is programmable from 1 to 16 hits. Additionally, the full scale range of the MTD133B may be programmed from 0 to 32.768 μsec.

Each 1877S has 96 channels of front panel hit inputs and a Common input. All inputs are differential ECL (dECL) and are terminated by a balanced 110 ohm impedance matching network. The 1877S can operate in either Common Start or Common Stop mode. In Common Start mode, the common input receives a start pulse and the individual channels can register up to 16 subsequent hits during a programmable Common Start Timeout window. In Common Stop mode, the 96 front panel inputs register individual channel hits and the common inputs latches a stop pulse. Each channel can be programmed to detect rising and/or falling edges (hits) and can store up to 16 hits. Selected edges can be detected with as little as 10 nsec separating them. If more than 16 hits occur per channel, only the last 16 hits are retained. If multiple common input pulses are received, only the first is registered.

Operation of the 1877S can be divided into four phases: programming, acquisition, buffering and readout. Once the control/status registers have been programmed the module is in acquisition mode and ready to latch hits. In Common Start mode, the acquisition phase begins when the module latches a start and ends after a user programmable common start timeout. No hits will be recorded after the programmed hit window expires. A front panel dECL input is also provided to allow the use of an external timeout if desired. The maximum acquisition time, however, is internally restricted to 32.768 μsec regardless of the application of an external timeout. Immediately following the acquisition phase, the time data is transferred to an eight event circular buffer, awaiting readout to FASTBUS. The module automatically returns to acquisition mode once all the time data for a particular event has been safely buffered. Readout of events previously stored in the buffer memory may occur simultaneously with acquisition or buffering without any performance penalty.

In both Common Start and Common Stop modes, a programmable fast clear window begins immediately following the end of acquisition. During the fast clear window (FCW), a user can safely clear an event (e.g. based on a experiment trigger decision) and return to acquisition mode, thus saving the time necessary for buffering and reading out the event. The FCW can range from 1 μsec to 524 μsec.

The data for each event stored in the multi-event circular buffer is preceded by a header word identifying the address (geographic or logical), the buffer number, and the word count for the event. A parity bit is set to give an even number of bits for the word. The timing measurements of the 1877S are stored as 32 bit words. The least significant 16 bit word is the time measurement data. The most significant 16 bit word contains the channel number, phase (rising or falling), even parity, MTD133B hit count (modulo 4), and the geographic address.

The functionality of the 1877S can be tested using either an internal tester or a front panel dECL test input. The internal tester can be programmed to produce 1, 2, 4 or 8 pulses with a width and separation of 125, 250, 1000, or 2000 nsec. Either rising, falling, or both edges of the pulses are selectable for detection, creating up to 16 internal hits per channel. Testing can be performed in either Common Start or Common Stop modes.

Unlike the LeCroy Model 1877 and previous LeCroy FASTBUS modules, no support is provided for the auxiliary function card. Also, no triggers are provided at the auxiliary connector.

SPECIFICATIONS

Please refer to the Model 1877S technical data sheet for a complete summary of all relevant specifications.

FRONT PANEL

The LeCroy Module 1877S TDC front panel provides connectors for system integration and LEDs to indicate the module status and assist system debugging. Cables necessary for proper installation can be purchased from LeCroy. See "Installation" for more information regarding cabling.

Displays

Two colored LEDs reside on the front panel of the 1877S to indicate the status of operations. A brief description of each is listed below. The LED illumination is stretched to a minimum of 10 msec to aid in viewing.

Slave Addressed LED: As per the FASTBUS specification, this yellow LED is lit whenever the TDC module is attached to the FASTBUS as a slave.

Common Hit LED: This green LED is illuminated whenever the TDC registers a common hit (start or stop). The common hit may be received via the front panel input marked COM, a FASTBUS command, or it may be created by the module's internal tester. See "Tester" for more information regarding the internal tester.

Inputs

All front-panel inputs to the 1877S are differential ECL compatible with the ECLine standard. The "+" input is quiescently at least 200 mV more negative than the "-" input. Each pair of differential inputs is terminated with an effective 112 ohms.

All hit inputs are received via six 34 pin connectors. A 3M connector type 3414-6034 will mate with the TDC header and provide strain relief. Pin 33 is connected to circuit ground, and pin 34 is connected to chassis ground. The circuit ground and the chassis ground are connected to each other on the printed circuit board through 100 ohms. The hit inputs are numbered from top to bottom in ascending order. Four control inputs are differentially received via an 8 pin header located at the bottom of the front panel.

The control signals can be connected by single pair headers AMP part number 5-87456-2 or they can all be connected simultaneously by a 8 position connector AMP part number 87456-2. A brief description of each input follows below:

COM: A dECL input which receives the common input pulse. Any pulse, whether it be a start or a stop, received via the COM input is global to all 96 channels. In Common Start mode the pulse acts as a global start for every channel, and in Common Stop mode it acts as a global stop for every channel. Front panel input of this signal is selected by setting CSR1<1> to 0 (default). This signal may be daisy chained on the front panel if the two jumpers connecting the 112 ohm input termination are removed from all except the last module in the chain.

CLR: A dECL input used to issue fast clears to the module. A clear pulse can be issued at anytime inside the Fast Clear Window or when buffering is not in progress, provided it is at least 40 nsec wide. When a clear is issued, the data of a just measured, unbuffered, event is cleared and the module returns to acquisition mode 300 nsec after the rising edge of the pulse. The control and status registers are not affected by a clear. Front panel sourcing of this signal is always enabled. This signal may be daisy chained on the front panel if the two jumpers connecting the 112 ohm input termination are removed from all except the last module in the chain.

TIME: A dECL input used to receive the Common Start Timeout pulse. When operating in Common Start mode, it is necessary to define a period of time when the TDC will register hits. The beginning of this period starts with receipt of the Common Start. The end of this time occurs when the module receives the timeout pulse. Front panel input of this signal is selected by setting CSR1<7:4> to 0 (default). This signal may be daisy chained on the front panel if the two jumpers connecting the 112 ohm input termination are removed from all except the last module in the chain. This signal can also be provided by an on board programmable timer. If the front panel source for this signal is selected but does not arrive, the module will still time out after 32 μsec. The TIME input may also be used as a level sensitive input which will hold the MTD133B's Hit Counter and LIFO in cleared condition. While the TIME input is asserted, no hits will be registered into the MTD133B LIFO and transitions on the channel inputs will not increment the Hit Count.

IN: All 96 dECL inputs are used to receive individual channel hits. In Common Start mode the stop pulses are received via the connectors marked IN, and in Common Stop mode the start pulses are received.

Outputs

The one front panel output from the 1877S is differential ECL. The "+" output should be quiescently at least 200 mV more negative than the "-" output. This output is terminated with 112 ohms to -2 V.

BIP: Buffering in Progress (BIP) is a single dECL signal provided to aid in readout. While BIP is true, the current event's data is being buffered and the data from this event is not ready for readout via FASTBUS. BIP will also become true when all buffers are full and no further events can be accepted. In the event of a fast clear, BIP will go false within 300 nsec of the rising edge of the fast clear pulse. Of course, events previously buffered may be readout via FASTBUS at any time.

GENERAL OPERATION

The operation of the 1877S can be divided into four unique phases. The first phase includes all the setup necessary before the 1877S TDC can successfully be used. This includes installation of the module and programming the control registers. The module will not latch hits until the control registers have been programmed. Once all the setup is complete, the module is in acquisition mode and ready to accept hits. The module remains in acquisition mode until either a Common Start Timeout or a Common Stop occurs, depending on the acquisition mode programmed.

Following acquisition mode, the module buffers the data into a multiple event data buffer. It can take a maximum of 78 μsec and minimum of 1.7 μsec for an event to be buffered, depending on the number of hits in the event. While the data is being buffered, the Buffering In Progress (BIP) signal is true. The user can begin the final phase, readout, as soon as BIP has been deasserted indicating that the event is safely buffered. Previously buffered events can be readout while the most current event is being buffered, without a penalty in buffering speed.

Setup

As per the FASTBUS specification, the 1877S may be inserted in the FASTBUS crate with the power either on or off. No special precautions are required when attaching the front panel connectors. If it is desired to daisy chain the COM or CLR signals, the jumpers connecting the terminations for these signals must be removed on all except the last unit in the daisy chain.

1. **CSR0:** CSR 0 must be programmed for the desired addressing mode and Multi-Block configuration.

2. **CSR1:** CSR 1 contains most of the configuration bits for the module. Acquisition mode, edge selection, and Common Start Timeout (if Common Start operation is chosen) must be set for the desired operational modes. CSR1 also contains internal tester configuration and FASTBUS TR line configurations as well as sparsification enable/disable.

3. **CSR3:** CSR 3 <31:16> must be written to the desired value if logical addressing is being used.

4. **CSR7:** This register must be configured if it is desired to use class N broadcasts.

5. **CSR18:** This register controls the full scale time measurement and LIFO depth (number of hits each channel will register) of the MDT133. After power up or a master reset this register defaults to full scale and maximum LIFO depth.

After the CSR registers are programmed, the unit is ready to acquire data.

CONTROL AND STATUS REGISTERS

Seven Control and Status registers are implemented within the 1877S TDC module.

Control and Status Register 0

When CSR 0 is read, the 1877S presents $103D_h$ on the Address/Data bus lines 16-31 as its manufacturer's identification. CSR0 is the default

register when a primary address to control space is issued. See Figures 1 and 2 for individual bit definitions.

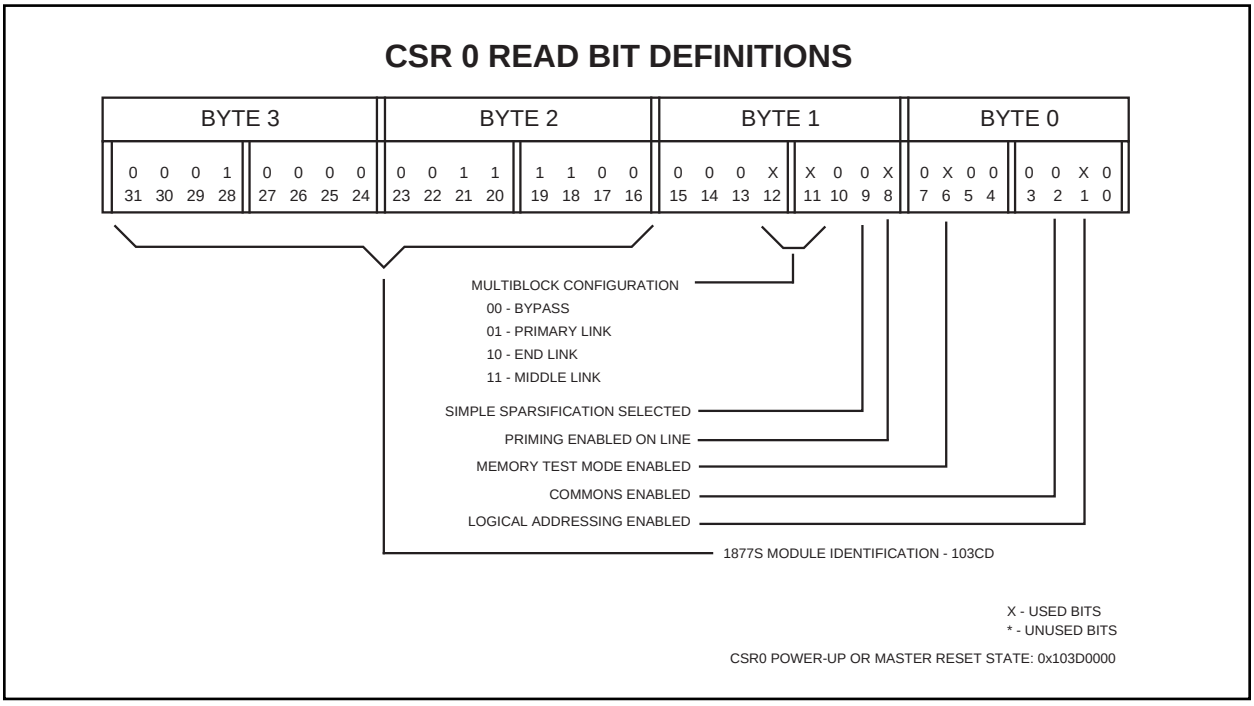

Figure 1: CSR 0 Read Bit Definition

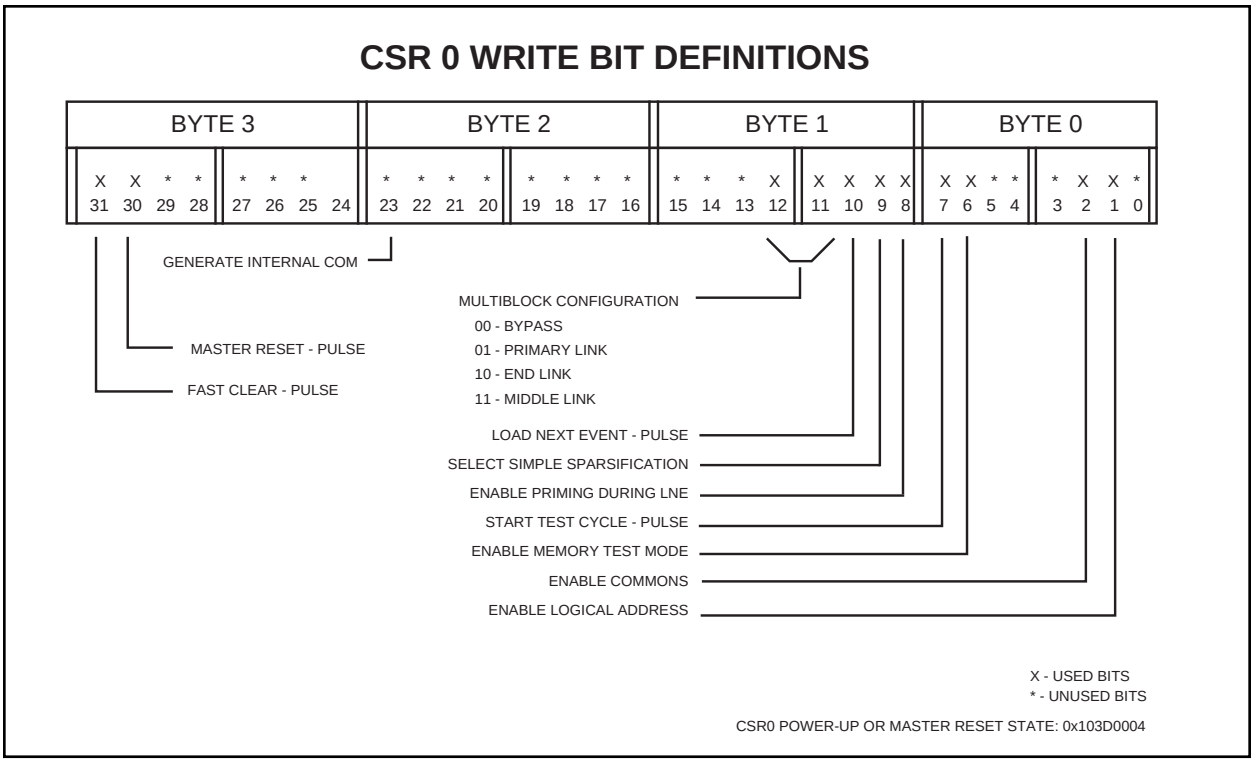

Figure 2: CSR 0 Write Bit Definition

Latched Bits

Logical Address Enable: Bit 1 must be set for the unit to respond to logical addressing.

Select Simple Sparsification: Bit 9 should be set in conjunction with bit 20 of CSR1 to enable sparsification in a simple straightforward way. If bit 9 is off while bit 20 of CSR1 is on, a more complex sparsification is used which leaves some data below threshold. That mode is only appropriate to the operation of this unit with MQT300 front ends.

Enable Priming on Load Next Event: When bit 8 is set, the module primes its internal data pipeline during a Load Next Event command. This option is provided to improve block transfer start-up times and Multi-Block token passing times. Priming on LNE must be enabled when the module is participating in a MDT (Multi-Block) scan. Failure to do so will result in the module responding to the transfer with SS=3, the MDT error response. Enabling Priming on LNE when in Memory Test Mode must be done with great care since the priming operation results in the data space NTA being advanced. Also CSR5 (only visible while in Memory Test Mode) is decremented during priming. It must, therefore, be understood that the use of Priming on LNE with Memory Test Mode enabled results in a non-compliant FASTBUS mode.

Enable Commons: The module is enabled to register common starts or common stops when bit 2 is set. Upon power-up or master reset, bit 2 is set (enabled). The Enable Commons bit must be cleared (disabled) before FASTBUS access to User CSR Space (sparsification memory) is allowed. Attempts to set the Next Transfer Address (NTA) in CSR Space while the Enable Commons bit is set will result in SS=7.

Memory Test Mode Enable: If Bit 6 is set, the memory in data space may be accessed by specifying an NTA in data space corresponding to the memory location desired. This feature may be used to facilitate testing of the memory. In normal operation, this bit should be 0. See "Memory Test Mode (MTM)" for further discussion.

Multi-Module Data Transfer (Multi-Block) Configuration: Bits 11 and 12 configure the module for MDT operation as described in Appendix N to the FASTBUS Specification. Also see "Multi Block" for further discussion of the implementation specific to the 1877S. Priming on LNE (CSR0<8>) must be enabled when the module is participating in a MDT (Multi-Block) scan. Failure to do so will result in the module responding to the transfer with SS=3, the MDT error response.

Pulsed Bits

Fast Clear: Writing Bit 31 will produce a clear signal equivalent to a front panel clear or TR0 clear.

Master Reset: A write to Bit 30 will reset all CSRs to their power up condition.

Load Next Event: This input advances the buffer page pointer by 1 and loads CSR5 with the word count (the contents of the first memory

location of the next page of memory) for that event. This facilitates a block read of the event. Note: CSR5 is only visible to FASTBUS while in Memory Test Mode.

Test Cycle: A write to Bit 7 initiates a burst of pulses from the internal tester.

Internal Com: Writing Bit 23 is equivalent to a pulse on the front panel Com (or TR6 input). This method of generating a Com signal is always enabled.

Note: As per the FASTBUS specification, CSR0<29:22> are clears for corresponding user defined bits CSR0<13:6>.

Control and Status Register 1

The information necessary to define such user-programmable functions as the acquisition mode, the edge detection, the fast clear window, the internal tester's operation and the trigger mode are contained within CSR 1. See Figure 3 for individual bit definitions.

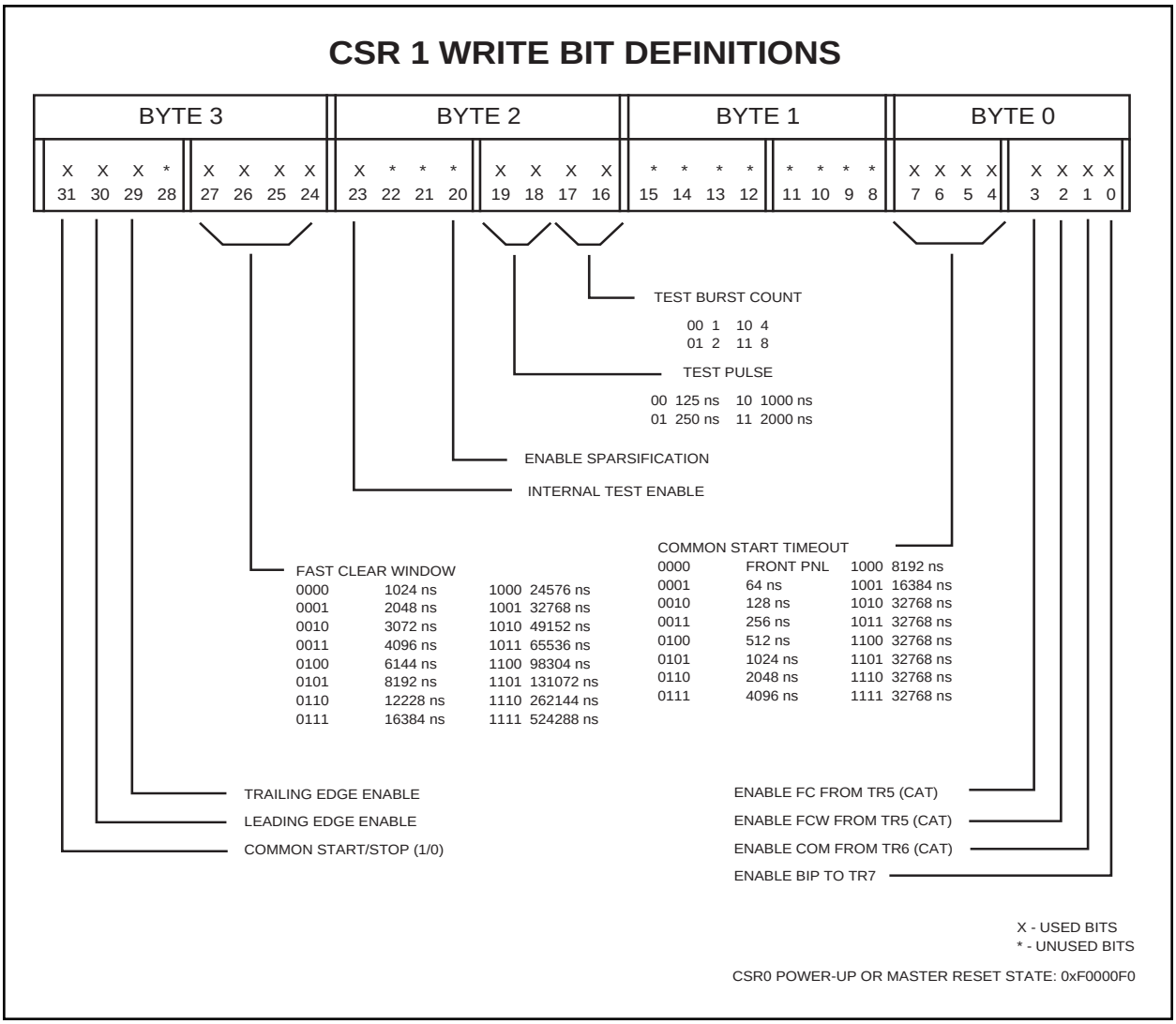

Figure 3: CSR1 Bit Definition

Acquisition Mode: Bit 31 determines whether the TDC will operate in Common Start or Common Stop mode. When a one is written the board operates in Common Start mode, and when a zero is written the board operates in Common Stop mode. When read, the status of the bit is presented.

Rising Edge Enable: Bit 30 determines whether the TDC will register the rising (low-to-high transitions) edges of incoming hits. Hits may be received from either the front panel IN connectors or the on-board tester. When a one is written the board will detect rising edges, and when a zero is written the board will not detect rising edges. When read, the status of the bit is presented.

Falling Edge Enable: Bit 29 determines whether the TDC will register the falling (high-to-low transitions) edges of incoming hits. Hits may be received from either the front panel IN connectors or the on-board tester. When a one is written the board will detect falling edges, and when a zero is written the board will not detect falling edges. When read, the status of the bit is presented.

Fast Clear Window: Bits 24-27 determine the length of time the on-board timer permits the user to issue a fast clear to the module after the end of acquisition. The fast clear window begins immediately following a stop pulse in Common Stop mode and immediately following a Common Start Timeout in Common Start mode. Note, this is independent of a Fast Clear Window supplied from the 1810 CAT module; the two sources are in effect OR'ed together. Once the fast clear window has ended, the current event can no longer be cleared from the multi-event buffer. When read, the status of the bits is presented.

Internal Test Enable: Bit 23 enables operation of the internal tester. When read, the status of the bit is presented.

Enable Sparsification: Bit 20 enables sparsification based on the threshold constants programmed in User CSR Space (sparsification memory). When read, the status of the bit is presented. If bit 20 is set, sparsification will be done with an algorithm, which depends on the setting of CSR0 bit 9. If bit 20 is cleared, there is no sparsification and the state of CSR0 bit 9 is without importance.

Test Pulse Width: Bits 18 and 19 determine the width of the on-board tester's hit pulses. The width can be programmed to be 125, 250, 1000, or 2000 nsec when a 0, 1, 2 or 3 are written respectively. When read, the status of the its is presented.

Tester Burst Count: Bits 16 and 17 determine the number of pulses the on-board tester will generate. The tester can be programmed to create 1, 2, 4 or 8 pulses when 0, 1, 2 or 3 are written respectively. The duty cycle of the pulses is 50% during the burst. When read, the status of the bits is presented.

Common Start Timeout: Bits 4-7 determine the measurement full scale in Common Start mode. These bits define the period of time during which the TDC will detect hits. It is initiated by a start pulse and ended a variable time later by the timeout. The timeout can be programmed to

arrive as quickly as 64 nsec after the start pulse or as long as 32,768 nsec after the start pulse. The Common Start Timeout is only meaningful in Common Start mode. When read, the status of the bits is presented. There exists an option to produce 16 time-out values in the range 2 to 7.5 μsec, if needed by your particular application.

Enable Fast Clear from TR0: Setting Bit 3 permits receipt of a fast clear from TR0. The front panel source of fast clear remains enabled.

Enable FCW from TR5: Setting Bit 2 permits a fast clear window to be supplied from TR5.

Enable COM from TR6 / TR3: If Bit 1 is set to 1, either TR6 or TR3 is enabled as the source for the COM signal, and the front panel COM is disabled. If the 1877S is in Common Stop mode, the TR6 is the source. If in Common Start mode, TR3 is the source.

Enable BIP to TR7: Setting Bit 0 outputs the Buffering in Progress signal to TR7. This should not be set if a model 1810 CAT is in the same crate.

Control and Status Register 3

As per FASTBUS specification, CSR 3 is used to store the desired logical address for the unit. CSR3<31:16> contain the logical address. This register powers up to 0 but is not disturbed by a FASTBUS reset, RB.

Control and Status Register 5

CSR 5 is implemented as an 11 bit read/write register used to control the number of words transferred during a block transfer. During a FASTBUS readout, it is decremented after each transfer. CSR5 is automatically loaded with the word count for the next event to be read out after a Load Next Event command has been issued. Bits 0 through 10 only are meaningful. Bits <31:11> will read back as 0. CSR5 is set to 0x00000000 by a Master Reset.

NOTE: *CSR 5 is only accessible from FASTBUS when the module is in Memory Test Mode.*

Control and Status Register 7

CSR 7 is used to specify the broadcast classes to which an 1877S will respond. It is implemented as an 4 bit read/write register. Bits 3 through 0 correspond to broadcast classes 3 through 0 respectively. If bit N is set, the 1877S will be selected by a broadcast to class N devices. CSR7 is not affected by Bus Reset.

Control and Status Register 16

CSR 16 is implemented as a 16 bit read-write register used to indicate and control the location of the read and the write buffer addresses. CSR 16 <15:8> indicates the next buffer to be readout to FASTBUS, and CSR 16 <7:0> indicates the next buffer to be filled. Master Reset and Power-up reset CSR16 to 0x00000700, reflecting an empty condition. Unused bits always read back as zero.

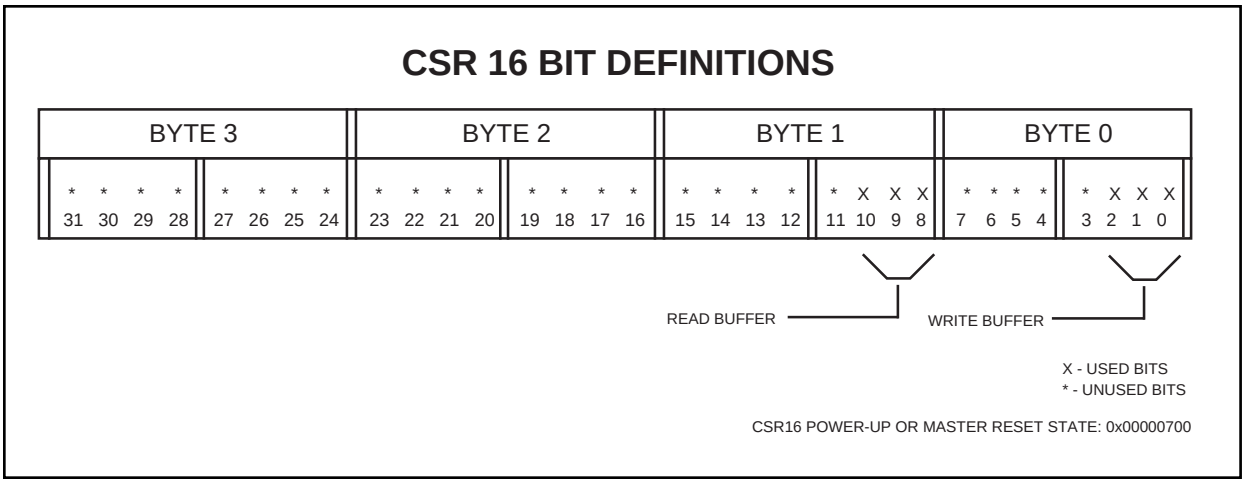

Figure 4: CSR 16 Bit Definition

Control and Status Register 18

CSR 18 controls the full scale time measurement of the MTD133B as well as the LIFO depth. Full scale can be programmed from 0 to 32.768 μsec in steps of 8 nsec.

MTD133B Full Scale Time Measurement: Bits 4 - 15 control the MTD133B time measurement full scale. Only time measurements below the programmed value will be registered in the MTD133B's internal LIFO.

MTD133B LIFO Depth Control: Bits 0 - 3 control the MTD133B's internal LIFO depth which may be set between 1 data word (measured time value) and 16 data words.

Note: *CSR18 must be programmed for 32.768 μsec if module is to be used in Common Start mode.*

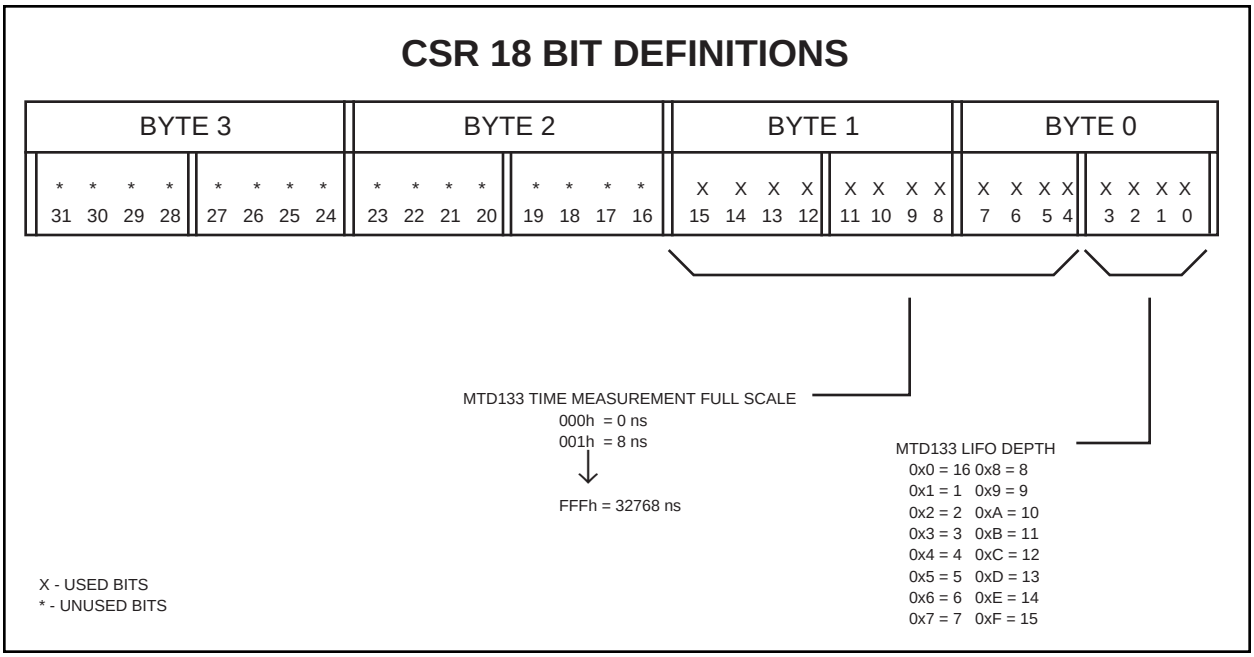

Figure 5: CSR 18 Bit Definition

FASTBUS OPERATIONS

FASTBUS Address Cycle

The 1877S TDC responds to geographical, logical and broadcast addressing.

Logical Addressing

CSR3<31:16 > contain the logical address to which the 1877S will respond in both CSR space and Data space.

Geographic Addressing

The Model 1877S responds to geographical addressing in both CSR space and data space.

Broadcast Addressing

The following is a list of Broadcast operations responded to by the 1877S. The case numbers are selected from Table 4.3.2 of the IEEE 960-1989 FASTBUS specification. Example address uses G=0 and L=1 for broadcasts on the local FASTBUS segment only.

Case 1: General Broadcast: 0x00000001. All devices respond to subsequent data cycles.

Case 2: Class N Broadcast: 0x000000N5. Only devices of class N respond to subsequent data cycles. CSR7<3:0 > controls the classes of class N broadcast to which the 1877S will respond in both Data and CSR spaces.

Case 3: Sparse Data Scan: 0x00000009: Devices respond by asserting T-Pin during following read cycle if data present.

Case 3a: Sparse Data Scan: 0x00000019. Devices respond by asserting T-Pin if they contain no data or are available for use.

Case 4: 0x0000000D. Devices respond by asserting T-Pin during following read cycle.

Case 8-C: 0x000000CD. Unique 1877 and 1877S Sparse Data Scan: 1877 and 1877S TDCs respond by asserting T-Pin during following read cycle if unsuppressed data is present in the next buffer.

Important Note: In some rare cases, the module will not be able to respond to a broadcast primary address cycle within the 500 nsec minimum Master/ANC Logic handshake time. In these circumstances, the module will assert the FASTBUS WAIT signal for the period of time required by the slave to properly decode the broadcast.

DATA SPACE

Data memory in the 1877S TDC is organized in a 16K word circular buffer with eight 2K word pages. Data resulting from an event is stored in one of the eight 2048 word buffers. Each event buffer contains enough addresses to hold the maximum data resulting from a single event (1537 words). An event is defined as the occurrence of a Common Start or Stop.

In the power-up or reset state, Memory Test Mode is disabled, and the 1877S data space consists (from the FASTBUS point of view) of only DSR0; writes to the Data Space NTA have no effect. CSR16 controls the buffer which is currently accessible to FASTBUS (read buffer) as well as

the buffer which will be used to store the next event readout of the MTD133B's (write buffer). At power-up or when a master reset is issued, the next event buffer to be read will be 7, and the next event buffer to be filled will be 0. Once an event occurs and is buffered the write buffer number is automatically incremented. CSR16 is a read-write register which can be used to control the position of the read and write buffers. Under normal operating circumstances, CSR16<10:8> is modified by the Load Next Event command and CSR16<2:0> is modified by the MTD133B readout circuitry. The user should, in general, not need to manipulate CSR16 directly except to re-read an event.

When Memory Test Mode is enabled, any location within the 16K data space is directly accessible via FASTBUS. At any particular time, there are 2048 (one complete buffer) secondary addresses (DSRs) available in data space. The buffer currently accessible can be modified by the Load Next Event command or by writing CSR16 directly.

CSR5<10:0> controls the number of words transferred in a block read. During normal data acquisition, a Load Next Event both advances the read buffer to the next event and loads CSR5<10:0> with the correct word count for the event contained in the next buffer. This can, of course, be done for an entire crate of 1877Ss at once using a broadcast command. The maximum number of words transferred is limited to one full buffer. Though CSR5 is always maintained in the 1877S, it is only visible to FASTBUS when Memory Test Mode is enabled.

When the read pointer is one less than the write pointer (modulo 8) the buffers are considered empty. When the read pointer and the write pointer are equal, the buffers are considered full. The condition "not empty" is used for the Sparse Data Scan. The condition "full" is used to extend Buffering in Progress (BIP) until the buffers are not full.

Header Word Format

The first word (zeroth address) of each buffer contains a header word for the event data which follows and is normally the first word readout during a block transfer. This header word contains the word count for that event as well as parity, phase, buffer number, and geographic or logical ad-

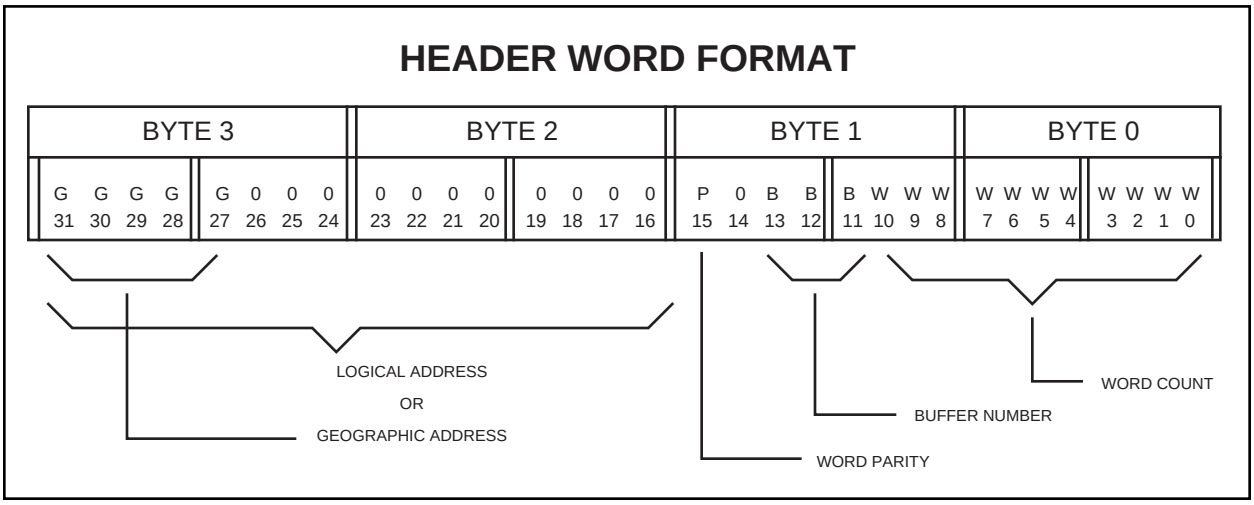

Figure 6: 1877S Header Word

dress of the module. The word count is automatically loaded into CSR5 when a Load Next Event command is issued. After each FASTBUS block transfer data cycle, the word count register is decremented. The parity bit is high or low so as to make the total number of bits in the header word even.

Data Word Format

The 1877S time data is read out as a 32 bit data word. The 16 least significant bits are the time data, the next bit is the hit phase (denoting rising or falling edge), and the next 7 bits are the channel identification. The most significant byte contains the geographic address, parity, and a hit count. The parity bit is set high or low to make the total number of bits in the word even.

The hit count indicates the number of edges received on that channel. This is presented in modulo 4 format, and reflects only edge polarities enabled in CSR1 (leading and/or trailing edges). This hit count value is independent of LIFO depth programming and has a maximum value of 3. The hit count is useful in identifying the range of interest when used with an MQT300 Multi-range Charge-to-Time Converter front end. For this application both leading and trailing edges must be enabled.

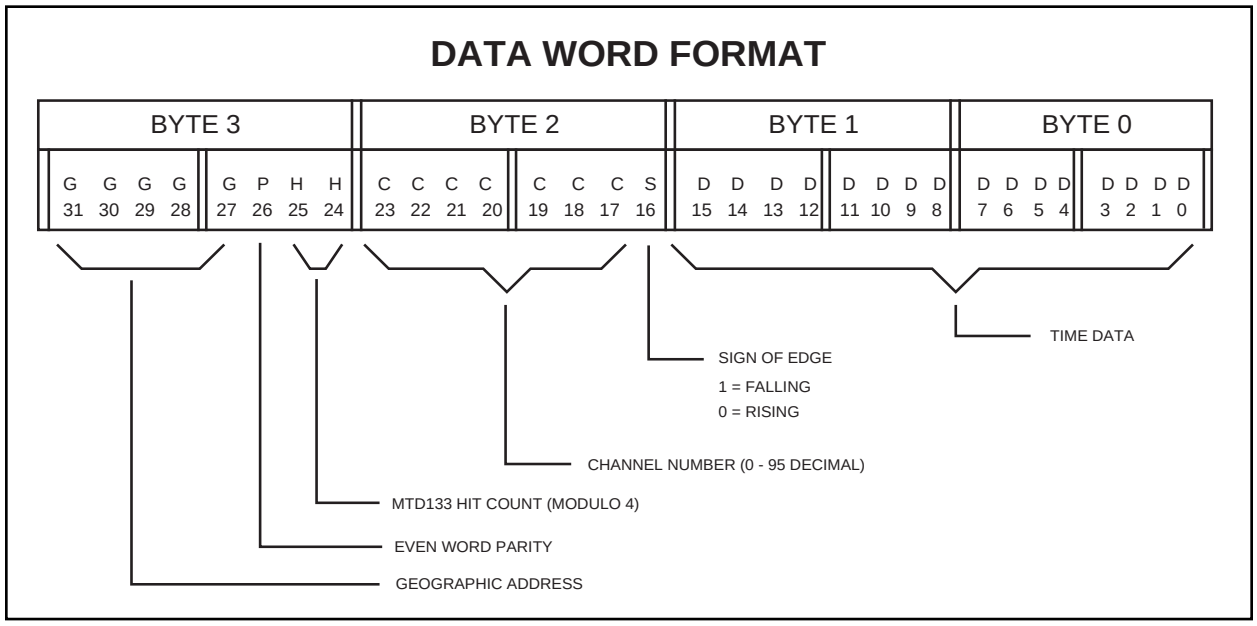

Figure 7: 1877S Data Word

READOUT

Single Read from Data Space

Reading of the data stored in the multi-event buffer can be done using random read cycles. However, first the correct number of words to read must be ascertained. Assuming Load Next Event has been used to select the desired event to read, the first location of this buffer, the header word, must be read to find out how many words are in the event. Bits <10:0> of the header word contain the word count for the event.

This word count is the number of data words plus 1 for the header word itself. With this information the correct number of words for the event can be read by repeated reads to DSR0.

Block Transfer Read from Data Space

Block transfers are the preferred way to read data from the 1877S, and this is facilitated by the Load Next Event function, CSR 0<10>. A write to CSR 0<10>, Load Next Event, increments the read pointer by 1 and loads CSR 5 with the word count for that event. This can of course be done for an entire crate at one time using a broadcast. A subsequent block read will transfer data until automatic decrementing of CSR 5 reaches 0, the end of the event's data. The header word for the event is the first word transferred. SS = 2 indicates the end of the block transfer.

FASTBUS WRITE TO DATA MEMORY

Although not pertinent to data acquisition, it is possible to write to the data memory via FASTBUS providing that Memory Test Mode has been enabled. This may be desired for testing. For this purpose, the data memory appears as a 16384 word x 32 bit RAM with the upper three bits of the address being CSR 16<10:8> and the lower 11 bits being the Data Space NTA. Data may be written into this RAM using random, or broadcast modes. Block writes to data space are not supported. Since the 1877S event manager is not managing this loading, however, the parity checking, channel identification, and geographic address identification normally present in the data are not present when read back.

TESTER

An on-board tester is provided for easy verification of the unit's functionality. When CSR0<7> is written with the internal tester enabled, a test cycle of square wave pulses is initiated. The number of pulses generated can be 1, 2, 4, or 8 as programmed by CSR1<17:16>. The width of the pulses is controlled by CSR1<19:18>. By enabling both rising and falling edge detection (CSR1<30:29> = 1), and setting the tester to 8 pulses, it is possible to generate 16 measurements on 96 channels.

Since the clock generating the test pulses is asynchronous to the acquisition clock, the tester pulse measurements will have a non-zero standard deviation, typically less than one count. This is, however, usually larger than that attainable using a high quality external source.

FAST CLEARS

A fast clear can be applied any time during the fast clear window. This will cause the event just recorded in the front end not to be buffered. The write pointer for the buffer will not be incremented. The buffering situation will be as though the cleared event never took place. This action requires 300 nsec from the rising edge of the fast clear pulse before the module is ready to accept another event. Fast clears can be applied either from the front panel input, by writing CSR0<31>, which can of course be done using a broadcast write, or via a model 1810 CAT (TR0). The application of a Fast Clear during the Fast Clear Window will terminate the Fast Clear Window.

ALLOCATION OF RESTRICTED USE LINES

Using CSR1, the 1877S can be enabled to accept Common, Fast Clear Window, and Fast Clear inputs on the TR lines. Four of these lines have been allocated to be compatible with the LeCroy Model 1810 Calibration

and Timing (1810 CAT) module facilitating distribution of these signals throughout a crate. The assignments are:

TR0 - Fast Clear

TR3 - Common (Start)

TR5 - Fast Clear Window

TR6 - Common (Stop)

The fifth line is incompatible with the LeCroy Model 1810 CAT:

TR7 - Buffering In Progress (BIP)

The Fast Clear Window corresponds to the 1810 CAT MPI signal, which can be either programmed internal to the 1810 or supplied via the 1810 front panel. The Common signal corresponds to the 1810 CAT input signal marked TDC Stop. The Test Pulse input corresponds to the 1810 CAT Test Pulse output.

When testing with the 1810 CAT it should be understood that the 1810 was designed for a Common Stop TDC, the LeCroy Model 1879. The pulse width of the signal output on TR3 and the delay of the signal output on TR6 can be programmed. The pulse width of the TR6 signal can not be programmed and is nominally 225 nsec. When using the 1877S in Common Stop mode, operation is straightforward. The signal on TR6 is used as the Common Stop and the signal on TR3 is used to generate test hits to the channel inputs of the 1877S.

With the 1877S set for Common Start mode, the signal from TR6 is used to generate test hits for the channels, and TR3 is used for the Common Start. This is because the 1810 CAT can not change the time ordering of the pulses output on TR3 and TR6; TR3 occurs before TR6. The user must take care in programming the 1810 CAT so that both edges of the TR6 pulse are detectable in Common Start mode. There is also a difference in propagation delays for the two signals on the 1877S of about 15 nsec. This results in a small discrepancy between the time programmed into the 1810 CAT DSR1 and what is actually measured in the 1877S. Pulse width measurements should still be accurate.

In both Common Start and Common Stop modes the signal from the 1810 CAT used to generate hits to the channels is always enabled. So if the 1810 CAT is used when acquiring real data in any way that might cause a test cycle, the test pulse from the 1810 CAT must be disabled. This is done in CSR1 of the 1810 CAT.

Additionally the BIP output signal from the 1877S can be enabled to TR7 so that all 1877S TDCs in a crate could be wire OR'ed to produce a crate wide BIP. This practice is, however, incompatible with the use of TR7 by the 1810 CAT. The 1810 uses TR7 to distribute a reference timing signal to 1879 TDC modules. If a 1810 CAT is in the crate, the 1877S CSR1<0> must be set to 0.

USER CSR SPACE - SPARSIFICATION MEMORY

The 1877S allows the user to program 96 (14-bit) constants, one per channel, which can be compared to measurement values during readout. The two MSBs bits of the programmed thresholds are internally set to zero. Only data exceeding the programmed threshold is buffered. The type of events to which sparsification can be applied must adhere to certain strict constraints. See "Sparse Data Readout".

The sparsification memory is accessed at User CSR Space, 0xC0000000 to 0xC000005F. Each memory location is 14 bits. Access to the user CSR space is only allowed if the Enable Commons bit (CSR0<2>) and Enable Sparsification bit (CSR1<20>) are disabled.

EXAMPLE CODE

```
/* The following are examples of some possible general purpose 1877S subroutines.  This code has been compiled
but never executed.  It is intended only to illustrate the methods.  */

/* Include these header files for C applications.  */
#include < stdlib.h >
/* Program Parameters */
#define ARRAY_SIZE 1537  /* 12 ics * 8 channels * 8 hits * 2 phases=1536 + 1 _____ */
#define NO_OF_CHAN 96
#define SLOT 0x00000000BL

/* FASTBUS Prototypes; Primitive FASTBUS Action Routines */
int fb_cycle_pa_csr(unsigned long slot);
int fb_cycle_pa_data(unsigned long slot);
int fb_cycle_write_word(unsigned long data);
int fb_cycle_read_block(int max_words, unsigned long data[ ]);
int fb_cycle_read_word(unsigned long * data);
int fb_read_length();

/* Prototypes */
void master_reset(unsigned long slot);
void setup(unsigned long slot);
unsigned long test_for_buffer();
void skip_event();
int read_event(unsigned long data[ ], unsigned long slot);
void sort_n_sum( long summed_data[ ]);

/* Routines */

/* The routine ‘master_reset’ clears the 1877S, all is set to the power up state except for the logical address (csr 3h)
and broadcast classes (csr 7h).  */

void master_reset( unsigned long slot )
{
      fb_cycle_pa_csr(slot);
      fb_cycle_write_word(0x40000000L);
      return;
}

/* The routine ‘setup’ selects a particular operating mode for the 1877S.  */

void setup( unsigned long slot)
{
      fb_cycle_pa_csr(slot);
```

```
/* Enable Common Hits (Presently Common Hits are always enabled and this bit has no effect) */

        fb_cycle_write_sa(0x00000000L);
        fb_cycle_write_word(0x00000004L);

/* Select Common Start, Rising Edge Detection, Falling Edge Detection,16 μsec Fast Clear window, and maximum
Common Start Timeout 32 μsec */

        fb_cycle_write_sa(0x00000001L);
        fb_cycle_write_word(0xe70000f0L);

        return;
}

/* The 'skip_event' routine advances the 1877S buffer pointers on all boards in the crate with a broadcast of the 'Load
Next Event' feature.  This bit in CSR 0h sets the NTA and word count register (csr 5h) to read the next event.  Note
the Data Space NTA must not be directly modified for this feature to work properly.  Also note that the Secondary
Address cycle to Control Space is not required as the 1877S resets the CSR NTA at disconnect */

void skip_event() {

        fb_cycle_pa_csr_multi(0x00000003L);  /* General Broadcast */
        fb_cycle_write_word(0x00000400L);   /* load next event  */
        fb_cycle_disconnect();
}

/* The 'read_event' routine advances the 1877S buffer pointers on all boards with the 'skip_event' defined above.
The word count for the block transfer is returned.  */

int read_event( unsigned long data[ ], unsigned long slot) {

        skip_event();

        fb_cycle_pa_data(slot);
        fb_cycle_read_block(ARRAY_SIZE, data);
        fb_cycle_disconnect();

        return(fb_read_length()/4);

}

/* The routine 'test_for_buffer' uses FASTBUS broadcasts to poll for full buffers in the 1877S.  This is a T-pin scan.  */

unsigned long test_for_buffer() {

        unsigned long i;
        fb_cycle_csr_multi(0x0000000BL);   /* Sparse Data Scan */
        fb_cycle_read_word(&i);
        fb_cycle_disconnect();

        return(i);
}

/* The procedure 'sort_n_sum' processes the data from one 1877S buffer.  It is assumed that the 1877S generates
exactly the same number of hits for every event and the sum for each hit is computed.  This routine would function for
the test modes of the 1877S to compute the mean of the test pulses.  */

int channel_number( unsigned long data )
        { return((data & 0x00FE0000) >> 17); }
```

```
int tdc_counts( unsigned long data)
      { return(data & 0x0000FFFF); }

void sort_n_sum( long summed_data[96][16],
      unsigned long *raw_data, int word_count)
{
int current_channel, current_edge, last_channel, i;

      i = current_edge = last_channel = 0;

/* Process all the words in the block */ for (i=0; i word_count; i++) {

/* Process only data words; Header words have channel = 127 */
   current_channel = channel_number(raw_data[i]);
   if ( (current_channel <= 95) && (current_channel >= 0) ) {

/* if the channel number has changed, reset edge counter */
   if(current_channel != last_channel) {
      current_edge = 0;
      last_channel = current_channel;
   }

/* update sums */
   summed_data[current_channel][current_edge] +=
      tdc_counts( raw_data[i]);
   current_edge++;
      }
   }
}

/* The main routine waits for external triggers and processes each event.  If the triggers observe the Buffer In
Progress (BIP) hold off signal, a buffer overrun is avoided.  */

void main()
{
long data[ARRAY_SIZE];
long summed_data[96][16];
int word_count;
      fb_cycle_disconnect();
      master_reset( SLOT );
      setup( SLOT );
      while ( 1 ) {
            while (test_for_buffer() == 0x0L) {}
            word_count = read_event( data, SLOT);
            sort_n_sum( summed_data, data,  word_count );
       }
      }
```

INSTALLATION

GENERAL

The LeCroy Model 1877S Time-to-Digital Converter is intended for use within a FASTBUS crate with the following voltage sources properly connected to the backplane: +5.0 V, -5.2 V, -2.0 V, +15.0 V, and -15.0 V. The crate should be an ECL implementation. If an Aux. card is to be used, e.g. for trigger outputs, the FASTBUS crate must include a 195 pin/ connector auxiliary backplane. Each crate must be controlled by a crate master such as a LeCroy Model 1821 SM/I. Its purpose is to execute standard FASTBUS cycles for control of the module and transfer of data. A processor interface of some sort is necessary to communicate with the crate. A LeCroy Model 1821/DEC interface card with either a DEC DR11-W Unibus or a MDB DRV11-2 Qbus parallel I/O board can be used with the DEC computer line. A less expensive way of getting started, useful for a small number of crates, is to use an IBM PC/AT or compatible with a LeCroy Model 1691B Interface Card. The 1691B plugs into a slot in the PC and it is connected via a 34 conductor multiwire cable to the front panel of an 1821 SM /I.

The software package LeCroy Interactive FASTBUS Tool kit (LIFT) is available for the LeCroy Model 1691B/IBM PC system providing the user with a substantial package of software to exercise and test FASTBUS modules using a LeCroy Model 1821 SM/I. LIFT also includes an extensive library which the user may employ in the development of user specific data acquisition software.

Either with the power on or off, the 1877S is inserted into one of the slots of the FASTBUS crate. The edge connector of the module should mate with the bus connector with modest pressure. Note the slot number of the module, as it will later be used for addressing.

CABLES

The use of twisted-pair cables generally results in lower cabling costs and typically higher density and is usually adequate for digital signals. Thus the 1877S was designed to accept 34 conductor ribbon cable. If using twisted-pairs, care should be taken to install high quality, shielded cables to minimize the effects of noise and crosstalk. Many of such cables can be purchased from LeCroy Research Systems. In particular, there are two types of 34 conductor multiwire cables available, one for short connections using flat cable and the second for long connections using twisted and flat ribbon cable.

The model numbers of such cables are as follows:

STC-DC /34/L - flat multiwire cable for short interconnections

LTC-DC /34-L or DC2 /34-L - twisted-pair multiwire cable for long interconnection.

STP-DC /02-L - single twisted-pair cable, 3 ft maximum length

Note: *L is the length in feet that must be specified by the user.*

All inputs are differential ECL and terminated by 112 ohms. The terminations are SIP components and may be easily replaced to accommodate other characteristic impedances.

GENERAL DESCRIPTION OF BUFFER ARCHITECTURE

The buffer memory on the 1877S is a 16K word SRAM structure with a word width of 32 bits. The memory is constructed out of eight 8K x 8, 12 nsec SRAM. Access to the buffer memory from the module's front end (i.e. MTD readout) and from FASTBUS is completely interleaved, resulting in a synchronous dual-ported memory.

Readout of events from the MTDs into the buffer memory can occur at a maximum rate of 20 MHz while readout of the buffer memory to FASTBUS via Block transfers can proceed at a rate up to 10 MHz. It is important to note that front end/FASTBUS access to the memory is synchronous and interleaved 2:1. This means that the maximum transfer rate to FASTBUS will always be exactly half of the front-end readout rate which is itself half of the 40 MHz system timebase. Additionally, since the FASTBUS interfacing circuits are operating from the same clock as the memory control circuits, DK and AK response times are also a function of the 40 MHz timebase.

Figure 8 shows a simplified block diagram of the 1877S data paths. Event data is readout of the MTDs through a pipeline at 20 MHz into the buffer memory. Sparsification of the data (if enabled) is performed as the data is pipelined into the buffer memory. Events are readout to FASTBUS through a two stage pipeline at speeds up to 10 MHz, depending on the Master. The FASTBUS readout pipeline stages are required to maintain the maximum transfer rate to the asynchronous FASTBUS. The addresses for front-end and FASTBUS access are multiplexed at a rate of 40 MHz.

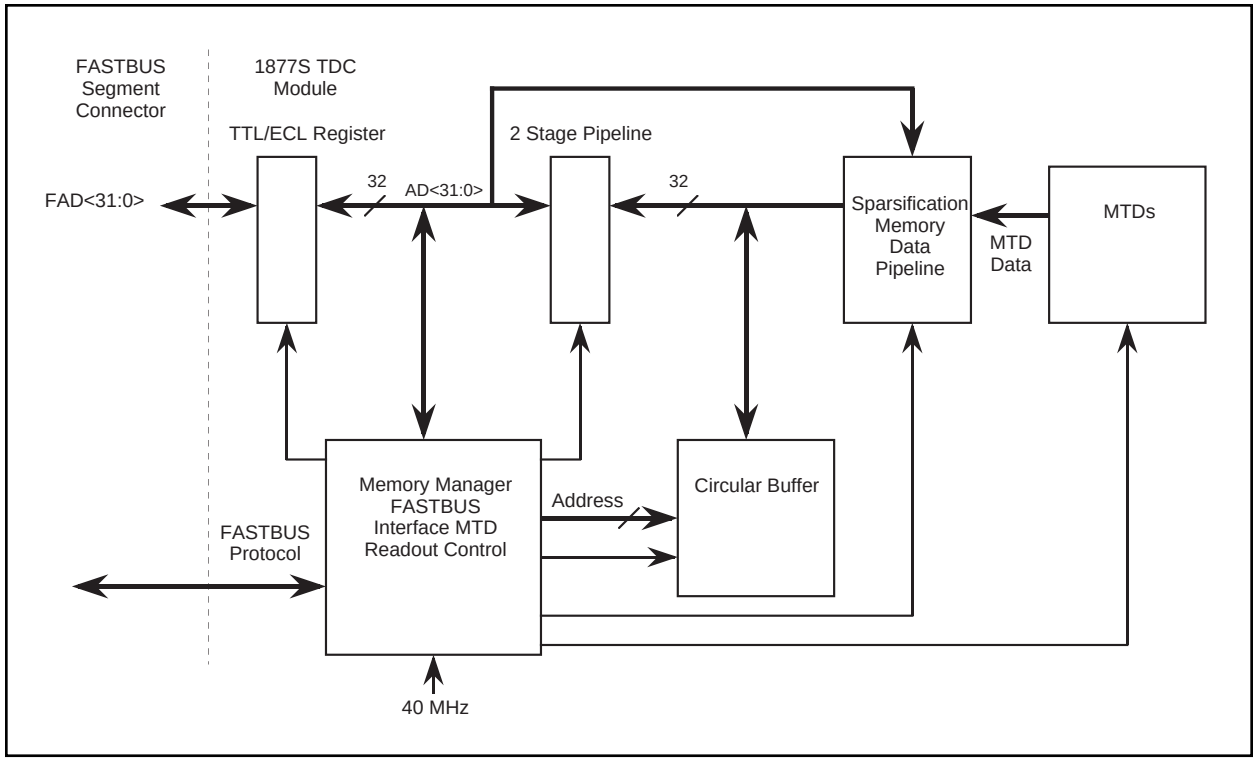

Figure 8: Simplified 1877S Interface/Buffer Block Diagram

Multi-Event Buffer Memory Organization

The 16K memory is logically partitioned into pages, each representing a separate event buffer. For the 1877S, there are eight 2K pages or buffers. Since there are a maximum of 1536 + 1 data words per event, each page of memory can hold one complete event.

Buffer Memory Pointers

The eight individual buffers are logically organized as a circular buffer structure. Two pointers are maintained into the circular buffer memory - MTD Write Pointer (MWP) and FASTBUS Read Pointer (FRP). Each pointer is really made up of two separate pointers: a buffer pointer - Read Buffer (RB) and Write Buffer (WB) - and an address pointer within that page - Read Page Address (RPA) and Write Page Address (WPA). See Figure 9. How the buffer pointers are controlled depends on the operational mode of the module.

FASTBUS Read Pointer (FRP): The Read Buffer (RB) can be manipulated directly by writing to CSR 16. RB may also be effected through the use of the Load Next Event (LNE) command which prepares the module for FASTBUS readout. A LNE command would have the effect of incrementing RB so that the FRP is advanced to the next buffer in the circular structure. In the default mode of the module, the Read Page Address (RPA) is not accessible to the user. In Memory Test Mode, however, the RPA becomes the Data Space Next Transfer Address and may also serve as a write pointer to Data Space. See "Memory Test Mode" for discussion.

MTD Write Pointer (MWP): The Write Buffer (WB) can be manipulated directly by the user by writing to CSR 16. Otherwise, WB is maintained by the front-end MTD readout circuits. The Write Page Address (WPA) is maintained solely by the front-end MTD readout circuits and is not accessible to the user in any way.

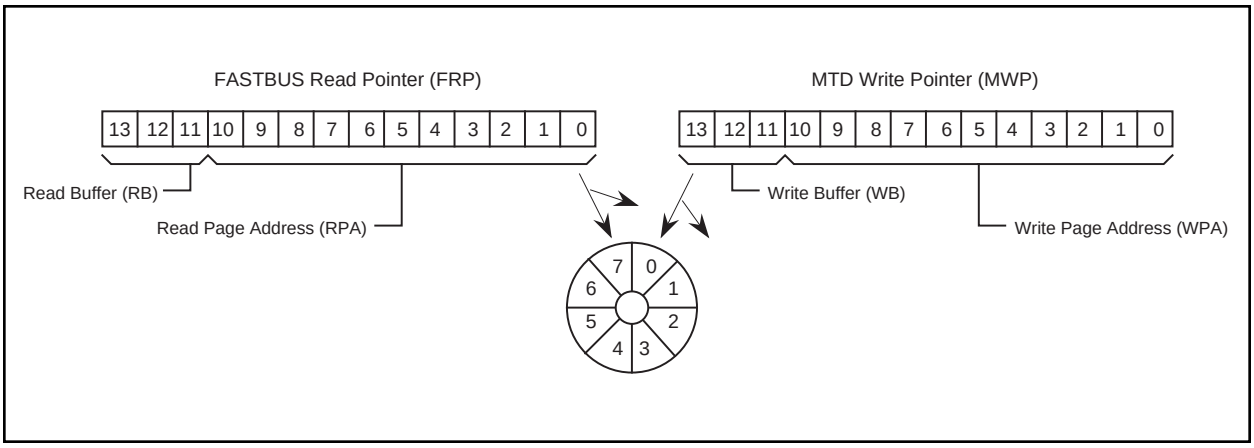

Figure 9: 1877S Circular Buffer

Buffer Full/ Empty Conditions

Upon power up of the module, or Master Reset via FASTBUS command, the MTD Write Pointer is pointing to the beginning of buffer zero and the FASTBUS Read Pointer is pointing to the beginning of buffer seven. See Figure 8. This relative positioning of the pointers, that is, the read pointer one buffer behind the write pointer, defines the Empty Condition. Conversely, the Full Condition is defined as the case where the write pointer is one buffer behind the read pointer. The Full and Empty conditions as described apply before a LNE is issued: i.e. if a single event is in the buffer and a LNE is issued, the Empty condition would be true even though an event is now ready for readout.

As events are readout of the MTDs into the circular buffer, the WB is incremented to point to the next available buffer. Similarly, as events are prepared for readout via FASTBUS using the Load Next Event (LNE) command, RB is incremented to point to the next event which will be read out of the circular buffer. For example, after one event has been completely buffered (after power-up or reset) WB would be at buffer one and WPA would be zero. RB would be at buffer seven and RPA would be zero. A subsequent Load Next Event would prepare the module for FASTBUS readout of that event by incrementing RB to buffer zero. See "Load Next Event" for further discussion.

ACQUISITION AND BUFFERING

Readout of MTDs

Readout of event time data from the MTDs begins either upon receipt of a common hit (in common stop mode) or at the end of the common start timeout period (in common start mode). During the time that the module is buffering event data, the signal Buffering In Progress (BIP) is asserted. Data words are written into the buffer currently pointed to by WB starting at the location pointed to by WPA. If the module receives a Fast Clear during its programmed Fast Clear Window, the event just buffered (or being buffered) is discarded - WB is not incremented and WPA is cleared.

Organization of Data in Events

As data words are written to memory, the WPA is incremented until all data words have been readout of the MTDs. BIP is then deasserted and a header word (which is the complete buffer address of the last data word) is written into Write Page Address zero, the first memory location of the page. In this manner, all events, once completely buffered, consist of a header word in the first memory location of a given buffer (page) followed by the data words for that event. Further, since the header word contains the absolute memory location one beyond the last data word for that event, it reflects both the buffer number (within the circular buffer structure) and the complete word count for that event including the header word itself. If an event occurs which has no data words - a null event - a header word with a word count of one is still written and the MTD Write Pointer is advanced to the beginning of the next buffer.

FASTBUS ACCESS TO MODULE

Control and Status Registers

Several Control and Status Registers (CSRs) control the configuration and operation of the 1877S. The following is a list of the CSRs contained in the 1877S and a brief description of their function(s):

CSR0, CSR1 - Primary control and configuration registers. These registers contain the configuration bits for all operational modes of the 1877S. Additionally, CSR0 contains pulsed bits which initiate operations specific to the module such as Master Reset, Load Next Event, internal test cycles, etc.

CSR3 - Logical Address.

CSR5 - Block transfer word count register. CSR5 controls the number of words which will be transferred during a block transfer. A SS=2 response is generated by the module when CSR5 has decremented to zero during a block transfer. This register is read/write and may be loaded with an arbitrary value up to 7FFh (one full buffer). CSR5 is loaded automatically with the word count for the next event when the module is prepared for readout of an event using a LNE command.

CSR7 - Controls Class-N broadcast response.

CSR16 - Buffer Status register. CSR16 contains the Read Buffer (RB) and Write Buffer (WB) of the FASTBUS Read Pointer and the MTD Write Pointer, respectively. This register, therefore, indicates to which buffer, in the circular buffer structure, each of the pointers is pointing. CSR16 is read/write and can be used to directly manipulate the positions of the read and write pointers within the circular buffer. In the 1876/1881, CSR16 is read-only and cannot be used to directly control the positions of the pointers.

CSR18 - MTD133B configuration register. CSR18 holds the full scale time measurement and internal MTD LIFO depth.

Secondary Addressing in Data Space

Data is readout of the module via FASTBUS by first accessing the module through a primary address cycle to Data Space and then performing subsequent read data cycles. In the default operational mode, secondary addressing in Data Space is not relevant. A second operational mode, Memory Test Mode, is provided which supports secondary addresses in Data Space and allows direct access to any buffer memory location within the 16K Data Space.

Default Addressing Mode

The default addressing mode, which does not support secondary addressing in Data Space, is primarily useful if the FASTBUS readout method is a block transfer. In this mode, writes to the Data Space NTA is acknowledged but ignored. There is, in effect, only one location in Data Space, DSR0.

For block transfers in this mode, each individual buffer appears similar to a FIFO. For example, assume that the module has been prepared for readout (i.e. a Load Next Event command had been previously issued.). The first data word transferred during a block read is the event header

word. This header contains the geographic (or logical) address, parity, and the absolute address (in the 16K word circular buffer memory) of the last valid data word of the event being readout. The absolute address contains the buffer number, RB (also available in CSR16) and the word count including the header word, RPA for the last data word written to memory. Subsequent transfers produce the event data words in a similar manner to a FIFO until all valid data words in the event have been transferred and the module generates SS=2.

The RPA is incremented after each read to point the next word in the buffer during the block transfer. Random reads from Data Space must be used with care since the location of RPA (not visible to FASTBUS) is not known except under very specific circumstances. Random reads will increment the RPA and thus can be used to readout the module in a way similar to a FIFO however no indication will be given when the last valid data word has been readout. The number of words to readout by this method must be ascertained from the header word.

In the default readout mode, re-reads of a particular buffer are not directly supported since it is difficult to be certain, after the event has been initially readout via block transfer, what the value of RPA is. Re-read of a buffer may be accomplished indirectly by manipulating RB via CSR16 and issuing a Load Next Event command. See "Mechanisms for FASTBUS Readout".

Memory Test Mode (MTM)

Memory Test Mode (MTM) is an operational mode selectable via CSR0 which supports secondary addressing in Data Space. In this mode, the RPA portion of the FASTBUS Read Pointer is accessible as the Data Space Next Transfer Address (NTA). Additionally, CSR5, the block transfer word count register, is accessible to FASTBUS as an 11 bit read/write register.

In MTM, the 1877S buffers must be thought of as a paged memory, or circular buffer scheme; not as a FIFO. Random read or write data cycles may operate on any location addressable by the current RPA. By manipulating RB (via CSR16) and NTA, any location in the 16K Data Space can be addressed for reads or writes. This mode facilitates memory testing but may also serve as a very useful operating mode, depending on the specific user application. As per the FASTBUS specification, RPA and therefore NTA is only incremented during block reads. Block writes are not supported in the 1877S.

Block transfers are controlled in exactly the same way as with the default mode except that RPA is now accessible as the Data Space NTA and may be set by the user. In all cases, CSR5 controls the number of words transferred during a block transfer and RPA controls the address within the buffer where the transfer will begin. RPA (and therefore NTA) is incremented with each word transferred during a block transfer. If CSR5 > (2048 - RPA), then RPA will wrap around back to the beginning of the page.

In contrast to MTM in the 1876, the 1877S NTA appears as only 11 bits so there is no need for the user to keep track of the Read Page to avoid accidentally changing the page to which the FASTBUS Read Pointer is pointing. This allows existing user software that always writes the sec-

ondary address before beginning a transfer to operate without modification.

Though not recommended, it is possible to operate the module in Memory Test Mode with Priming on LNE enabled. The user must be aware that the priming operation causes the RPA to be incremented and CSR5 to be decremented as the pipeline is filled. When in MTM, the RPA is visible to FASTBUS as the Data Space NTA and is affected in a way not compliant with the FASTBUS specification.

MECHANISMS FOR FASTBUS READOUT

To avoid possible corruption of an event that has not yet been readout, only seven consecutive events may be buffered before the circular buffer becomes FULL. When this condition exists, the MTD Read Pointer must be advanced, either by issuing an LNE or manipulating CSR16 before additional events can be buffered. Several broadcast operations are implemented to monitor the 1877S buffering status.

Sparse Data Scan (case 3, code 0x09): Assert T pin on following read cycle if one or more events are buffered and available for readout.

Device Available Scan (case 3a, code 0x19): Assert T pin on following read cycle if the circular buffer is Empty.

1877S Unique Sparse Data Scan (case 8-c, code 0xCD): Assert T pin if CSR5 = 1. This scan only has meaning after a Load Next Event command has been executed. It is used to determine if the event just loaded has unsuppressed data words. Note: all buffered events will have at least a header word. Also, although CSR5 is only accessible to FASTBUS in Memory Test Mode, it is always maintained internally to control the number of words transferred during a block transfer.

Load Next Event

The Load Next Event (LNE) command is provided to prepare the module for readout after one or more events has been completely buffered. Assuming there is at least one event in the buffer, a LNE command advances the Read Buffer (RB) to the next buffer (the buffer to be readout), clears the Read Page Address (RPA), and copies the word count found in the header (of the event to be readout) to CSR5. A LNE issued when no events are available to readout is ignored since this would result in either an old event being loaded or CSR5 loaded with a meaningless value.

In order to reduce the time required by the module to begin a block transfer, LNE can also prime the two stage readout pipeline - see Figure 8. The priming during LNE is enabled by setting bit CSR0<8>. In the module's default data space addressing mode, this action is transparent to the user. In MTM however, the result of this action is to increment the data space NTA twice prior to the first data transfer. Priming of the readout pipeline does not prevent access to any of the 1877S's internal registers.

Block Transfers from Data Space

The normal method of reading event data out of the buffer memory is FASTBUS Block Transfer. In the default data space addressing mode of the unit, block transfers (in combination with the Load Next Event command) is the recommended method to access event data.

In all cases, FASTBUS block reads are controlled by CSR5 and the Read Page Address (RPA). RPA may or may not be visible to the user as the Data Space NTA depending on the operational mode of the module. Also, CSR5 is only visible to FASTBUS when in MTM. CSR5 is decremented with each block read transfer until CSR5 = 0, resulting in SS = 2.

A typical implementation for a crate full of TDCs might be as follows:

1. Determine if data is available for readout. This determination would be made based on either Sparse Data Scans or trigger information.

2. Issue a broadcast LNE to prepare all TDCs in the crate for readout. If readout of a particular event is not required, additional LNE's can be issued to effectively skip an event in the buffer (providing additional events are available to readout).

3. Address each module in data space and perform a block read.

Re-reads of a particular buffer are possible but not directly supported. In order to re-read a buffer when not in MTM, the Read Page (RP) must be set to the buffer preceding the buffer to be re-loaded by writing to CSR16. A LNE must then be issued to reload CSR5 and reset the Read Page Address (RPA).

In Memory Test Mode, the user has complete control over the data space NTA as well as the block transfer word count (CSR5) and Read Page pointer (CSR16). Re-reads can be accomplished as with non-MTM. Additionally, the user can re-read any buffer by setting RP to the buffer to be read, fetching the word count for that event from the first location in that buffer (using a random read from Data Space), and loading CSR5 directly with the block transfer word count.

Multi-Module Data Transfers (Multi-Block)

The 1877S fully supports the Multi-Module Data Transfer (MDT-1) specification. The modules participating on the Multi-Block scan must be in adjacent slots with the left most module (highest slot number) programmed as the Primary Link and the right most (lowest slot number) programmed as the End Link. The modules between the Primary and End (if any) must be programmed as either Bypass (default) or Middle Links. It is permissible for non-participating modules to be within the Multi-Block array as long as their FASTBUS daisy chain lines are appropriately connected to pass the Multi-Block token through.

Assuming a group on 1877S modules has been configured for a MDT scan as per the specification, it must first be established that all modules involved in the scan have data available. This could be done, for example, through a broadcast LNE. The scan is initiated by addressing the primary link and beginning a FASTBUS block read. The scan proceeds with each module participating, in turn, in the block read until the end link completes its transfer and issues SS=2.

It is important to realize that if all data words in an event are suppressed (a null event), a header word is still written into the buffer for that event. Thus, a module participating in a Multi-Block scan which has a null event

loaded for readout will still transfer the header word during its portion of the transfer.

MULTI-RANGING ADC COMPATIBILITY

The 1877S is designed to provide the necessary interface and readout features to provide compatibility with single and multi-range Charge-to-Time converting front ends. The 1877S provides the time encoding function of the charge-to-time converter output pulse as well as all FASTBUS readout and interface functions. In general, charge-to-time converters such as the LeCroy MQT300 always generate an output pulse, even at pedestal. This guarantees that non-zero time data is recorded by the 1877S on every channel.

Configuration Considerations

When the 1877S is used in a multi-ranging ADC application (e.g. LeCroy MQT300), the TDC is programmed to operate in Common Start mode. The common start timeout is used to set the full scale rundown time of the front end charge-to-time conversion. Either the 1877S's internal programmed Common Start Timeout or front panel TIME input may be used as appropriate.

A two-bit hit count field has been provided in the 1877S data word format. This field indicates (modulo 4) how many edges were registered in the MTD133B's LIFO. By programming the MTD133B LIFO depth to one (via CSR12h), it is possible to readout only one word from each channel while also knowing the total number of hits that channel received. This feature provides a second level of data reduction from the multi-ranging MQT300.

Since it is critical to know how many edges were registered during the common start event, care must be taken in the application of the common start timeout. In Common Start Mode, the MTD133Bs are returned to acquisition mode after buffering is completed. Once the TDC is in acquisition, the MTD133B's internal hit counter will be incremented on every transition on its channel inputs independent of the Common input. This means that edges arriving before the Common Start will increment the hit count and potentially result in misinterpretation of the range information. It is therefore strongly recommended that the front panel TIME input is used to control the common start event. The front panel TIME input is both edge and level sensitive; buffering of the event begins on the rising edge of the TIME input and the MTD133B's LIFO and hit counter are held in reset while the front panel input is asserted. This allows the user to control when the TDC will begin registering hits after the current event has been buffered. The MTD133B hit counter and LIFO are always cleared at the end of buffering so edges received during buffering will have no effect.

Sparse Data Readout

In a mode similar to the LeCroy FASTBUS ADC 1881M, a sparse data readout scheme can be used to prevent unwanted data from being buffered. The 1877S allows the user to program 96 constants (14 bits each), one per channel, which can be compared to the measurement values. Only data exceeding (value > threshold) these individual thresholds is buffered, reducing both dead time and the quantity of data that must be transferred over FASTBUS to the host computer.

There are two cases:

1. If bit 9 of CSR0 is cleared, the sparsification threshold is only applied to channels that had a hit pattern corresponding to the low range of the multi-ranging MQT300. This criterium for activating the sparsification is a number of transitions multiple of 4, the last transition containing the charge information for the low range.

2. If bit 9 of CSR0 is set (simple sparsification), all hits of all channels are compared to their respective thresholds, and all hits smaller than or equal to the threshold are removed.

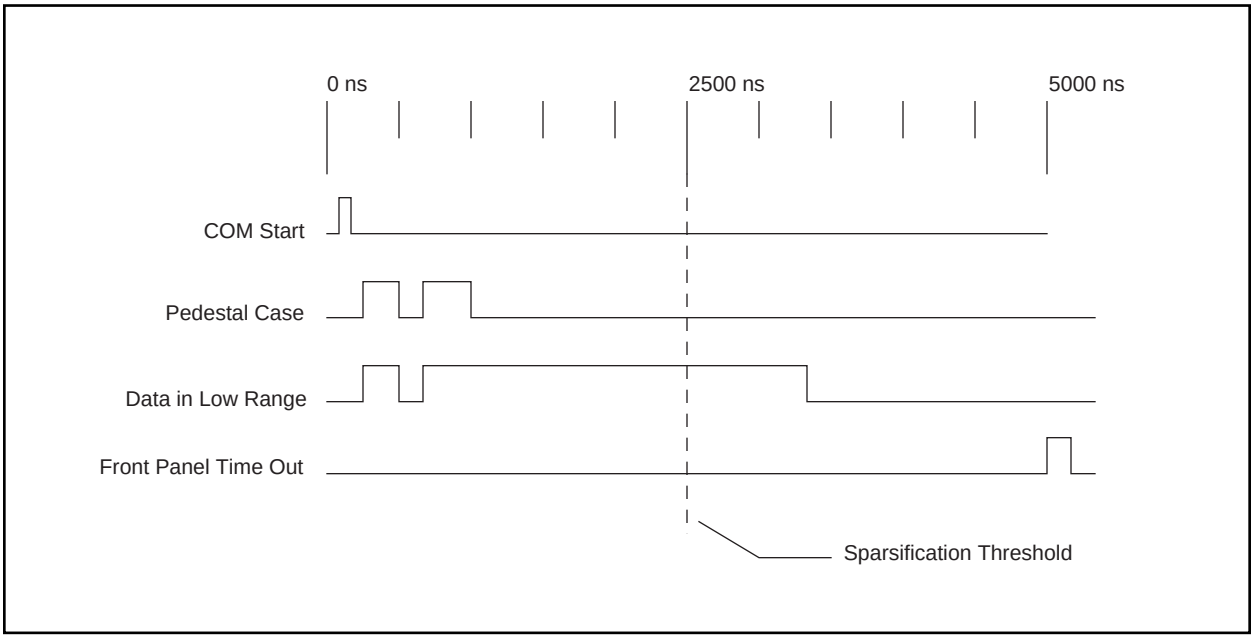

Figure 10 Example: MQT300 Low Range Data

INDEX

Symbols

1691B 29
1810 CAT 25
1810 CAT MPI 25
1821 SM /I 29
1821/DEC Interface Card 29
34 Pin Connectors 12
8 Position Connector 13

A

Acquisition Mode 14

B

BIP 13, 25
Block Transfer 24
Block Transfers 31, 36
Broadcast Operations 21
Buffer Memory 31
Buffer Memory Pointers 32
  FASTBUS Read Pointer (FRP) 32
  MTD Write Pointer (MWP) 32
Buffer Re-reads 37
Buffering In Progress 33
Buffering in Progress 13, 22

C

Cables 29
  Flat Multiwire 29
  Single Twisted-pair 29
  Twisted-pair Multiwire 29
Class N Broadcast 14, 21
Common 25
Common Hit 12
Common Start 11, 12, 13, 25
Common Start Timeout 13, 14
Common Stop 11, 12
Control and Status Register 14, 34
Customer Service Department 9

D

Daisy Chain 14
Differential ECL 11, 13
DSR0 24

E

Empty Conditions 33

F

Fast Clear 24
Fast Clear Window 13, 24
  FCW 11
FIFO 34
Front Panel Displays 12
  Common Hit LED 12
  Slave Addressed LED 12
Front-panel Inputs 12
  CLR 13
  COM 13
  IN 13
  TIME 13
Front-panel Output 13
  BIP 13
Full Condition 33

I

Internal Tester 12

L

LIFT 29
LNE 36
Load Next Event 32, 36

M

Maintenance Agreements 9
Manufacturer’s Identification 14
Master Reset 19
MDT-1 37
Memory Test Mode 35
Memory Test Mode Enable 16
MQT300 8, 11, 16, 23, 38, 39
MTD133B 11
MTM 35
Multi-Block 37
  Bypass 37
  Middle Link 37
  End Link 37
  Primary Link 37
Multi-Event Buffer 32

O

On-board Tester 24

P

Priming During LNE 36

R

Restricted Use Lines 24
  TR0 25
  TR3 25
  TR4 25
  TR5 25
  TR6 25
  TR7 25

S

Secondary Addressing 34
Service Procedure 10
Software Licensing Agreement 10
Sparse Data Scan 21, 36
Sparse Data Readout 38
Synchronous Dual-ported memory 31

T

Test Pulse 24

U

Unique Sparse Data Scan 36

W

Warranty 9