0954 Precision Interval Gate Generator (PIGG)

The PIGG is a double width CAMAC module that will generate a precision gate signal. The module obtains its timing reference from a precision 10 MHz crystal oscillator module. The oscillator output is processed by a programmable prescaler to provide a 1us to 1 sec clock to the 24 bit gate generator counter. A start command from CAMAC or from a front panel NIM input will load a preset value into the counter, start it, and set the gate output "active". The counter counts down, and when it reaches zero, will stop and set the gate output "inactive", and will generate a LAM if enabled. The counter preset value can be written by CAMAC. Writing a new value to the preset register while the gate is active will have no effect on the current timing cycle. A timing cycle can be stopped at any time from CAMAC or from a front panel NIM input.

The gate counter can be read using F(0)A(1). The module will return Q = 1 for this function only while the gate is active.

If bit 4 of the configuration word is clear (0), a start command received while the gate is active will have no effect. If this bit is set (1), a start command received while the gate is open will re-load the Preset Register value into the Gate counter, and restart the timer.

If bit 5 of the configuration word is clear (0), a LAM will be generated only on a time-out, and not on a manual (front panel or CAMAC) stop. If this bit is set (1), a LAM will be generated when the gate is closed/counter stopped for any reason.

The leading and trailing edges of the generated gate signal will be synchronized to an internal 1 MHz clock derived from the 10 MHz master oscillator.

The module also contains a 48 bit continuously-running counter driven from a 1 MHz source derived from the precision oscillator. Both words of this counter are latched during a CAMAC read of the high word and will remain latched until the low word is read, so the value read will not change until both words are read. If the low word is read first, the high word will not be latched. The counter will continue to run undisturbed at all times.

CAMAC F ‘n A codes

Command	Q	Action
F(00)•A(00)	1	Read Gate Generator Preset Register
F(00)•A(01)	Gate	Read Gate Generator Counter
F(00)•A(02)	1	Read Status Register (including prescaler setting)
F(01)•A(00)	1	Read Low Word of 48 bit Counter
F(01)•A(01)	1	Read High Word of 48 bit counter (and latch low word)
F(01)•A(15)	1	Read Module ID (0954)
F(07)•A(15)	1	Read Module ID (0954)
F(08)•A(00)	LR	Test LAM
F(09)•A(00)	1	Reset Module
F(10)•A(00)	1	Clear LAM
F(12)•A(00)	1	Clear 48 Bit Counter
F(16)•A(00)	1	Write Counter Preset Register
F(16)•A(02)	1	Write Prescaler Setting
F(24)•A(00)	1	Disable LAM
F(25)•A(00)	(note)	Start Gate
F(26)•A(00)	1	Enable LAM
F(27)•A(00)	1	Stop/Close Gate

Note: If the module is set for non-retriggerable operation, F25 will return no Q if the gate is active, indicating the start command was ignored. In retriggerable mode, F25 will always return Q = 1.

Ins and Outs

The front panel has the following LED indicators:

N	Lit following a CAMAC cycle (driven by a 100 ms one-shot)
LAM	Lit if a LAM request is active
Gate	Lit while the Gate output is active
Running	Flashes once per second while the Gate is active.

There is a 1 MHz NIM level output, and another output of the pulse rate selected by the prescaler.

The Start and Stop inputs require negative-going NIM pulses.

There are four connectors for the Gate output, providing both True and Inverted NIM and TTL level signals.

All input and output connectors are Size 00 Lemo.

Status Register

The lowest three bits of the status register contain the prescaler control bits.
The prescaler sets the clock interval for the gate counter. The available settings are:

Bits 3..1
000 1 usec (1 MHz)
001 10 usec (100 KHz)
010 100 us (10 KHz)
011 1 ms (1 KHz)
100 10 ms (100 Hz)
101 100 ms (10 Hz)
110 1 second (1 Hz)
111 0.1 usec (10 MHz)

Bit 4 = 0: Non-retriggerable (start ignored while gate active)
1: Retriggerable mode (re-start any time)

Bit 5 = 0: LAM generated only on time-out
1: LAM generated when gate ends for any reason

Bit 9 = 1 when the Gate Output is active
Bit 10 = 1 when there is a LAM request
Bit 11 is bit 25 of the 48 bit counter (effectively, overflow of the low word.)

Known Bugs

1. When using the 1uS clock, the gate time will be 1 uS longer than programmed. When using the 0.1 uS clock, the gate time is unpredictable. As these clock settings are intended for debugging only, these faults will (probably) not be fixed.

2. In non-retrigger mode, if the gate is stopped before timeout, further start commands are generally ignored. Retrigger mode works fine. Research will continue regarding the non-retrigger mode fault.