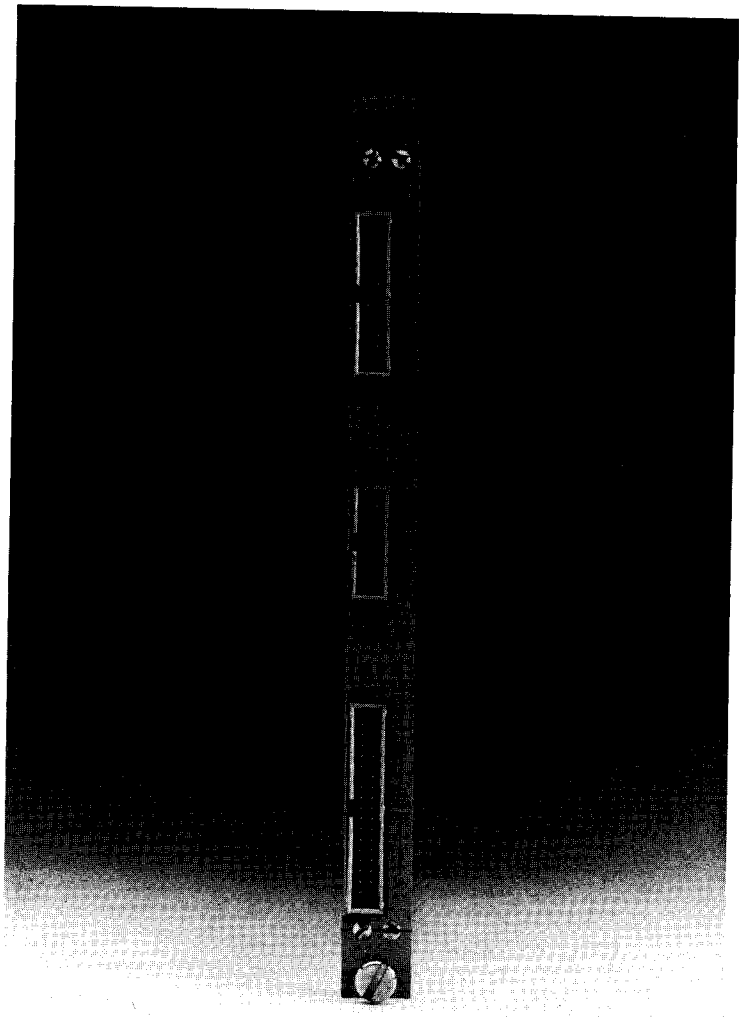
SILENA CAMAC
MOD. 4418/V



SILENA CAMAC MODEL 4418/V ADC
for Pulse Amplitude Analysis

- 8 INPUT CHANNELS in a single-width CAMAC module
- PULSE PEAK MEASUREMENT of gated-selected signals
- SPECTROSCOPY GRADE PERFORMANCE:
  - High resolution
  - Wide dynamic range
  - High linearity, both integral and differential
  - Low temperature coefficient
  - High long-term stability
- Fast conversion:
  4 μsec for every valid input channel
- Lower and upper threshold control through CAMAC (8-bit)
- Offset control through CAMAC (8-bit)
- Common threshold for noise rejection through CAMAC (8-bit)
- Programmable zero suppression
- Header and Pattern word available
- Sequential or random access CAMAC readout
- Data memory
- ECL readout logic – System compatibility with Le Croy FERA (*) (Fast Encoding and Readout ADC) modules
- System compatibility with CES modules
- Common test feature

(*) FERA is a trademark of Le Croy Corp.

DESCRIPTION

The SILENA Mod. 4418/V combines, in a single CAMAC module, a high resolution analog-to-digital converter with 8 input channels to perform simultaneous data acquisition and pulse amplitude analysis.
The Mod. 4418/V is a highly stable module offering superior integral and differential linearity performance, combined with fast conversion capabilities.

It features a conversion time of 4 μS for each valid channel.
The Mod. 4418/V represents a significant advance in data acquisition from multiple inputs. It has been designed for use in a variety of experimental situations employing many ADC's to perform high resolution, high stability pulse amplitude analysis.

The Mod. 4418/V uses the most advanced surface-mounting techniques to offer a previously unattained combination of operational features and specifications in a highly compact module.
In this pulse amplitude acquisition module, the 8 input channels acquire the peak voltage of the input signals which occur within the time interval marked by a common gate command. The circuit accepts all the typical pulse shapes of nuclear electronic modules, such as spectroscopy amplifiers, time-to-amplitude converters, etc.: RC-RC shaped pulses, semi-gaussian pulses, approximately square pulses.
The overall performance (wide dynamic range, high linearity, etc.) of the input channels and ADC makes the module suitable for high resolution spectroscopy.

SPECIFICATIONS

- *Analog Inputs:* 8
- *Connector:*
  8x2-pin front panel connector (ANSLEY 609-1607)
  The 8 pins of the left row are positive signal inputs; the 8 pins of the right row are ground returns.
- *Input Sensing:*
  Peak voltage
- *Range:*
  100mV to 10V
- *Coupling:*
  D.C.
- *Impedance:*
  1 KΩ; other values available on request
- *Signal Polarity:*
  Positive
- *Signal Shape:*
  All typical shapes from nuclear electronic modules, such as semi gaussian, RC-RC shaped, quasi rectangular are accepted, provided that the pulse peaking time Tpk (defined as the time from the onset of the pulse to the point where the pulse reaches its maximum height) is within the range. 8 μsec ⩾ Tpk ⩾1 μsec.
- *Selection of Acceptable Analog Inputs:*
  By means of the common threshold level for all channels for noise rejection under CAMAC control with 8-bit resolution (0 ÷ 1 Volt) and separate lower and upper level discriminators for each channel under CAMAC control with 8-bit resolution (LLD from 0 to 10%, ULD from 100% to 85%).
- *Resolution:*
  3840 channels (4096 minus 256 channels for sliding scale) corresponding to 2.5 mV/channel.
- *Conversion Time:*
  3 μS for every valid input channel.
- *System Busy Time with "Zero Suppression":*
  Variable as a function of the number of valid channels.
  Valid Channel:
  4 μS
  Channel without Signal-In:
  0.23 μS.
  Channel with Signal In but outside the preselected Window (LLD-ULD):
  1.1 μS.
  Total Busy Time:
  $BT_{Ch\ 1} + BT_{Ch\ 2} + \ldots BT_{Ch\ 8} + 1\ \mu S$.
- *System Busy Time without "Zero Suppression":*
  Fixed 33 μS
- *DC Offset Control (Zero Energy Intercept):*
  ± 3% of full scale value under CAMAC control with 8-bit resolution.
- *Integral Linearity:*
  Typically ± 0.025% of F.S., better than 0.05%; in any case over 95% of the dynamic range.
  Measured with 0.5 μS semi-gaussian pulse shape. (Tpk = 1,2 μS).
- *Differential Linearity:*
  Typically ± 0.5%, better than ± 1%, in any case over 95% of the dynamic range.
- *Gain Stability:*
  ⩽ 100 ppM/°C.
- *Zero Stability:*
  ⩽ 200 μV/°C.
- *Cross Talk between two Adjacent Inputs:*
  >66 db (measured with 0,5 μS semi-gaussian pulse shape).
- *Count Rate Shift:*
  Not detectable at 100 KHz.

ECL BUS
(Command Bus)

- *Connector:*
  8x2-pin front panel connector. The input matching resistors and output pull-down resistors may be removed to achieve high input and output impedances.
  When these resistors are mounted, the associated LED indicator (RPON) is lit up.
- *Input Level:*
  Differential ECL.
- *Impedance:*
  100 Ω differential.
- *Output Level:*
  Differential ECL (into 100 Ω differential).
- *Gate input (GATE):*
  Common for all analog inputs. For optimum results the gate signal must be applied delayed with respect to the analog signal, but before the pulse to be measured reaches its peak, and must be maintained at least up to this instant.
- *Clear Input (CLR):*
  Common for all analog and digital logic.
  Pulse width ⩾50 ns.
  The module is ready to process a new event after 1,2 μS.

- *Request Output (REQ):*
  Indicates that the module is ready to send data to the ECL DATA BUS. The REQ signal is generated at the end of conversion if the bit related to ECL READOUT in the Status Register has been selected.
- *Write Strobe Output (WST):*
  Indicates the time period during which the data present in the ECL Data Bus can be stored in the external memory. WST is generated in a minimum of 10 ns after the data is ready. Its width is higher than 40 ns.
  During the entire WST pulse, the ECL Data Bus data is maintained stable.
- *Write Acknowledge Input (WAK):*
  This input receives the acknowledge signal indicating that the data present on the ECL bus has been loaded into memory and the next data word may be sent.
  The next WST signal is generated at least 50 ns after the WAK signal.
  Minimum WAK width must be 30 ns.
- *Busy Output (BUSY):*
  This output is set to the "1" state 1 μS after the end of the GATE signal and is held to this state until after the end of the read-out cycle (ECL Read-out or CAMAC Read-out). The BUSY state may be reset only by sending a CLEAR signal via CAMAC or via ECL BUS (CLR). The ADC is ready to start a new conversion 1,2 μS after the end of the BUSY state.

ECL PORT ENABLE/NEXT

- *Readout Enable Input (RDE):*
  1x2-pin panel connector. The RDE signal indicates to the module that it can take control of the ECL Data Bus; RDE must be maintained during entire readout time.
  The signal enables the ECL Data Bus, WST Output and WAK input if the module is ready for data transfer (REQ output ON).
- *Input Level:*
  Differential ECL.
- *Input Impedance:*
  100 Ω differential.
- *Next Output (NEXT):*
  1x2-pin front-panel connector.
  Indicates that the module is not ready to transfer data present on the ECL Data Bus or it has finished data transfer.
  The NEXT output signal is generated by the RDE line in the absence of the REQ internal command or, if this command is present, at the end of data read-out.
  The transit time between RDE and NEXT output is typically 3 ns if the module does not include data read-out capabilities.
- *Output Level:*
  ECL differential (into 100 Ω differential).

ECL PORT OUTPUT

- *Connector:*
  17x2-pin front-panel connector (ANSLEY 609-3407).
  The last two pins are not connected.
- *Output Level:*
  Differential ECL level (into 100 Ω differential).
  The pull-down resistors must be removed for high impedance outputs.
  When these resistors are mounted, the associated LED indicator (RP ON) is lit up.
- *Data Word Size:*
  16 bits.
- *Read-out Mode:*
  Sequential.
- *Max Read-Out Frequency:*
  8 MHz

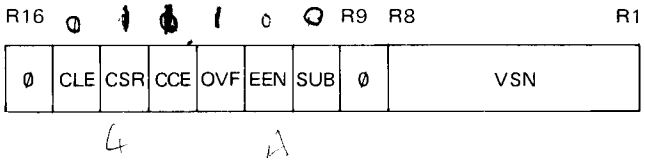
CAMAC COMMANDS AND FUNCTIONS

Z : Initialize; clears the module and the Status Register.
C : Clears the module; does not clear the Status Register and Memory
I : Inhibits the front-panel GATE during CAMAC inhibit command.
X : X response is generated for all valid functions
Q : Q response is generated when the function can be executed
L : LAM (Look-at-me) is set after the end of conversion, if it was enabled, with CAMAC Readout enabled.

F(Ø) . A(Ø) or F(2) . A(Ø)	Read Data	a) CSR=1 CCE=1 with zero suppression b) CSR=1 CCE=Ø without zero suppression

Note: CSR and CCE are STATUS WORD bits (see Status Word)

F(Ø) . A(Ø-7) or F(2) . A(Ø-7)	Reads Data:	CSR = Ø CCE = X addressed readout
F(Ø) . A(14) or F(2) . A(14)	Reads Header Word	
F(Ø) . A(15)	Reads Pattern Word	
F(2) . A(15)	Reads Pattern Word and clears LAM	
F(1) . A(0-7)	Reads Threshold Memory (Upper Threshold - ULD)	
F(1) . A(8-15)	Reads Threshold Memory (Lower Threshold - LLD)	
F(4) . A(Ø-7)	Reads Offset Memory	
F(4) . A(9)	Reads Common Threshold	
F(4) . A(14)	Reads Status Word Register	



R1-R8 (VSN) Logical address of the Module: index source for sequential readout with zero suppression.

R10 (SUB) Channel Subaddress Enable (enabled when SUB=Ø).

R11 (EEN) ECL Readout Enable.
EEN=1 ECL Port Readout
EEN=Ø CAMAC Readout

R12 (OVF) Overflow Indication Enable (enabled when OVF=Ø)

R13 (CCE)
R14 (CSR) Acquisition and Readout Control:
- With zero suppression (sequential readout) CSR=1 and CCE=1
- Without zero suppression (sequential readout) CSR=1 and CCE=Ø
- Addressed readout (without zero suppression) CSR=Ø and CCE=X

R15 (CLE) CAMAC LAM Enable (enabled when CLE = 1)

F8 - A(Ø) Tests LAM. Q = 1 if LAM is present

F9 . A(Ø) Clears the Module

F10 . A(Ø) Clears LAM

F16 . A(Ø-7) Reserved for ADC 4418/Q

F17 . A(Ø-7) Writes Threshold Memory (Upper Threshold - ULD)

F17 . A(8-15) Writes Threshold Memory (Lower Threshold - LLD)

F20 . A(Ø-7) Writes Offset Memory

F20 . A(9) Writes Common Threshold

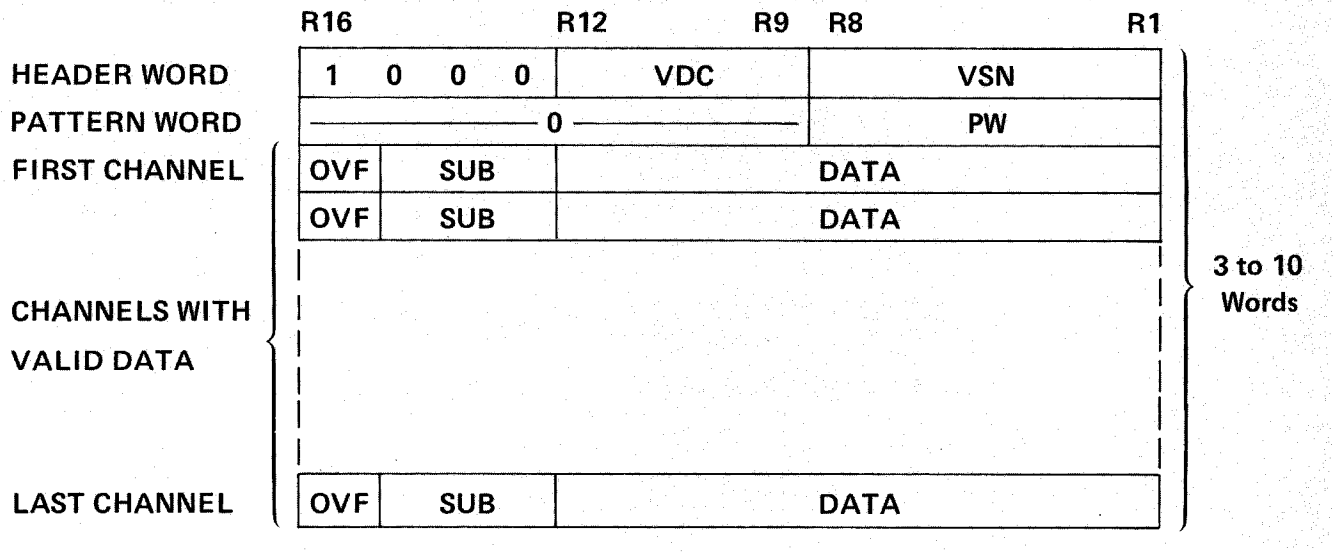
F20 . A(14) Writes Status Word

F25 . A(Ø) Test Function

Readout Format

Note: EEN, CSR and CCE are Status Word bits (see Status Word)

1) With zero suppression (sequential readout):
CSR=1 CCE=1
EEN=1 ECL Port Readout
EEN=Ø CAMAC Readout



VSN : Virtual Station Number; loaded in the associated Memory

VDC: Number of Valid Data following Pattern Word (from 1 to 8)

PW : Valid Data View: R1 is referred to channel Ø
R8 is referred to channel 7

OVF : Overflow Indication; enabled with OVF=Ø (Status Word bit)

SUB : Channel Subaddress, enabled with SUB=Ø (Status Word bit)

DATA : 12-bit output Data

There is sequential readout.
CAMAC Readout function F(Ø) . A(Ø) or F(2) - A(Ø)

2) Without zero suppression (Sequential readout):
CSR=1 and CCE=Ø
EEN=1 ECL Port Readout
EEN=Ø CAMAC Readout

There is always sequential readout of 8 words.
OVF : Overflow Indication; enabled with OVF=Ø (Status Word Bit)
SUB : Channel Subaddress, enabled with SUB=Ø (Status Word Bit)

Always 8 words

R16	R15	R12 ... R1
OVF	SUB	DATA - CHANNEL Ø
OVF	SUB	DATA - CHANNEL 1
OVF	SUB	DATA - CHANNEL 2
OVF	SUB	DATA - CHANNEL 3
OVF	SUB	DATA - CHANNEL 4
OVF	SUB	DATA - CHANNEL 5
OVF	SUB	DATA - CHANNEL 6
OVF	SUB	DATA - CHANNEL 7

3) CAMAC Addressed Readout
CSR=Ø CCE=Indifferent
EEN=Ø Only CAMAC Readout

There is Camac Addressed Readout with
F(Ø) . A(Ø-7) or F(2) . A(Ø-7) functions
F(2) . A(7) clears the module during S2
Header Word can be readout with
F(Ø) . A(14) or F(2) . A(14)

Pattern Word can be readout with
F(Ø) . A(15) or F(2) . A(15)
OVF : Overflow Indication; enabled with OVF=Ø (Status Word bit)
SUB : Channel Subaddress; enabled with SUB=Ø (Status Word bit)

Max 8 Words

R16	R15	R12 ... R1
OVF	SUB	A(Ø) - DATA
OVF	SUB	A(1) - DATA
OVF	SUB	A(2) - DATA
OVF	SUB	A(3) - DATA
OVF	SUB	A(4) - DATA
OVF	SUB	A(5) - DATA
OVF	SUB	A(6) - DATA
OVF	SUB	A(7) - DATA

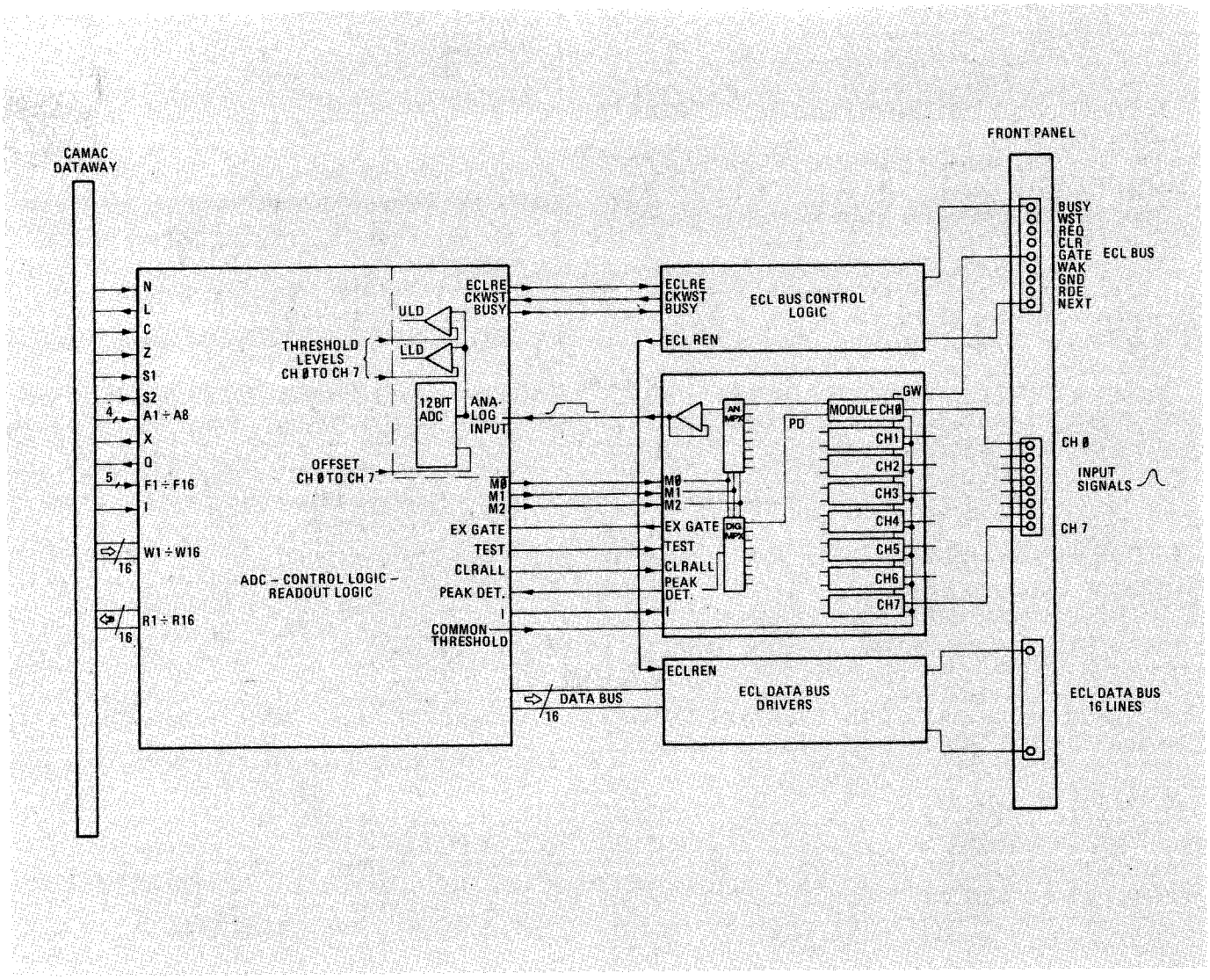
GENERAL

Packaging. RF-shielding 1-width CAMAC module

Power Requirements:
+ 24V at 0,3A, -24V at 0,3A; + 6V at 1,4A;
-6V at 1,55A

Note: When all output pull-down and input matching resistors are removed, the current at -6V is reduced to 1,4A.

SILENA 4418/V - EIGHT CHANNELS ADC
BLOCK DIAGRAM



Specifications are subject to changes without notice.

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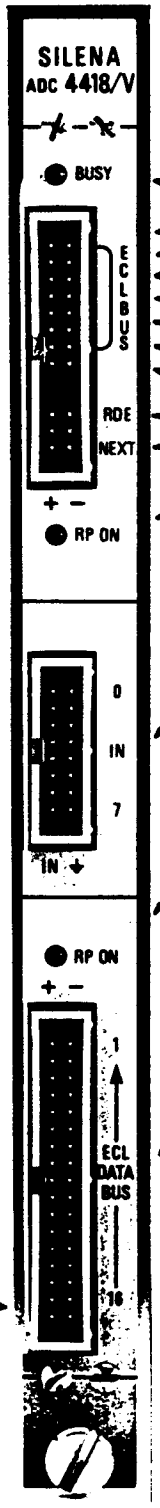
1.1 FRONT PANEL



ECL BUS (section 1.10.1)

BUSY LED

BUSY = BUSY output
WST = write strobe line
REQ = request bus line
CLR = fast CLEAR
GATE = GATE input
WAK = write acknowledge
GND = GROUND
RDE = readout enable input
NEXT = readout enable output

} ECL LEVEL differential

LED on if matching and pull-down resistors are mounted on the ECL BUS (section 1.10.1)

Analog inputs IN signal (section 1.3)
⏚ ground

LED on if data bus pull-down resistors are mounted on the ECL DATA BUS (section 1.10)

ECL DATA bus outputs (section 1.10)

Last 2 pins not connected