CAMAC COMMANDS & FUNCTIONS

STANDARD CAMAC FUNCTION CODES

F0, A0	Read FIFO data until end of event, Q=1 for valid data, Q=0 at end
F0, A1	Read FIFO data always, (common start only)
F0, A2	Examine FIFO output, do not advance FIFO (common start only)
F1, A0	Read Control register 0
F1, A1	Read Control register 1
F1, A2	Read Control register 2
F1, A3	Read Control register 3
F1, A4	Read Control register 4 (common start only)
F1, A5	Read Control register 5 (common start only)
F1, A6	Read CAMAC Test Register (common start only)
F8, A0	Test LAM
F9, A0	Clear all data and LAM. This does NOT affect the control registers
F10, A0	Clear LAM
F16, A0	Write 16 bit data to FIFO (common start only)
F16, A1	Write fifo tag bit (common start only)
F17, A0	Write Control register 0
F17, A1	Write Control register 1
F17, A2	Write Control register 2
F17, A3	Write Control register 3
F17, A4	Write Control register 4 (common start only)
F17, A5	Write Control register 5 (common start only)
F24, A0	Disable LAM
F24, A1	Disable Acquisition mode
F25, A0	Initiate test cycle (common start only)
F26,A0	Enable LAM
F26, A1	Enable Acquisition mode
F27, A0	Test buffering in progress (BIP), Q=1 while BIP
F27,A1	Test busy, Q=1 while busy
F27, A2	Test event ready, Q=1 if event ready for readout
F27, A3	Test fifo tag bit, Q=1 if tag bit set for word to be read next
F30	Begin the reprogramming sequence

For completeness, the following commands are available only during the programming mode of the model 3377's internal Xilinx logic chip. These enable the mode to be set by selecting a firmware program from the 4 that are installed in the EPROM, or loading a different program from CAMAC. For these commands, the A lines are not decoded, they are simply ignored.

F9	Clear data buffers, enable Xilinx program
F12	Test if Xilinx ready for data (Q=1 when ready)

F13	Test Xilinx programming done (Q=1 when done)
F14	Test Xilinx INIT signal
F16	Write 8 bits to Xilinx
F21	Select EPROM mode 1
F22	Select EPROM mode 2
F23	Select EPROM mode 3
F25	Begin Xilinx programming sequence
F28	Select CAMAC programming mode
F30	Enable Xilinx programming mode (this resets the Xilinx, and selects EPROM mode 0)

OPERATING INSTRUCTIONS

The 3377 has four separate operating modes. The mode is determined by the Xilinx program loaded from the eprom, see below for changing operating mode. The times are measured with respect to a common hit, which can occur before or after the individual time signal to be measured (Common Stop or Common Start mode). The other mode dependent feature is the data format, which can be either single or double word. A summary of the modes is listed below.

Mode	Operation	Data Format
0	Common Stop	Single Word
1	Common Start	Single Word
2	Common Stop	Double Word
3	Common Start	Double Word

Since the features and control registers of the modes are quite different in some cases, the control registers, data word formats, and operation of the four different modes are discussed separately in the "Operating Modes" section.

PROGRAMMING THE UNIT FOR A DIFFERENT MODE OF OPERATION

When initially powered on, the module configures itself for Common Stop, Single Word mode. The module is ready for the first command approximately 200 milliseconds after power on.

To change to any other mode the following sequence of CAMAC operations to the module is required:

1. F30, any subaddress. This selects programming mode and resets the Xilinx gate array. The default program load is the Common Stop mode, Single Word data format.

2. To select a program mode other than the default, perform an F21, F22, or F23 CAMAC operation. To reprogram the Common Stop Single Word mode, simply skip this step.

   F21, any subaddress. This selects the common start, single word program load.

   F22, any subaddress. This selects the common stop, double word program load.

   F23, any subaddress. This selects the common start, double word program load.

3. F25, any subaddress. This begins the programming of the Xilinx chip, using the selected program load (or the default load). This will take less than 200 milliseconds to complete.

4. F13, any subaddress. Test the done flag, return Q=1 when programming is complete. The host computer should loop on this command until Q is equal to 1.

5. F9, any subaddress. This is REQUIRED after reprogramming. This resets the on board PAL (programmed array logic device) which allows the Xilinx to be programmed, causing all function codes to be ignored by the PAL, except for F30, which starts the reprogramming sequence. The F9 command also MUST be the FIRST command received by the module after power up, to ensure that the PAL has been disabled.

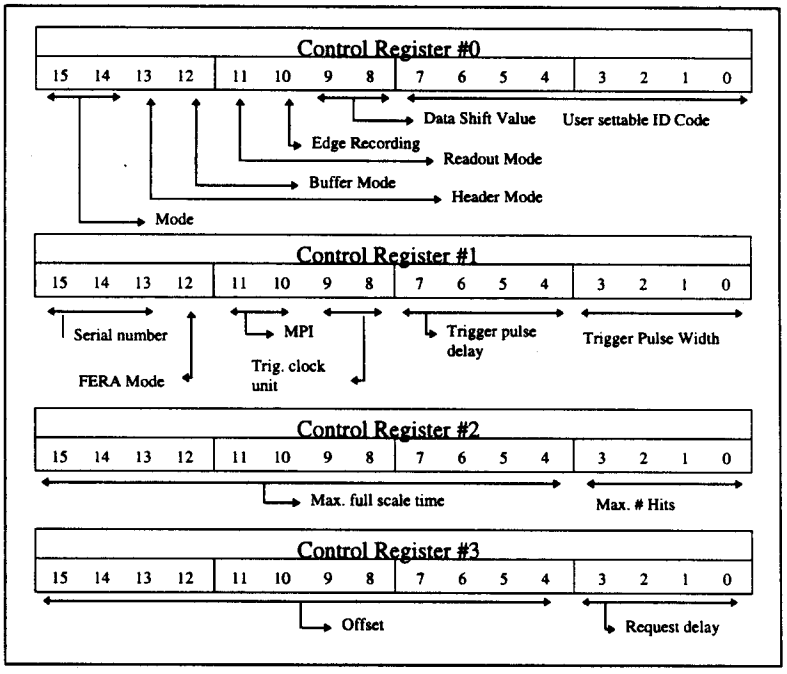
After loading the Xilinx gate array, and performing the F9 command, the Xilinx gate array takes control of the module. The new CAMAC function codes which have been programmed into the gate array logic become operational.

OPERATING MODES

The control registers, header contents, data word format, and trigger outputs are dependent on the mode setting.

Mode 0: Common Stop, Single Word Mode

Control Registers



Mode 0 Control Registers

control register 0 (subaddress 0)

bits 0-7 user definable module ID code. This appears in the header data word. default is 0.

becomes false. If the next data word is valid, the handshake sequence is repeated, otherwise PASS is set true and the FERA drivers are disabled.

After the event has been transferred, the 3377 waits for REN to become false, then PASS is set false. The 3377 is now ready to send the next event, as soon as REN becomes true again

For test purposes the PASS output can be connected to the REN input (with a half twist, to invert the signal), to simulate the existence of a 4301 or other FERA driver.

Similarly the WST output can be connected to the WAK input (without a twist) to perform the handshake. With this jumper in place the FERA readout will run at maximum speed, 100 nsec per word.

The FAST FERA select bit in register 1, when set to 1, disables the WST - WAK handshake. The WAK is ignored, the WST is asserted at 100 nsec intervals, and the readout runs at its maximum speed. The effect is similar to adding the WST - WAK jumper, without using up the WST output. If the select bit is set to 0, the WST -WAK handshake proceeds normally, as described above.

Suppressing the Header

The Header mode bit, register 0, bit 13, when set to 1, allows suppressing the header word if there is no data in the event. This is effective in all readout modes, single or double word, buffered or unbuffered, CAMAC or FERA. The event is not suppressed, only the header, so the event ordering remains correctly synchronized among multiple 3377 modules. If the channel occupancy is low, the use of this feature can result in a reduction in the size of the data block for each event, and a small decrease in readout time (not the same as the dead time). It is recommended that the last module in a readout group be set to always supply the header (bit 13 set to 0).

Data Formats

The 3377 output data is in either single or double word format. These formats are identical for Common Start or Common Stop operation, and for CAMAC or ECLbus readout.

Single Word Format

The output data consists of a header word, followed by up to 512 data words. An event with no data consists of only the header word. If header suppression is selected, an event with no data results in zero words.

HEADER

bits 0-7	the 8 bit module ID (from register 0)
bits 8-9	the 2 bit resolution value (from register 0)
bit 10	the leading/both edge recording bit (from register 0). 0 = leading only 1 = both
bits 11-13	the event serial number, modulo 8
bit 14	always 0, identifies single word readout
bit 15	always 1, identifies header word

DATA WORD, leading edge only recording

bits 0-9	10 bit data value
bits 10-14	5 bit channel number
bit 15	always 0, identifies data word

DATA WORD, leading edge AND trailing edge recording

bits 0-8	9 bit data value
bit 9	Identifies the edge, 0 = leading, 1 = trailing
bits 10-14	5 bit channel number
bit 15	always 0, identifies data word

Double Word Format

The output data consists of a header word, followed by up to 1024 data words. An event with no data consists of only the header word. If header suppression is selected, an event with no data results in zero words.

HEADER

bits 0-7	the 8 bit module ID (from register 0)
bits 8-9	the 2 bit resolution value, always 0
bit 10	the leading/both edge recording bit (from register 0). 0 = leading only, 1 = both
bits 11-13	the event serial number (modulo 8)
bit 14	always 1 (identifies double word readout)
bit 15	always 1, identifies header word

FIRST DATA WORD

bits 0-7	8 bit data value
bit 8	1, indicates that the data is the most significant byte.
bit 9	Identifies the edge, 0 = leading, 1 = trailing
bits 10-14	5 bit channel number
bit 15	always 0, identifies data word

SECOND DATA WORD

bits 0-7	8 bit data value
bit 8	0, indicates that the data is the least significant byte.
bit 9	identifies edge, 0 = leading, 1 = trailing
bits 10-14	5 bit channel number