ORTEC®

A
CAMAC 16k

- 16,128-channel ADC with CAMAC and fast FERAbus™ readout for: single- or multi-parameter experiments, high counting rates, and wide energy ranges
- 5-µs conversion time
- FERAbus readout can skip ADCs with no information in 3 ns, and read each active ADC in 200 ns
- Gedcke-Hale Live-Time Clock includes dead-time correction for amplifier pulse pile-up losses
- CAMAC control of: live-time clock, FERAbus/CAMAC readout, zero and overflow suppression, master gate, local gate, singles/coincidence modes, upper- and lower-level discriminators, and input dc-offset
- Differential input suppresses ground-loop noise

The ORTEC Model AD114 CAMAC 16k ADC is a 14-bit analog-to-digital convert (ADC) with CAMAC and fast FERAbus readout. It is a very productive solution for high-multiplicity multi-parameter experiments, because it has a conversion time of 5 µs, and a 100-ns-per-word FERAbus readout that skips ADCs with zero information in 3 ns. The 16,128-channel digital resolution provides excellent peak definition when analyzing wide energy ranges with high-resolution germanium detectors. In four-fold coincidence experiments a dead time as low as 15% for each detector channel results in a coincidence dead-time loss of 48%. Consequently, the live-time clock included in each Model AD114 is vital for calculating the true coincidence rate. The flexibility of the computer-controlled functions also makes the Model AD114 useful for silicon charged-particle detectors, scintillation detectors, proportional counters, and ionization chambers.

The dc-coupled analog input employs a peak amplitude stretcher, and accepts pulses in the linear range from 0 to +10 V. A 14-bit, successive-approximation ADC with sliding scale linearization provides the conversion to a digital number in 5 µs. The analog input accepts unipolar and bipolar pulses from standard spectroscopy amplifiers with shaping times from 0.25 to 20 µs. A differential input is incorporated to suppress ground-loop noise when connected to systems with multiple power supplies and grounds. CAMAC control of the input dc-offset, the lower-level discriminator, and the upper-level discriminator facilitates computer adjustment of the analog operating parameters.

Several types of gating are provided. For coincidence experiments employing the FERAbus readout, the master GATE input is delivered to all ADCs through the ECL CONTROL bus. This gate synchronizes the ADCs on coincident events and forces all ADCs to wait for a common clear at the end of event readout. In the CAMAC readout mode, the master GATE can be delivered to all ADCs as a TTL input on the front-panel LEMO connector. Using only the master GATE to define coincident events can lead to the random analysis of unrelated events at individual ADC inputs. These unwanted events can be suppressed by providing a LOCAL GATE input to each ADC only when there is a valid, coincident event at the ADC INPUT. The rear-panel PUR input is an anticoincidence gate for use with the pile-up rejector logic pulse from a spectroscopy amplifier. It can also be used as a general-purpose veto input. CAMAC commands permit enabling and disabling the module's response to the master GATE or the LOCAL GATE inputs. This is useful when selecting the coincidence mode or the singles mode for the Model AD114 under CAMAC control.

Additional modes selectable by CAMAC command are: CAMAC or FERAbus readout, zero-suppression or no zero-suppression during readout, overflow suppression, and singles or coincidence analysis.

Each Model AD114 includes its own live-time clock for correction of dead-time losses. The Gedcke-Hale live-time clock[1] corrects for the pile-up losses occurring in the spectroscopy amplifier, and for the dead time of the ADC conversion and readout. It provides complete dead-time correction for amplifiers directly presenting their unipolar output pulse, and/or amplifiers providing the appropriated BUSY and PUR logic signals. Via CAMAC commands, the live-time clock can be reset, started, stopped, and read without stopping.

The Model AD114 is compatible with the standard LeCroy FERA control and data output busses. This system can provide very fast readout of the ADCs with non-zero events in a CAMAC crate full of ADCs. For both data acquisition and readout, the control bus synchronizes all ADCs with the experiment's master trigger. This permits identification of all the ADC outputs from the same event and their subsequent assimilation into a common block of data. To the standard FERAbus features, ORTEC has added the ability to select the singles or coincidence analysis mode for any Model AD114. This feature allows checking the functionality of a detector via the singles spectrum at any time during an experiment. The Model AD114 can be mixed with the ORTEC Model AD413A in the same FERAbus readout loop.

Normally, all the ADCs in the crate are connected to a LeCroy Model 4301 FERA Driver for control and readout (Fig. 1). The FERA Driver, in turn, delivers the data to either a LeCroy Model 4302 Dual Port Fast Memory in CAMAC, or a CES Model HSM8170 High Speed Memory in VMEbus. Both memories operate in the list mode to assemble the block of coincident events for further processing by an event builder. To facilitate making the interconnections between the FERAbus modules, the C-ECLBUS Cable Kit is recommended as a separately ordered accessory. This kit contains the cables and connectors needed for a crate full of FERAbus modules.

PERFORMANCE

ADC ANALOG INPUT Accepts analog input pulses in the range from 0 to +10 V. The peak amplitude of an input pulse is converted to a digital value by a successive-approximation ADC with sliding scale linearization.

RESOLUTION 16,128 channels (0.625 mV/channel).

CONVERSION TIME 5 µs.

INTEGRAL NONLINEARITY <±0.025% over the top 99% of the dynamic range.

DIFFERENTIAL NONLINEARITY <±1% over the top 99% of the dynamic range.

TEMPERATURE SENSITIVITY 0 to 50°C.
Gain <50 ppm/°C.
Zero Offset <50 ppm of full scale per °C.

LOWER-LEVEL DISCRIMINATOR RANGE CAMAC controlled from 0 to 512 mV (2 mV/bit).

UPPER-LEVEL DISCRIMINATOR RANGE CAMAC controlled from 8.5 V to 10.5 V (8 mV/bit).

DC OFFSET RANGE CAMAC controlled adjustment of input dc offset from –40 mV to +40 mV (0.312 mV/bit).

LIVE-TIME CLOCK CAMAC controlled, Gedcke-Hale live-time clock 1 with a maximum count of 167,772.16 seconds (1.94 days) and a resolution of 10 ms. Readable without interruption.

CAMAC CONTROL OF READOUT MODES Selection of: CAMAC or FERAbus (ECL bus) readout, sequential readout of all ADCs or suppression of ADCs with zeros (zero-suppression mode), overflow-suppression option, and singles or coincidence modes.

READOUT TIME
Zero-Suppressed Readout Mode Two words at

CONTROLS AND INDICATORS

BUSY Front-panel, multicolor LED indicates the percentage of time the ADC is busy: green for 0–40%, yellow for 40–70%, and red for >70% busy.

PD Two front-panel red LEDs: one for the ECL CONTROL connector, and one for the ECL DATA OUTPUT connector. Turned on when the ECL pull-down resistors or termination resistors are installed for the respective connector.

INPUTS

INPUT Front-panel BNC connector accepts analog pulses for pulse amplitude digitization in the linear range from 0 to +10 V. Input signals can be positive unipolar pulses, positive gated integrator pulses, or bipolar pulses (with the positive lobe leading). Pulse shapes can be semi-Gaussian or triangular, with shaping time constants from 0.25 to 2 0 µs, or delay-line-shaped with widths >0.25 µs. Maximum input is ±12 V. No internal delay. Center conductor input impedance is 2000 Ω to ground, dc-coupled. The floating BNC connector shield is used with a differential input amplifier to suppress common-mode input noise caused by ground loops. The common-mode rejection ratio is nominally 99:1 with a zero-impedance source, and nominally 22:1 with a 93 Ω signal source.

LOCAL GATE Front-panel BNC connector provides individual gating for the associated analog input. A low TTL logic level (0 to +0.8 V) prevents analysis of the analog signal at the INPUT connector. A high TTL logic level (+2 to +5 V) permits analysis of the analog signal. Resides in the high state with no input connected. The LOCAL GATE signal must be at the desired logic level prior to the peak amplitude of the analog pulse, and must extend ≥0.5 µs beyond peak detection. Input impedance is 1000 Ω. Response to the LOCAL GATE connector can be enabled/ disabled by CAMAC commands.

100 ns per word for FERAbus readout, or at 1 µs per word for CAMAC readout.
Sequential Readout Mode One word at 100 ns per word for FERAbus readout, or at 1µs per word for CAMAC readout.

CAMAC COMMANDS

Z Initializes module. Clears the module and sets all bits of the control register to zero. Sets the LLD register to 36 (72 mV), the ULD register to 255 (10.5 V), and the offset register to 128 (0 V). Enables the ADC [F(26)·A(0)], and clears the live-time clock.

C Performs the same function as the CLR input.

I Inhibits subsequent conversions and stops the live-time clock when asserted. Conversions and readouts already in progress are not affected. Used to start or stop data acquisition on all ADCs in the CAMAC crate at the same time.

X Generated by the module for all valid functions.

Q Generated by the module if the function can be executed.

L Indicates LAM is set. Occurs after the end of conversion, if there are data to be read (provided CAMAC readout is enabled, and LAM is enabled). See CONTROL REGISTER FORMAT.

F(0)·A(0) Read Control Register.

F(1)·A(0) Read lower-level discriminator (LLD) setting. The value returned is in units of 2 mV. Only the lower 8 bits are valid.

F(1)·A(1) Read upper-level discriminator (ULD) setting. Multiply the lower 8 bits by 0.008 V and add 8.5 V to calculate the voltage setting.

F(1)·A(2) Read the input dc offset setting. Subtract 128 from the lower 8 bits and multiply the resulting 8-bit number by 0.312 mV to calculate the voltage setting.

F(2)·A(0) Read ADC converted digital output. If the zero-suppression mode is disabled (Control Register B9 = 1), and the CAMAC readout mode is selected (B10 = 1), the command is issued once to read the ADC data. If zero-suppression is enabled (B9 = 0) with the CAMAC readout mode (B10 = 1), the command is issued twice, or until Q = 0. Q = 1 for a valid readout.

F(3)·A(0) Read the lower 16 bits of the live-time clock. The value is returned in units of 10 ms. When this command is issued the highest 8 bits of the live-time clock are simultaneously captured and stored for a subsequent F(3)·A(1) command.

F(3)·A(1) Read the higher 8 bits of the live-time clock. This command reports the value of the higher 8 bits captured by the last F(3)·A(0)

GATE Front-panel LEMO connector accepts the master gate signal for coincidence mode operation with CAMAC readout. See ECL GATE for function. A low TTL logic level (0 to +0.8 V) prevents analysis, and a high TTL logic level (+2 to +5 V) permits analysis. Resides in the low state with no input connected. Input impedance is 1000 Ω.

PUR Rear-panel BNC connector accepts the pile-up rejecter logic signal from the spectroscopy amplifier supplying the associated analog input pulses. A high TTL logic level (+2 to +5 V) causes rejection of the analog signal; a low TTL logic level (0 to +0.8 V) permits analysis of the analog signal. Defaults to a low state with no input connected. For required timing see LOCAL GATE. Input impedance is 1000 Ω.

BUSY Rear-panel BNC connector accepts the Busy output logic signal from the spectroscopy amplifier supplying the analog input pulses. Either a high TTL logic level (+2 to +5 V) at the BUSY input, or the analog input pulse exceeding the ADC lower-level discriminator will cause the live-time clock to start counting backwards. The live-time clock turns off when the stretcher detects peak amplitude on the analog input pulse, or when a PUR input occurs. The live-time clock resumes counting forward after BUSY, PUR, and the lower-level discriminator all become inactive, and readout of the conversion has been completed. The BUSY input is inactive at a low TTL logic level (0 to +0.8 V) when no input is connected. Input impedance is 1000 Ω.

ECL INPUTS/OUTPUTS

The fast FERAbus readout utilizes the front-panel ECL CONTROL bus and the ECL DATA OUTPUT bus. Differential input impedances are 100 Ω with termination resistors installed. Only one module should have the termination and pull-down resistors installed (See PD LED and Fig. 1).

ECL LOGIC LEVELS Nominal differential ECL logic levels (into 100 Ω differential load) are:

	Left (+) Pin	Right (–) Pin
Logic 0	–1.8 V	–0.9 V
Logic 1	–0.9 V	–1.8 V

ECL DATA OUTPUT Front-panel 17- by 2-pin connector (AMP 1-103326-7) provides the digitized ADC outputs for connection to the FERA data readout bus. Differential ECL outputs are employed, with bit 1 assigned to the two pins in row 1, and bit 16 occupying the two pins in row 16. Row 17 is not connected. See READOUT FORMAT. Interconnection between ADC modules and the FERA Driver (LeCroy 4301)

command.

F(8)·A(0) Test LAM. Q = 1 if LAM is present.

F(9)·A(0) Clear Module. Performs the same function as the C command, except only for the single module being addressed through CAMAC.

F(10)·A(0) Test and clear LAM. Q = 1 if LAM was set.

F(12)·A(0) Reset live-time clock to zero.

F(16)·A(0) Write into the Control Register.

F(17)·A(0) Write lower-level discriminator value. See F(1)·A(0) for format.

F(17)·A(1) Write upper-level discriminator value. See F(1)·A(1) for format.

F(17)·A(2) Write input dc-offset value. See F(1)·A(2) for format.

F(24)·A(0) Disable ADC. Performs the same function as the Inhibit (l) command, but only for the addressed ADC. Stops the live-time clock and prevents further conversions from occurring until F(26)·A(0) is issued.

F(26)·A(0) Enable the ADC. Enables conversions and starts the live-time clock when the Inhibit (l) command is not active.

F(27)·A(0) Test current status of the ENABLE/DISABLE flag as set by the F(26)·A(0) and F(24)·A (0) commands. Q = 1 if the ADC is enabled.

CONTROL REGISTER FORMAT

Bit and Function

B1 to B8 Virtual Station Number. Index Source for readout with zero-suppression. (Lower eight bits of header word.)

B9 Zero-suppression enable. When B9 = 0, ADCs with zeros for data are skipped during readout.

B10 ECL port enable. When B10 = 0, ECL port readout is enabled. When B10 = 1, CAMAC readout is enabled.

B11 Enable LOCAL GATE (B11 = 0). When B11 = 1, the LOCAL GATE input is ignored, and all analog pulses are converted, unless gated by the master GATE or by PUR.

B12 Enable master GATE (B12 = 0) for the coincidence mode. When B12 = 1, the master GATE signal is ignored, and all analog pulses are converted, unless gated by the LOCAL GATE or by PUR. B12 = 1 is used only in conjunction with the singles mode (B13 = 1).

B13 Selects the Coincidence mode or the Singles mode. When B13 = 0, the coincidence mode is selected (requires B12 = 0). When B13 = 1, the requires construction of a 34-conductor ribbon cable (3M part number 3365/34) with 17- by 2-pin headers (3M 3414-6006 or AMP 499498-9) spaced to match the configuration of modules (Fig. 1).

ECL CONTROL BUS Front-panel 8- by 2-pin connector accommodates the control bus for synchronizing data acquisition among multiple ADCs, and for ECL readout. Except where noted otherwise, the inputs to the Model AD114 are provided from the LeCroy 4301 FERA Driver connected to the bus. A row of two pins is assigned to each differential ECL input or output. Interconnection between ADC modules and the FERA Driver (LeCroy 4301) requires construction of a 16-conductor ribbon cable (3M part number 3365/16) with 8- by 2-pin headers (3M 3452-6006 or AMP 499497-3) spaced to match the configuration ofmodules (Fig. 1). The logic signals in the ECL CONTROL bus are listed below.

N/C No connection.

WST The Write Strobe output indicates when each output word is valid on the ECL DATA OUTPUT connector. WST is released 15 ns after the Write Acknowledge (WAK) is received.

REQ The Request output indicates that the module has completed its conversions, and is ready to take control of the ECL DATA OUTPUT bus for readout. REQ can be asserted only if FERAbus readout is enabled.

CLR Clears stored data and conversions in progress for all ADCs connected to the ECL CONTROL bus. Required in the coincidence mode at the end of readout to simultaneously release all ADCs for the next conversion. CLR is not required in the singles mode. Minimum width, 5 ns. Clear can also be initiated from the CAMAC interface. If Clear is asserted during ADC conversion, up to 5 µs are required to clear the module.

GATE The Gate input simultaneously provides the master gate signal to all ADCs connected to the ECL CONTROL bus for coincidence mode operation. The logic 1 state enables acceptance of the analog input signal for conversion, and forces all ADCs to wait for a common clear (CLR) after analyzing coincident events. With no signal connected, the GATE input remains in the logic 0 state. See LOCAL GATE for required timing. The ECL GATE input is OR'ed with the TTL GATE input from the LEMO connector. Response to the GATE input can be enabled/disabled by CAMAC commands.

WAK The Write Acknowledge input signal

singles mode is selected (typically with B11 = 1, B12 = 1). When in the singles mode, the zero-suppression mode must be selected (B9 = 0) for all ADCs, if the FERAbus readout loop includes more than one ADC.

B14 Not used.

B15 CAMAC LAM enable. When B15 = 1, LAM is enabled.

B16 Overflow-suppression enable. When B16 = 0, overflows are converted to zeros in the ADC output data. Readout will be suppressed only if the zero-suppression mode (B9 = 0) is selected.

READOUT FORMAT

The readout format of the Model AD114 is identical in both the CAMAC and the FERAbus ECL readout modes.

WITHOUT ZERO-SUPPRESSION

B16	B15	B14 . . . . . .B1
0	0	DATA

WITH ZERO-SUPPRESSION When zero-suppression is enabled and valid data are received, two data words are output. The first is always a header word:

B16	B15	B14	B13 B12	B11	B10	B9	B8 . . . B1
1	0	0	WRDCNT	0	0	0	VSN

Followed by one data record with the following format:

B16	B15	B14 . . . . . . B1
0	0	DATA

DEFINITIONS

WRDCNT The word count defines the number of data records that follow the header word in the readout. The word count is always 01 for a Model AD114.

VSN The Virtual Station Number (0 to 255) identifies the module number during zero-suppressed readout. VSN is set via CAMAC command in the lower 8 bits of the Control Register.

DATA Fourteen bits of ADC conversion data. DATA over 16,128 indicates an overflow.

ELECTRICAL AND MECHANICAL

POWER REQUIRED The model AD114 derives its power from a CAMAC crate supplying ±24 V and ±6 V. The power required is +24 V at 160 mA, +6 V at 1.4 A, –6 V at 0.9 A, and –24 V at 170 mA.

WEIGHT
Net 1.1 kg (2.5 lb).

indicates through the readout controller (LeCroy 4301) that the associated memory has read the current word and that the next word may be sent. WAK minimum width is 30 ns.

GND Connected to ground.

N/C No connection.

REN The Readout Enable input is a front-panel, 1- by 2-pin connector. It accepts the PASS output from a previous module, or the REO output from the LeCroy 4301, to enable readout of the Model AD114. Interconnection requires construction of a 100-Ω, twisted-pair cable with a 2-pin socket and housing (AMP 1-87756-8 and AMP 5-87456-3) on each end.

PASS The PASS output is provided on a front-panel, 1- by 2-pin connector. It indicates completion of the module's readout cycle on the ECL bus. The PASS output is normally connected to the REN input on the next module to enable readout of the next module (Fig. 1). In the zero-suppression mode, the Model AD114 generates the PASS signal typically within 3 ns of receiving the REN signal if the Model AD114 has no data to read out. The PASS signal from the last Model AD114 in the readout loop is used to generate the CLR signal via the external master trigger logic for the experiment and/or the LeCroy 4301.

OPTIONAL ACCESSORIES

The C-ECLBUS Cable Kit is recommended as an accessory to facilitate the FERAbus interconnections.

Each kit contains:

Qty	Description
1	16-conductor ribbon cable with 23 headers installed at 7.6 cm intervals for the ECL Control Bus.
1	34-conductor ribbon cable with 23 headers installed at 7.6 cm intervals for the ECL Data Bus.
1	51-cm long twisted pair cable with 2-pin sockets and headers on each end for the PASS to CLI connection.
23	15-cm long twisted pair cables with 2-pin sockets and headers on each end for the REO to REN, and the PASS to REN connections.

The ribbon cables will serve an entire crate full of FERAbus modules, and can be cut to handle smaller groups of modules.

ORDERING INFORMATION

Shipping 2.0 kg (4.5 lb)

DIMENSIONS CAMAC-standard double-width module, 3.42 X 22.15 cm (1.35 X 8.72 in.) front panel IEEE/583-1982 (Reaff 1988).

To order, specify:

Model	Description
AD114	CAMAC 16k ADC
C-ECLBUS	Cable Kit for the ECLBUS

[1] Ron Jenkins, R.W. Gould, Dale Gedcke, *Quantitative X-Ray Spectrometr*y, (New York and Basel: Marcel Dekker) 1981, pp. 266–271.

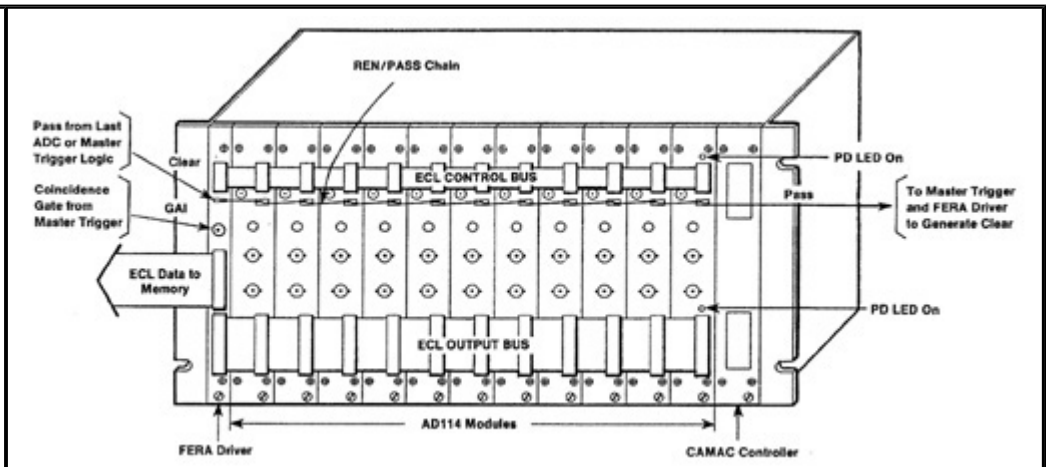

Fig. 1. Interconnection of Multiple AD114s and the LeCRoy 4301 FERA Driver for FERAbus Readout.