Instruction Manual

KineticSystems

Model 3615

Six-Channel, 100 MHz Counter

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CAMAC module

3615 6-Channel, 100 MHz Counter

PRODUCT BRIEF

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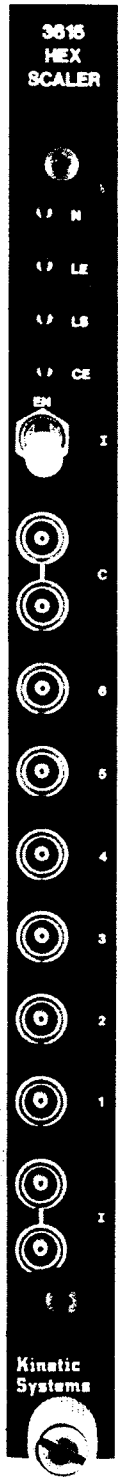
FEATURES

- 6 COUNTERS
- MAXIMUM COUNT 16,777,215
- LAM ON OVERFLOW
- NIM STANDARD INPUTS
- dc TO 100 MHz
- 10 nsec PAIRED PULSE RESOLUTION

APPLICATIONS

- EVENT COUNTING
- NUCLEAR COUNTING
- FREQUENCY MEASUREMENT
- TOTALIZER



GENERAL DESCRIPTION

The Model 3615 is a single-width CAMAC module containing six 24-bit counters. These counters accept terminated NIM* signals at rates from dc to 100 MHz (minimum pulse width 3 nsec). Each counter has an overflow bit which is set on a carry from either bit 16 or bit 24, and which can generate a LAM, if enabled. The pattern of overflow bits in a module can be read. An overflow output for each counter can be wired to a rear-panel P.C. edge connector for cascading counters. The counters can be inhibited by Dataway Inhibit or by a front-panel signal. The counters can be individually cleared by Dataway command or as a group by Dataway clear or front-panel signal. The input is protected for a ±50 volt transient or ±4 volts dc. Counter inputs are terminated in 50Ω while inhibit and clear inputs are bridged high impedance.

The Model 3655 Timing module can provide a time base for this module since the Model 3655 can assert the Dataway Inhibit line for a programmable interval. A front-panel switch is provided to enable the inhibiting of counting by the Dataway Inhibit line.

When the count in any counter reaches 2^{24} (or 2^{16} selected by a jumper), the counter rolls over and continues to count and a corresponding overflow LAM status bit is set. The six LAM status bits are OR'ed and can be enabled to produce a LAM request. The pattern of the six LAM status bits can be read to locate the specific counter that overflowed.

*The nominal NIM signal is: 16 mA into 50Ω for a 1 and 0 mA for a 0.

FUNCTION CODES

Command		Q	Action
F(0)·A(i)	RD1	1	Reads the counter i.
F(1)·A(12)	RD2	1	Reads the LAM status register.
F(2)·A(i)	RC1	1	Reads the counter i and clears the counter i and the LAM status i.
F(8)·A(0)	TLM	LR	Tests if a LAM request is present.
F(9)·A(i)	CL1	1	Clears the counter i and the LAM status i.
F(10)·A(i)	CLM	1	Clears the LAM status i.
F(24)·A(0)	DIS	1	Disables the LAM request.
F(25)·A(0)	XEQ	1	Increments all counters.
F(26)·A(0)	ENB	1	Enables the LAM request.
C	CC	0	Clears all counters and the LAM status register.
Z	CZ	0	Clears all counters, clears the LAM status register, and disables the LAM request.

Notes: i can range from 0 to 5.
Dataway inhibit (I) prevents counting.
X = 1 for all valid addressed commands.

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